DEVICES FOR TERABIT OPTICAL NETWORKS, AN OVERVIEW AND TRENDS

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In this paper we describe and demonstrate a new generation of all-optical devices (Demultiplexer, Routing switch and Clock extractor) based on a recently developed Terahertz Optical Asymmetric Demultiplexer (TOAD). These devices are capable of ultrafast all-optical operation and can be used in the future terabit optical networks.

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1 Introduction

Today's communication WDM or OTDM networks, packet- or circuit-switched, are characterized by hybrid architectures. In these architectures, electronic nodes are connected by optical links and switching is usually performed electronically using optoelectronic devices. However, the relatively low transmission bandwidth of the electronics and the associated optoelectronic interfaces, present an obstacle to fully utilize the large bandwidth offered by optical fibers. This obstacle can be eliminated if signals remain in optical form during address recognition/demultiplexing, switching, and other signal processing such as clock recovery.

The first step in completing all-optical path is to eliminate an opto-electronic conversion associated with packet address reading and use all-optical address recognition/demultiplexing instead.

The second step to complete the all-optical transmission path is to replace gigahertz bandwidth (opto)electronic switches with terahertz bandwidth all-optical routing switches. All-optical switches also avoid the delays associated with optoelectronic conversion, and if needed, can preserve the phase information carried by the light. In contrast to electronic switches, large throughput can be achieved in all-optical switching architectures through very high transmission bandwidth rather than large dimensionality.

The third step in completing the all-optical path is to replace the electronic signal processing associated with switching by all-optical signal processing. One very important issue is self-synchronization of an optical node based on clock extraction. If this can be achieved all-optically it can avoid a data flow bottleneck at the input to the photonic switch and also can reduce the need for flow control.

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In this paper we describe and demonstrate a new generation of all-optical devices (Demultiplexer, Routing switch and Clock extractor) based on a recently developed Terahertz Optical Asymmetric Demultiplexer (TOAD). These devices are capable of ultrafast all-optical operation and can be used in future terabit optical networks:

- for ultrafast all-optical demultiplexing.
- for ultrafast all-optical address recognition and ultrafast all-optical switching of photonic packets without the need for any opto-electronic conversion.
- for all-optical clock recovery using an all-optical thresholding device. Recovered optical clock is then used as an optical synchronization pulse by optical node.

We have demonstrated that even with bit rate as high as 0.25 Tbit/s (4 ps spacing between bits) the bit error rate is less than 10^{-9}, with strong jitter immunity.

2 New generation of ultrafast all-optical devices

Many functions must be performed in order to control traffic in networks. In ultra-high speed optical networks, bits in optically compressed packets are spaced only picoseconds apart. Before the routing of incoming packets at a switching node can take a place, destination address of an incoming packet must be obtained from the packet header. However, because of the high speed, address recognition can only be performed by using ultrafast all-optical demultiplexers. Once the address bits of the packet are read, the routing switch is set by a routing controller to properly route the packet(s). One device capable of reading address bits at such high bit rates is the Terahertz Optical Asymmetric Demultiplexer - TOAD [1,12]. This device, in principle, can demultiplex a picosecond time-slot from a nanosecond address-frame. It requires less than one picojoule of switching energy and can be made small enough to be integrated on a chip. In the next paragraph we will briefly review TOAD operation.

2.1 Ultrafast all-optical demultiplexer

The TOAD (Fig. 1a) is composed of a small optical fiber loop mirror, a nonlinear element - semiconductor optical amplifier (SOA), an intraloop 2×2 coupler for injecting control pulses into the SOA, and an adjustable fiber delay line (AD) which positions SOA near the optical midpoint of the loop mirror. When a train of closely spaced address bit pulses enters the TOAD, each address bit splits equally into a clockwise component (CW) and counterclockwise (CCW) component. They counter-propagate around the loop and arrive at the SOA at slightly different times as determined by the offset, Δx, of the near edge of the SOA from the midpoint of the loop. A control pulse arrives at the SOA before the CCW component of the signal pulse (address bit) which is to be demultiplexed. It arrives just after its CW counterpropagating component, and induces nonlinearities in the SOA which cause the two components to experience different losses and phase shifts. They then recombine and exit the loop at the output port. All other address bit pulses (for which the counterpropagating components do not straddle the control pulse arrival at the SOA) exit the loop at the input port.

As seen in Fig. 1b, the rising edge of the normalized output intensity, when measured as a function of the delay of the signal pulse relative to the control pulse, is nearly a step function (it

Fig. 1. a) TOAD diagram, SOA -semiconductor optical amplifier, P -polarizer, PLC -polarization loop controller, AD - adjustable delay; b) 4 ps switching window.

”follows” the rising edge of the control pulse). The duration of the falling edge is limited by the transit time through the SOA, nL/c_0, where n and L are the refractive index and length of the SOA respectively. The duration of the flat top is $2n_g\Delta x/c_o$, where n_g is the refractive index of the loop and c_0 is the speed of light in vacuum. The switching window is defined here as the full width at half maximum (FWHM) of the normalized output intensity as indicated in Fig. 1b. This 4 ps switching window was obtained when a 500 μm long SOA was placed asymmetrically at about the loop midpoint with one end approximately 100 μm from the loop midpoint. The pulse energy in each address bit was 100 fJ. 600 fJ of control pulse energy was needed to induce sufficient nonlinearity for demultiplexing the address bits at 250 Gb/s.

2.2 Ultrafast all-optical routing switch.

The future fiber-optic networks will place severe demands on the transmission bandwidth and reconfiguration speed of routing switches. It will be difficult for current opto-electronic switches (2×2 LiNbO3 cross-bars, maximum speed of several tens of GHz) to match the required speed of future ultrafast optical networks. This has spurred investigation and development [1–6] of a new type of all-optical devices for optical nodes a) for address recognition [1,2] and b) for routing [3] to increase their speed by eliminating opto-electronic conversion within the node. In general, the switching node (Fig. 2) consists of an switching element (SW) with two possible states, switched (cross) or unswitched (bar) state, an ultra-fast all- optical address recognition unit (ARU) which decodes the destination address, an electronic routing controller which sets the state of the switching element, and an optical buffer that matches the delay of the input packets to the processing delays of the routing controller.

In future optical networks, in addition to new types of ultrafast all-optical devices, using single bit addressing rather than binary addressing may be preferable to centralize control because the state of the switch must change very quickly [7]. A banyan network where no look-up table

Fig. 2. Node diagram with incoming photonic packets.

is needed and packets are self-routed through the switch by examining only one address bit is well-suited for ultrafast-packet switching. One ultrafast all-optical low-power device capable of performing all of these necessary functions in this type of the networks is modified TOAD.

To demonstrate all-optical address recognition and single bit self-routing, one node of a banyan-type network (see schematic in Fig. 3b was constructed using two TOADs. Photonic packets, with a 4 ps bit period (e.g. 250 Gbps), were composed of a large amplitude leading clock pulse, a three bit header, and an empty payload (see timing diagram in Fig. 4a). The switching node consists of an all-optically controlled routing switch (TOAD2 with $\Delta x = Tc/2$) in a switched or unswitched state, an ultrafast routing controller (TOAD1 with $\Delta x = \tau c/2$) that all-optically sets the state of the routing switch (TOAD2), and an optical buffer that matches the delay of the input packet to the processing delay of the routing controller. Fig. 4a shows the input multiplexed high intensity clock and two packets: ”1110 . . 0” and ”1010 . . . 0”. The 4 ps temporal separation of the header bits results in the different headers appearing as cumulative ”double height” (101 bit sequence) and ”triple height” (111 bit sequence) pulses when observed on a band limited oscilloscope (Fig. 4b).

After entering the node, the clock is separated from the optical packet using a polarization beam splitter, PS. Before entering the buffer, a portion (10%) of the packet is split off and sent to TOAD1 which reads the packet destination address bit. The demultiplexed address bit, after passing through an optical isolator (OI), is amplified in a Semiconductor Optical Amplifier (SOA) and then used as the optical routing control for the routing switch (TOAD2).

In a single bit routing scheme, we first use address bit 2 (alternately ”1” or ”0”) as the routing bit for the TOAD2.

Packets with address bit 2 with value ”1” are routed to output port Out 2, while packets with

Fig. 3. a) Terahertz Optical Asymmetric Demultiplexer; b) Switching node diagram with bit 2 as the routing signal.

Fig. 4. Node input; a) timing diagram; b) incoming packets as seen on a bandwidth limited oscilloscope.

address bit with value ”0” are routed to output port Out 1. This results in triple height pulses (the packets with header ”111”) at output port Out 2, and double height pulses (the packets with header ”101”) at output port Out 1 (see timing diagram in Fig. 5a). Fig. 5b is an oscilloscope photograph of the outputs of the routing switch, TOAD2 as seen on a bandwidth limited oscilloscope.

In the next experiment, we use bit 1 (always ”1”) as the routing bit. In this case, both packets are routed to output port Out 2 (see timing diagram in Fig. 6a). This results in zeroes at the output

Fig. 5. Output of the switch. Address bit ”2” is used as the routing signal; a) timing diagram (different packets appear as cumulative ”double height” (101 bit sequence) and ”triple height” (111 bit sequence) pulses on a bandwidth limited oscilloscope); b) Experimental demonstration.

port Out 1 and alternate double height (the packets with header ”101”) and triple height pulses (the packets with header ”111”) at the output port Out 2. Fig. 6b is an oscilloscope photograph of the outputs of the routing switch, TOAD2, as seen on a bandwidth limited oscilloscope.

In conclusion, we demonstrated all-optical ultrafast switching with single bit all optical routing control in a banyan type network. Both ultrafast address recognition and ultrafast routing of photonic packets were performed all-optically on a header in which the bit period was only 4 picosecond in duration (e.g. at 250 Gbps data rate). Photonic packets were self-routed through an all-optical ultrafast switch without the need for opto-electronic conversion. Two TOADs were used in different regimes: as an ultrafast all-optical routing controller, and as an ultrafast all-optically controlled routing switch. The bit- error rate at the switching element was measured to be less than 10^{-9}. All of these results indicate that the TOAD is a well-suited device for applications in ultrafast all optical banyan networks.

2.3 All-optically processed clock recovery for self-clocked ultrafast OTDM networks

As the transmission rate increases in the OTDM networks, synchronization is becoming a challenging task. Some recent demonstrations show it is possible to operate networks at bit rates up to hundreds of gigabits per second [8,9]. At these speeds, conventional bandwidth limited electronics can not be used to solve the network synchronization problem. To overcome this difficulty, a self-clocking scheme [10], in which an optical clock and data are generated from the same light source and distributed globally throughout the network, has been introduced previously. At the receiving end, clock and data are separated from each other and used for further processing. This becomes increasingly difficult at higher and higher bit rates.

For the separation of clock and data from a self-clocked OTDM network, either a polarization or an intensity selection technique can be employed. It has been previously demonstrated that clock and data can be transmitted with orthogonal polarization so that a passive optical device,

Fig. 6. Output of the switch. Address bit ”1” is used as the routing signal; a) timing diagram (different packets appear as cumulative ”double height” (101 bit sequence) and ”triple height” (111 bit sequence) pulses on a bandwidth limited oscilloscope); b) Experimental demonstration.

a polarizer, can be used to separate the signals at the processing end [9,11]. To maintain the orthogonal polarization between clock and data pulses, this scheme requires polarization control or PM components throughout the network. A practical method is to distinguish the clock and data by different intensities. For such a system, an intensity-dependent optical device with ultra-fast switching capability is required to separate the clock from the data. In addition, the recovered clock signal should have sufficient intensity to control an all-optical demultiplexer such as a Terahertz Optical Asymmetric Demultiplexer (TOAD) [12].

We present all-optical processing of clock recovery and demultiplexing for self-clocked 100 Gb/s OTDM systems. Without additional amplification, the recovered clock and data signal can be used directly as the control and data signal input for a TOAD respectively. Finally, demultiplexing one of the data channels is demonstrated at 100 Gb/s using a TOAD.

An experimental demonstration setup is shown in Fig. 7a. A mode-locked 100 MHz Nd:YLF laser with a pulse compression stage generates a train of picosecond pulses. The pulse train is coupled into an optical fiber and split using 2×2 couplers to generate one clock and two data pulse trains. For the input self-clocked cell, the clock and data pulses are multiplexed according to the timing diagram as shown in Fig. 7b. Each cell has a period of 10 ns and contains a clock pulse which has a higher intensity in a designated time slot preceding the transmitted TDM data. The spacing between the clock and the first data is 100 ps. This 100 ps ”guard band” is necessary to distinguish clock and data signals detected by a low bandwidth opto-electronic detection system for the purpose of our experiment. The spacing between adjacent data bits is 10 ps, corresponding to an effective aggregate bit rate of 100 Gb/s. For the experiment, time slot 1 is encoded with a ”1111...” sequence and slot 2 with a ”1010 ...” sequence. We leave the remaining slots empty. The clock and data pulse energies are 200 fJ and 40 fJ respectively, and there is no definite polarization relationship between them. At the receiving end of the network, the high intensity clock signal is first extracted from the weak data signals and then used to demultiplex the data in the TOAD. As shown in the inset, the receiver consists of two parts: the thresholding device for clock and data separation and the demultiplexer. The thresholding device is based

Fig. 7. a) The experimental set-up for the demonstration. MOD: EO modulator, BF: optical bandpass filter, PD: photodetector, and SOA: semiconductor optical amplifier; b) Timing diagram for the clock and data in the self- clocked cell. The cell contains a clock pulse and 2 aggregated TDM channels (CH1,2) at 100 Gb/s in a 10 ns time frame. A maximum of 990 channels can be accommodated in this cell.

on a fiber loop mirror with a SOA asymmetrically placed in the loop. The switching window is determined by the offset of the SOA position. A 2×2 coupler with the power splitting ratio of 20:80 is used in the loop. The driving current of the SOA and the uneven coupler in the loop mirror set the threshold energy of this device. Once the energy of the input pulse is above the threshold, the device is able to perform the thresholding function: rectifying, amplifying, then switching the optical pulse to the transmitted port (CLK Out). The input data pulses which have intensities less than the threshold will be reflected back by the loop mirror. Thus the clock and data pulses are separated. The detailed principle of operation of this switch has already been described elsewhere [13].

A bandwidth limited oscilloscope trace of the multiplexed signal is shown in Fig. 8a. The strong pulse is the clock signal and the weak pulse is the data signal. The data signal consists of two optical pulses which represent two different 100 Gb/s channels in the OTDM systems.

Fig. 8. Experimental demonstration of the clock extraction. a) The clock pulse (with higher amplitude) followed by two data pulses at the input of the all-optical separator. b) The extracted clock pulse at the CLK Out port. c) The clock and data pulses reflected to the DATA Out port.

However, these two optical pulses can not be resolved in the figure due to the limited bandwidth of the detection system. The transmitted and reflected signals from the thresholding device are measured with a bandwidth limited oscilloscope, and shown in Figs. 8b and 8c respectively. The strong signal shown in Fig. 8b is the transmitted clock. Since a semiconductor optical amplifier is utilized as the nonlinear optical element in the clock-and- data separator, the extracted clock signal obtains a gain of 5. The transmitted data signals which are 100 ps behind the clock signal are negligible. At the reflected port (DATA Out), the clock and data signals appear together as shown in Fig. 8c. Since the residual clock signal has an intensity comparable to the data but occupies a different time slot, it can be treated as another TDM data channel in the cell. Without the strong optical clock which may cause a saturation, the reflected data cell can also be fed directly into the TOAD for demultiplexing. After clock and data separation, the transmitted signal, comprised mostly of the clock signal, is sent to the control port of the TOAD. The reflected signal from the separator is used as the data input to the TOAD as shown in Fig. 7. inset. For the TOAD to select time slot 2, the recovered clock signal is time delayed accordingly. The demultiplexed signal of time slot 2 output from the TOAD, a ”1010...” pattern at 100MHz, is shown in Fig. 9. The pattern is the same as the modulation pattern encoded initially in time slot 2. Undesired signals, such as time slot 1 and the clock signal, are reflected by the TOAD and are negligible at the TOAD output. This is verified by modulating a ”0” in time slot 2 and observing the TOAD output. From this result, the contrast ratio between the ”1” and ”0” state of the demultiplexed output is high ($\sim$ 10 dB).

In conclusion, clock and data signals are separated from a 100 Gb/s self-clocked OTDM sys-

Fig. 9. Experimental result of the demultiplexed output of CH2 with "1010" pattern at 100MHz.

tem using an ultra-fast all- optical intensity-dependent switch. The recovered clock signal is 5 times larger than the input clock signal. This recovered clock signal has sufficient intensity to control a TOAD. Therefore, the recovered clock can be used without additional amplification as the control signal, and the reflected signal as the data input to a TOAD. The processing is performed at a relatively low energy of less than 200 fJ for both the clock extraction and demultiplexing. This all-optical scheme may be useful for emerging ultrafast OTDM networks.

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