The Analysis and Application of Resistive Superconducting Fault Current Limiters in Present and Future Power Systems

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This thesis is the result of the author's original research. It has been composed by the author and has not been previously submitted for examination which has led to the award of a degree.

Abstract

Fault current levels in electrical systems are rising due to natural growth in demand, the increasing presence of distributed generation (DG), and increased network interconnection. This rising trend is expected to continue in the future. Marine vessel power systems are highly power-dense and are often safety-critical. Power system protection is increasingly challenging in these systems. Superconducting fault current limiters (SFCLs) offer an attractive solution to many of the issues faced.

This thesis establishes and reviews the state of the art in resistive SFCL technology and application knowledge, and provides crucial research-based guidance for the adoption of resistive SFCLs in future power systems.

The issues associated with the application of resistive SFCLs—including location, resistance rating, the recovery period, and interaction with protection systems—are demonstrated. The relationship between several resistive SFCL design parameters is established using a generic analytical approach, hence providing a framework for validating SFCL designs. In particular, it is shown that a particular SFCL resistance rating leads to a peak in the superconductor energy dissipation, which generally should be avoided.

It is proven that resistive SFCLs have an inverse current-time characteristic, i.e., they will operate in a time that inversely depends upon the initial fault current magnitude. This knowledge is critical for underpinning the operation of a novel protection scheme using multiple resistive SFCLs. The scheme offers several advantages: very fast-acting operation in response to faults anywhere on the system under study; maximum prospective fault currents are prevented from occurring, reducing the duty on circuit breakers; inherent, fast-acting backup; and communications is not required. It is shown that the scheme is suited to highly-interconnected systems with a high presence of DG. The scheme is readily applicable to the design of future utility and marine vessel power systems.

Acknowledgements

I'd like to thank my supervisors, Prof Graeme Burt and Dr Campbell Booth. Their interest and dedication to my research is truly heroic. I've got a lot out of the time I've spent in our research group, so I'm—retrospectively—immensely grateful for the opportunity to do a PhD at Strathclyde.

I owe a lot of gratitude to others in our research group: Dr Ian Elders, Dr Andrew Roscoe, Dr Stuart Galloway, and Dr Steven Fletcher. There are many others who kept me going, and they know who they are.

Our colleagues at Rolls-Royce provided valuable guidance for my work, and I'd like to thank Chris Bright, Dr Jason Hill, Rob Slater, Jamie McCarthy, and Dr Anita Teo.

A great thanks to Lynsey Connie for her help reviewing my thesis.

I'd especially like to thank my parents, Sam and Linda, for all their support over the years. This thesis is dedicated to them.

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Glossary of Abbreviations

AC	Alternating Current
BSCCO	Bismuth Strontium Calcium Copper Oxide
CB	Circuit Breaker
CIGRÉ	Conseil International des Grands Réseaux Électriques
CDD	Current Division Discrimination
CT	Current Transformer
DC	Direct Current
DG	Distributed Generation
EPRI	Electric Power Research Institute
FCL	Fault Current Limiter
FEA	Finite Element Analysis
HTS	High-Temperature Superconductor
HV	High Voltage
HVDC	High Voltage Direct Current
IEC	International Electrotechnical Commission
IDMT	Inverse Definite Minimum Time
IFEP	Integrated Full-Electric Propulsion
LV	Low Voltage
MV	Medium Voltage
NOP	Normally-Open Point
PSCAD	Power Systems Computer Aided Design
RMS	Root Mean Square
RTDS	Real-Time Digital Simulator

SFCL	Superconducting Fault Current Limiter
SSCB	Solid State Circuit Breaker
SSSC	Static Synchronous Series Compensators
TCSC	Thyristor-Controlled Series Capacitor
TMS	Time Multiplier Setting
TRV	Transient Recovery Voltage
USD	United States Dollar
YBCO	Yttrium Barium Copper Oxide
VSC	Voltage Source Converter
VT	Voltage Transformer

Chapter 1

Introduction

1.1 Introduction to the Research

Power systems are growing and changing significantly. Global demand for electrical energy is projected to double by 2050 [Wor07], continuing the trend from the previous 40 years [Int12]. This growth will be caused by an expanding population [Uni09], improved availability of electricity in developing countries [Wor07], and the increasing electrification of loads such as domestic heating and vehicles [LTHP12]. The importance of using sustainable sources of energy will have a critical impact on future power systems [Mac08b], and is already leading to an increased presence of distributed generation (DG), microgrids, DC systems, and power electronic devices. These developments add further diversity to electrical sources and loads, and thereby complicate the system protection and control.

For future power systems to cater for these fundamental changes, in many cases fault current levels will increase. For example, resiliency against blackouts is of importance in both grid [PSA+11, AAB+06] and isolated [Mar11] networks. This, amongst other factors, may necessitate increased electrical network interconnection, which normally increases fault current levels [Ten10]. The connection of DG can also significantly increase fault levels [BRB+10, STB+10] and disrupt protection coordination [DBG+07]. Furthermore, the fault current levels in power-dense marine vessel and aircraft power systems are inherently high

[BBE+11, BES+08, FNGB11].

Safe network operation is very challenging in systems with a high fault level. Power system faults can cause significant damage—to life and to equipment—at the point of fault and to any equipment carrying fault current [BBE+11, MK01]. Circuit breakers must be rated to clear faults for a particular system fault current level; higher fault currents lead to higher circuit breaker costs.

A key solution to these issues is the adoption of fault current limitation in electrical systems. Fault current limiter (FCL) devices typically do not affect power system operation during normal conditions, yet rapidly act to mitigate the destructive and other undesirable effects caused by power system faults. This thesis examines the application, design parameters, performance, and applicability of resistive superconducting fault current limiters (SFCLs), in both land-based and marine vessel power systems.

1.2 Research Motivation

There is a growing impetus for a "smarter" power grid, with ever greater reliability and efficiency. The future smart grid should: be built upon sustainable sources of power [Mac08b]; allow increased network interconnection [McN12, Ene11]; allow flexible and adaptive networks [BC12]; provide better management of power demand [CSI09]; incorporate an increased use of communications and standardisation for improved data sharing [BCBB13, EPR11]; and implement faster-acting power system protection [BES+08].

There are several barriers to this vision:

- Power networks need substantial growth, but also need a cost-effective way to delay or avoid significant upgrades. The prospective long life of power system assets leads to a largely expensive and static infrastructure. For example, for transmission network reinforcement, a 39 GW increase (a 50% increase) in UK generation capacity is expected to cost approximately £8.8bn [ENS12]. Consequently, National Grid Electricity Transmission is planning for capital expenses of £2-2.5bn per year over the next decade

[McG12]. Similarly large investments will be needed by distribution network operators [Ele12], leading to an estimated £53.4bn total transmission and distribution investment by 2025 [Ofg09].

- The UK has the ambitious target of an 80% CO_2 emissions reduction by 2050 (relative to 1990 levels) [Cro08], and to achieve this goal significant DG using renewable sources of energy must be installed [Mac08b]. Increased electrical system interconnection can improve the security of supply during periods of generation intermittency which are inherent for many forms of renewables [Ene11]. Increased interconnection also reduces transmission and distribution losses, supports the system voltage along the length of feeders, and provides greater flexibility in the use of available network capacity [McN12]. Despite these benefits, a highly-interconnected power system will typically experience very high fault currents during faults, and faults can affect a greater area of the system. Furthermore, the coordination of protection can be difficult, expensive, or impractical for distribution networks with a high penetration of DG [BG04] and for networks which are highly-interconnected [PI09] because ensuring proper coordination often requires communications for protection signalling.

- Full-electric marine vessels and aircraft have increasingly power-dense electrical systems, which leads to extraordinarily high fault currents [BBE+11, BES+08, FNGB11]. These compact, isolated systems are also particularly prone to the dangers of arcing faults and blackouts [Mar11, SE12].

- There are several instances where circuit breakers in UK distribution systems are already over-stressed [BRB+10], which limits the network performance and flexibility, and prevents the connection of DG—including renewable sources. Therefore, higher fault levels can result in early obsolescence of existing circuit breakers, as well as incurring the replacement costs or other forms of network reinforcement. The size and weight of circuit breakers are additional constraints for marine vessel, aircraft, and offshore applications.

Therefore, in many circumstances fault current levels are already high or are

expected to rise. Conventional methods of reducing fault currents, which include splitting busbars and increasing system impedance, have significant operational shortcomings, such as reduced security of supply for customers or increased system losses. There has been an increased need for technologies, such as SFCLs, which avoid these issues. Consequently, significant world-wide SFCL development, including several system trials, has been undertaken over the past decade [NS07, Eck08], particularly in the UK, the USA, South Korea, Japan, Germany, and Italy.

Nevertheless, SFCLs are a relatively new technology and network operators need to understand the best ways to use SFCLs. This thesis provides such guidance. In particular, this thesis highlights the challenges with using SFCLs, advises on key SFCL design decisions, and analyses the application of multiple SFCLs in electrical networks, including the relevant control and protection issues.

1.3 Principal Contributions

This thesis provides the following contributions to knowledge:

- Investigation and quantification of the challenges involved with the application of fault current limitation in power-dense electrical systems.
- Evaluation and implementation of appropriate SFCL models for power system simulation.
- Analysis of the key SFCL design factors which determine the energy dissipation in resistive SFCLs. This affects the SFCL device recovery time and the level of fault current limitation, which are important for grid applications. This work thereby provides a generic methodology for validating the design of a resistive SFCL.
- Establishment of the fact that the minimum required volume of superconductor varies linearly with SFCL resistance but, for a given level of fault current limitation and power rating, is independent of system voltage and superconductor resistivity.

- Establishment of the fact that resistive SFCLs intrinsically have inverse current-time characteristics, and analysis of the implications of this for power system protection. This has been achieved through a mathematical derivation and also has been illustrated using simulations.

- Design, demonstration, and analysis of a fast fault detection method using multiple SFCLs. This method can provide the same—or better—performance as unit protection over a wide area, but without the need for communications.

- Recommended applications of and caveats with a fault detection method using multiple SFCLs.

1.4 Thesis Overview

Chapter 2 reviews the relevant background material. The chapter introduces power system protection, and emphasises the challenges with protecting present distribution and marine vessel networks. An overview of FCLs, focussing on resistive SFCLs, is provided in Chapter 3. Chapter 4 builds on this discussion to highlight the challenges related to the application of fault current limitation.

Energy dissipation in resistive SFCLs is investigated in Chapter 5. The implications for power system performance, SFCL recovery time, and the volume of superconductor required—and therefore SFCL cost—are analysed.

In Chapter 6, a representative resistive SFCL model is analysed to evaluate its dynamic characteristics during faults. The results are used in Chapter 7 to evaluate a fast-acting method of detecting and isolating faults in electrical systems using multiple SFCLs, without needing communications. The recommended applications and potential disadvantages of this method are explored in detail.

Chapter 8 concludes this thesis by summarising the contributions of the research. Further work, which leads on from this thesis, is also suggested.

1.5 Publications

The following publications have been completed during the course of this PhD:

1.5.1 Journal Articles

Measurement of 40 Power System Harmonics in Real-Time on an Economical ARM Cortex-M3 Platform
A.J. Roscoe, G. Oldroyd, T. Sklaschus, S.M. Blair, and G.M. Burt
IET Electronics Letters, volume 49, issue 23, 7 November 2013, p. 1475 - 1476
doi: 10.1049/el.2013.0299

Application of Multiple Resistive Superconducting Fault Current Limiters for Fast Fault Detection in Highly-Interconnected Distribution Systems
S.M. Blair, C.D. Booth, G.M. Burt, and C.G. Bright
IEEE Transactions on Power Delivery, vol. 28, no. 2, pp. 1120-1127, April 2013
doi: 10.1109/TPWRD.2012.2228011

An Open Platform for Rapid-Prototyping Protection and Control Schemes with IEC 61850
S.M. Blair, F. Coffele, C.D. Booth, and G.M. Burt
IEEE Transactions on Power Delivery, vol. 28, no. 2, pp. 1103-1110, April 2013
doi: 10.1109/TPWRD.2012.2231099

Current-Time Characteristics of Resistive Superconducting Fault Current Limiters
S.M. Blair, C.D. Booth, and G.M. Burt
IEEE Transactions on Applied Superconductivity, vol. 22, no. 2, pp. 5600205, April 2012
doi: 10.1109/TASC.2012.2187291

Superconducting Fault Current Limiter Application in a Power-Dense Marine

Electrical System

S.M. Blair, C.D. Booth, I.M. Elders, N.K. Singh, G.M. Burt, and J. McCarthy

IET Electrical Systems in Transportation, vol. 1, iss. 3, pp. 93-102, September 2011

doi: 10.1049/iet-est.2010.0053

Analysis of Energy Dissipation in Resistive Superconducting Fault Current Limiters for Optimal Power System Performance

S.M. Blair, C.D. Booth, N.K. Singh, G.M. Burt, and C.G. Bright

IEEE Transactions on Applied Superconductivity, vol. 21, no. 4, pp. 3452-3457, August 2011

doi: 10.1109/TASC.2011.2129518

1.5.2 Conference Papers

Demonstration and analysis of IP/MPLS communications for delivering power system protection solutions using IEEE C37.94, IEC 61850 Sampled Values, and IEC 61850 GOOSE protocols

S.M. Blair, F. Coffele, C.D. Booth, B. De Valck, and D. Verhulst

CIGRÉ Session, Paris, France, 2014 (accepted)

Improving IEC 61850 interoperability and simplifying IED configuration through the standardisation of protection settings

Q. Hong, V.M. Catterson, S.M. Blair, C.D. Booth, A. Dyśko, T. Rahman

CIGRÉ Session, Paris, France, 2014 (accepted)

Application of Multiple Resistive Superconducting Fault Current Limiters for Fast Fault Detection in Highly-Interconnected Distribution Systems

S.M. Blair, C.D. Booth, G.M. Burt, and C.G. Bright

IEEE Power & Energy Society General Meeting, Vancouver, Canada, 2013

An Open Platform for Rapid-Prototyping Protection and Control Schemes with

IEC 61850

S.M. Blair, F. Coffele, C.D. Booth, and G.M. Burt

IEEE Power & Energy Society General Meeting, Vancouver, Canada, 2013

Standardization of Power System Protection Settings Using IEC 61850 for Improved Interoperability

Q. Hong, S.M. Blair, V. Catterson, A. Dysko, C.D. Booth, and G.M. Burt

IEEE Power & Energy Society General Meeting, Vancouver, Canada, 2013

Demonstration of Adaptive Overcurrent Protection Using IEC 61850 Communications

F. Coffele, S.M. Blair, C.D. Booth, J. Kirkwood, and B. Fordyce

22nd International Conference on Electricity Distribution (CIRED), Stockholm, Sweden, 2013

Architecture for Automatically Generating an Efficient IEC 61850-based Communications Platform for Rapid-Prototyping of Protection Schemes

S.M. Blair, C.D. Booth, and G.M. Burt

PAC World Conference, Dublin, Ireland, 2011

The Use of Real Time Digital Simulation and Hardware in the Loop to De-Risk Novel Control Algorithms

S. Loddick, U. Mupambireyi, S.M. Blair, C.D. Booth, X. Li, A.J. Roscoe, K. Daffey, and J. Watson

European Conference on Power Electronics and Applications, Birmingham, UK, 2011

The Use of Real Time Digital Simulation and Hardware in the Loop to De-Risk Novel Control Algorithms

S. Loddick, U. Mupambireyi, S.M. Blair, C.D. Booth, X. Li, A.J. Roscoe, K. Daffey, and J. Watson

IEEE Electric Ship Technologies Symposium, Alexandria, Virginia, USA, 2011
doi: 10.1109/ESTS.2011.5770869

Investigation of Superconducting Fault Current Limiter Application in a Power-Dense Marine Electrical Network
S.M. Blair, N.K. Singh, I.M. Elders, C.D. Booth, G.M. Burt, and J. McCarthy
The 5th IET International Conference on Power Electronics, Machines and Drives (PEMD), Brighton, UK, 2010
doi: 10.1049/cp.2010.0024

Implications of Fault Current Limitation for Electrical Distribution Networks
S.M. Blair, A.J. Roscoe, C.D. Booth, G.M. Burt, A. Teo, and C.G. Bright
The 10th IET International Conference on Developments in Power System Protection (DPSP), Manchester, UK, 2010
doi: 10.1049/cp.2010.0355

Benchmarking and Optimisation of Simulink Code Using Real-Time Workshop and Embedded Coder for Inverter and Microgrid Control Applications
A.J. Roscoe, S.M. Blair, and G.M. Burt
Proceedings of the 44th International Universities Power Engineering Conference (UPEC), Glasgow, UK, 2009

Operational Control and Protection Implications of Fault Current Limitation in Distribution Networks
S.M. Blair, N.K. Singh, C.D. Booth, and G.M. Burt
Proceedings of the 44th International Universities Power Engineering Conference (UPEC), Glasgow, UK, 2009

Chapter 2

Review of Developments in Power System Protection

2.1 Introduction

This chapter reviews the background material which is relevant to the contributions of this thesis. The chapter begins by introducing the topic of power system protection, and hence establishes the motivation for curtailing the dangerous and costly effects of power system faults. Section 2.3 illustrates typical utility and marine vessel electrical systems—two key applications for fault current limitation—to highlight the main challenges associated with their operation.

2.2 Power System Protection

2.2.1 Faults

Faults can occur in power systems due to a variety of causes, including [IEE01]:

- Lightning strike to an electrical tower or to overhead lines.
- Tree branches touching overhead lines, due to weather or overgrowth.
- Overhead conductors clashing due to the wind.

- Wildlife coming into contact with equipment, such as transformer bushings.
- Accidental damage to underground cables, caused by utility maintenance personnel or by construction activities.
- Internal faults within generators, transformers, or other primary equipment, due to aging, moisture, or breakdown of insulation.
- Overvoltages due to electrical switching transients.

Faults in three-phase AC power systems are usually classified as one of the following: single-phase to earth; phase to phase; or three-phase (a "balanced" fault). Phase to phase and three-phase faults may or may not involve contact with earth. Another possible fault type is an open phase, which can be caused by a break in a conductor [IEE01]. It is also possible for one type of fault to develop into another type over time [MK01]. For example, a single-phase to earth fault may evolve into a phase-earth-phase fault [Lou10]. If the path of fault current flows through an external impedance, such as through a tree branch to earth, then this impedance is known as the fault impedance. A fault with negligible fault impedance is normally referred to as a short-circuit.

Faults can also be classified as being transient (e.g., caused by a lightning strike), permanent (e.g., a break in an underground cable), or semi-permanent (e.g., a tree branch across conductors which "burns-out" after sufficient fault current has passed through). Approximately 80-90% of faults on overhead lines are transient [Als11], and approximately 85% of faults are single-phase to earth [Cof12].

2.2.1.1 Arcing Faults

Most faults will include arcing at some stage, typically at the point of fault and between the contacts of the circuit breaker which isolates the fault [MK01]. An arc is a "cloud" of vaporised conductor which forms an ionised plasma, allowing current to pass through a dielectric material. An arc is initiated when there is sufficient ionisation of the air gap (or any dielectric medium) between two

(a) Evidence of vaporised conductor due to an arcing fault on a marine vessel transformer [Daf09]

(b) 480 V arc flash experiment [Sho11]

Figure 2.1: Arcing fault examples

conductors such that their voltage difference exceeds the dielectric breakdown voltage. There are many dangers associated with arcing faults, including:

- High risk to human life: burns, damage to eyesight and hearing due to intense pressure waves, permanently impaired balance, and loss of sense of smell [IEE02].
- Vaporised conductor (see Figure 2.1a) leads to very high temperatures (up to 20,000 °C [Lee82]), and gaseous copper, for example, expands in volume by a factor of 67,000 compared to solid copper [Lee87]. This can cause fires and severe damage to other equipment, as illustrated in Figure 2.1b.
- Due to the relatively low fault current, arcing faults can be difficult to detect, or can result in relatively long clearance times if time- and current-graded overcurrent protection is used [Lou10]. Therefore, if allowed to persist without interruption by a circuit breaker or otherwise, an arcing fault may develop into a more serious short-circuit fault. Furthermore, a long-lasting, low-current fault may cause more total damage than a short-circuit fault, which would be cleared by overcurrent protection relatively quickly [Lou10].

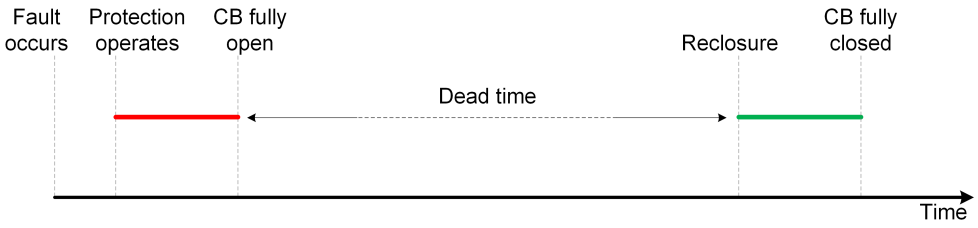


Figure 2.2: Typical autoreclose timing for a transient fault

2.2.2 Autoreclose

Autoreclose systems are commonly used to mitigate transient faults, which may include arcing at the point of fault [Als11]. After opening a circuit breaker to clear a fault, the circuit breaker is held open for a period of time, known as the dead time. The dead time allows for de-ionisation of the air gap at the fault location (or, if single-pole autoreclose is used, the dead time must also allow for the secondary arc to extinguish [Web95]). Following the dead time, the circuit breaker is reclosed to attempt to restore the supply of power. This process is illustrated in Figure 2.2.

If the fault is still present after reclosing—indicating a permanent fault—the circuit breaker will be opened and locked-out until the fault is repaired. Multi-shot autoreclose schemes involve two or more reclose stages, which can be useful for "burning-out" semi-permanent faults [Als11], but this approach has associated safety risks.

2.2.3 Earthing

The effects of faults in power systems will depend significantly on the system earthing scheme used [IEE01]:

- Solidly-earthed neutral.
- Resistance-earthed neutral.
- Inductance-earthed neutral, commonly known as a Petersen coil, or resonant earthing.

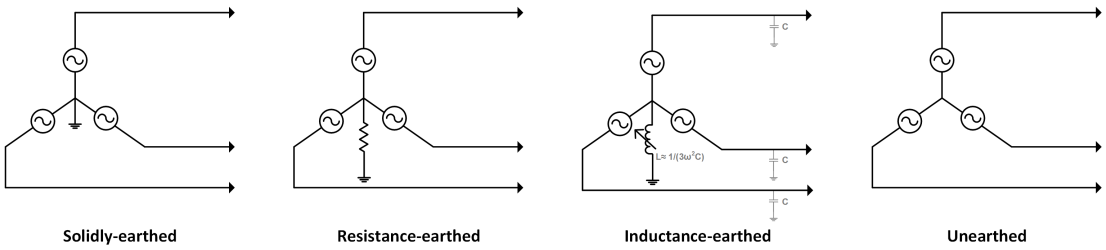


Figure 2.3: Comparison of system earthing types, shown at generator or transformer star-point connection

- Unearthed neutral, or isolated.

These earthing types are compared in Figure 2.3. In general, impedance-based earthing can significantly reduce the fault current experienced during earth faults. Unearthed systems are susceptible to transient overvoltages, particularly during single-phase to earth faults.

2.2.4 Calculating Fault Levels

The term "fault level" is used to express the prospective maximum effect of a fault at a particular location in a power system. It is typically given as a current value (in kA), or as a power rating (in MVA) at an associated voltage level. For example, typical maximum distribution system fault levels in the UK are 250 MVA at 11 kV, and 750-1000 MVA at 33 kV [Sco07, Ele10].

The IEC 60909 standard [IEC01] establishes methods for calculating fault currents in three-phase AC power systems, and defines naming conventions. The peak short-circuit current is the maximum instantaneous fault current experienced during a spontaneous short-circuit, or when a circuit breaker is closed onto a faulted circuit [Gri09].

Figure 2.4 illustrates a typical fault current waveform, for a single phase. Due to the nature of switching events in a (predominantly) *RL*-circuit, the fault current contains both an AC component and a decaying DC component. The magnitude of the DC component depends upon the current phase angle and the point on wave of fault occurrence, relative to the pre-fault voltage waveform. The DC decay time depends upon the system X/R ratio; a larger X/R ratio

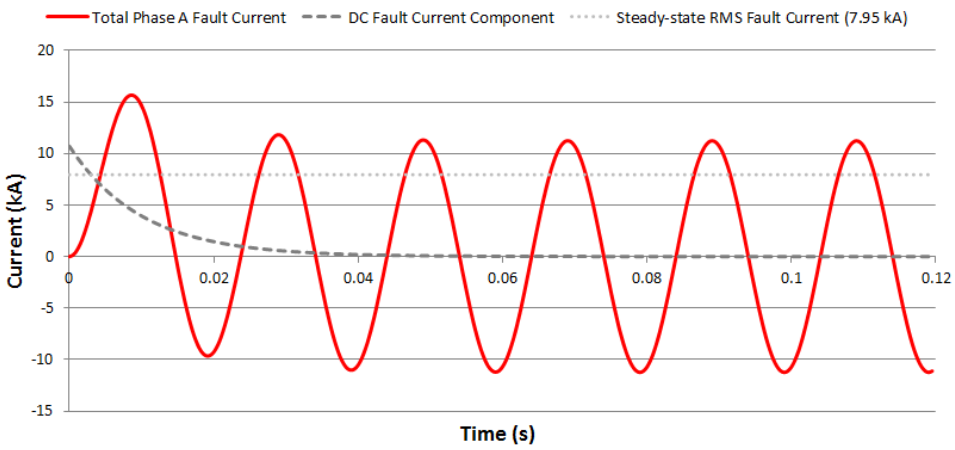


Figure 2.4: Typical fault current waveform (only phase A shown for simplicity)

leads to a longer decay time. The steady-state, or symmetrical, fault current value includes only the AC component, which is the value of fault current likely to be experienced when opening a circuit breaker.

In general, for three-phase faults, a power system can be simplified as a single-line diagram, with the fault current expressed as a differential equation, given by Equation 2.1 [Duf03]:

$$\hat{V}\sin(\omega t + \alpha) = i(t)R + L\frac{di(t)}{dt} \tag{2.1}$$

where $\hat{V}$ is the peak phase voltage, R and L are the resistive and inductive components of the system impedance, respectively, and $i(t)$ is the instantaneous phase current.

2.2.5 Conventional Protection Functionality

The role of power system protection is to detect and isolate faults. Clearly, this must be done for safety reasons, but protection is also needed to minimise the damage to power system equipment, and therefore to minimise the cost and duration of repairs. Protection systems should ensure that the minimal number of power consumers are affected by faults and, in the most extreme cases, protection aims to prevent wide-scale disruption or even blackouts in the power system.

A protection system conventionally consists of current and voltage measure-

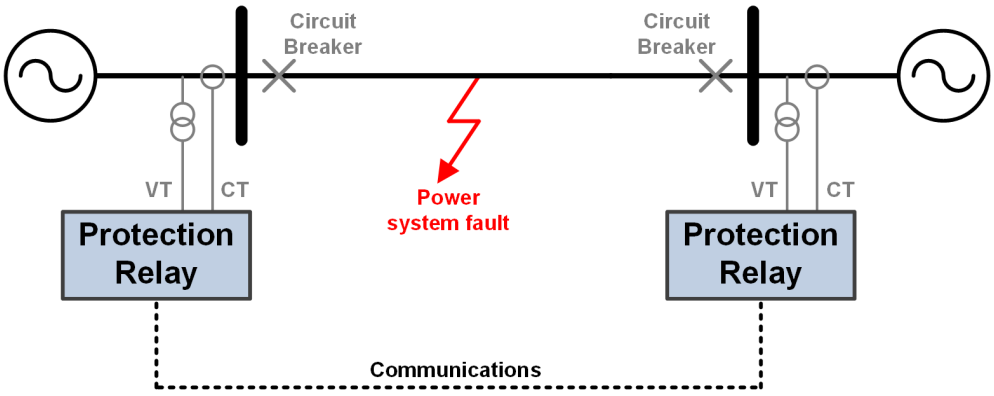


Figure 2.5: Typical two-terminal differential protection arrangement

ments, a protection relay, and one or more circuit breakers, as shown in Figure 2.5. There are several types of well-established protection functions, including: phase overcurrent, earth fault overcurrent, distance, differential, and loss of mains (which includes a variety of methods, such as under- or over-voltage, and under- or over-frequency [ENA10]). Multiple protection devices must be properly coordinated, or graded, to ensure correct and timely isolation of faults at any location throughout a power system.

2.2.6 Active Protection Research Areas

Several specific areas within power system protection are presently the subject of significant research:

- Communications is becoming increasingly important to the operation of modern and emerging protection and control schemes, particularly for managing the impact of DG [TLY09] and low voltage microgrids [Laa10, CSRAGB+12], for enabling fast-acting protection and restoration [YAA+02, BES+08, PSA+11], and for ensuring wide-area integrity of a power system [AAB+06]. IEC 61850 is an international standard which offers several benefits to these schemes, such as: high-speed Ethernet communications, a standardised data model, a formal configuration language, reduced life-cycle costs, and interoperability [Bra04, Mac06].

- Adaptive protection involves modifying protection settings in response to

changes in the electrical system. It is particularly relevant for networks with DG (see Section 2.3.1.1), for permitting islanding, and where Active Network Management (ANM) schemes may dynamically alter the electrical system topology [BC12, CBB+13].

- DC systems are of interest for several power system applications, including: relatively compact microgrid, marine vessel, and aircraft power systems [XC11]; long-distance HVDC transmission lines; and for interfacing non-synchronous sources of generation to AC systems. Protection of DC systems involves major challenges, such as the lack of a current zero-crossing for interrupting fault currents, the extremely high transient fault currents due to the discharge of capacitive filters on voltage source converters [Fle13], and the detection of faults in multiterminal systems [YFO10, FNG+12].

2.3 Typical Utility and Marine Power Systems

This section provides a summary of typical utility (i.e., land-based) distribution and marine power systems in use today, and the main protection and other operational challenges.

2.3.1 Utility Distribution Systems

Distribution systems are evolving in a number of ways, as described in the following subsections.

2.3.1.1 Increasing DG

There is an increasing presence of DG in distribution networks, as illustrated in Figure 2.6. DG can offer several benefits, such as voltage support, reduced electrical network losses, and the inherent environmental benefits from connecting renewable forms of generation. Nevertheless, DG can lead to increased fault levels at the point of connection, bi-directional power flows, and the potential for islanded operation. Each of these factors has a consequent impact on protection:

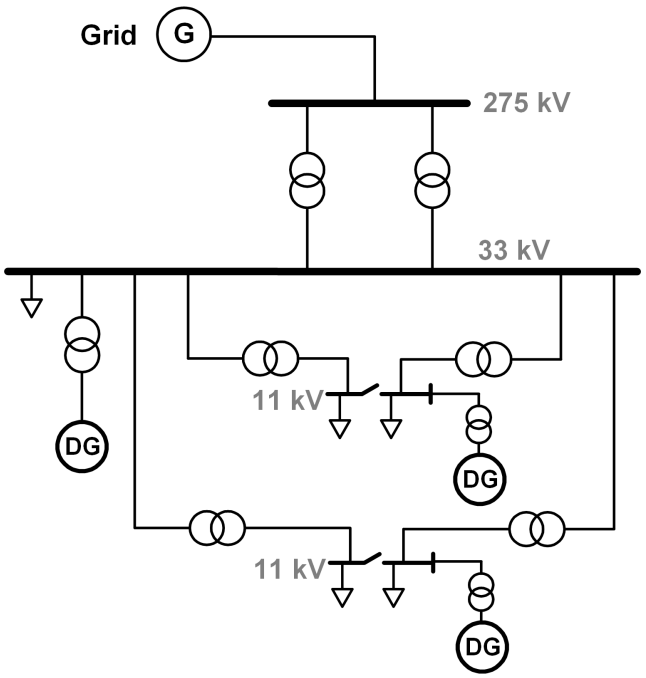


Figure 2.6: Distribution system with DG at 11 kV and 33 kV

- Increased DG has the potential to significantly increase fault current levels [SB07, Neu07]. In some cases, circuit breakers in the UK's distribution system are already stressed beyond their current breaking capability (requiring restricted network operation to alleviate the fault level constraint), and it has been shown that growth in DG may result in 1-6% of all distribution circuit breakers in the UK failing to meet prospective fault current levels [BRB+10]. This rise in fault levels must be dealt with in a cost-effective manner.

  Some forms of DG—such as photovoltaics, wind turbines, and fuel cells—are typically grid-connected via power electronic converters. To avoid damage to the internal semiconductor devices, converters must limit their fault current contribution to approximately 1-2 pu of their rated current output; these forms of DG therefore have a lower impact on fault current levels than directly-connected synchronous machines. A very high penetration of asynchronous generation could, overall, significantly reduce fault levels in the UK [Nat12].

- Several protection issues can arise due to relatively high levels of DG penetration, and the consequent opportunity for bi-directional power flows. These issues include false tripping of overcurrent relays for faults on adjacent feeders, protection blinding (where DG supports the system voltage during a fault, and thereby delays or blocks network protection due to the lower grid fault current contribution), and disruption of the grading between multiple overcurrent relays [BD00, Cof12].

- Islanding is not normally permitted within utility distribution systems. This is due to the issues involved with ensuring that the islanded system's voltage and frequency remain stable, and due to the difficulties involved with detecting faults in both islanded and grid-connected conditions [Cof12, BCBB13]. Presently, each DG owner must implement loss of mains protection to ensure that generators are tripped off in the event of disconnection from the grid [DBG$^+$07]. Nevertheless, islanding may be permitted in the future to improve the security of supply for customers.

2.3.1.2 Network Interconnection

There is a desire to increase network interconnection to improve voltage support, increase the available network capacity (and to allow more flexibility in the connection of large loads), reduce losses, and improve power quality [Ada06, McN12]. Furthermore, the connection of intermittent, renewable DG—such as wind—demands greater interconnection at both distribution and transmission levels to ensure adequate security of supply. In distribution networks, particularly at 11 kV in the UK, increased interconnection can be achieved by closing normally-open points (NOPs), as illustrated in Figure 2.7.

DG connected via power electronic converters can also inject additional harmonics into the AC power system due to their non-linear nature. This reduces power quality, leading to issues such as increased transformer losses [IEE93, Mas04]. Interconnection can mitigate this because lowering the system impedance reduces the voltage harmonic distortion resulting from non-linear currents.

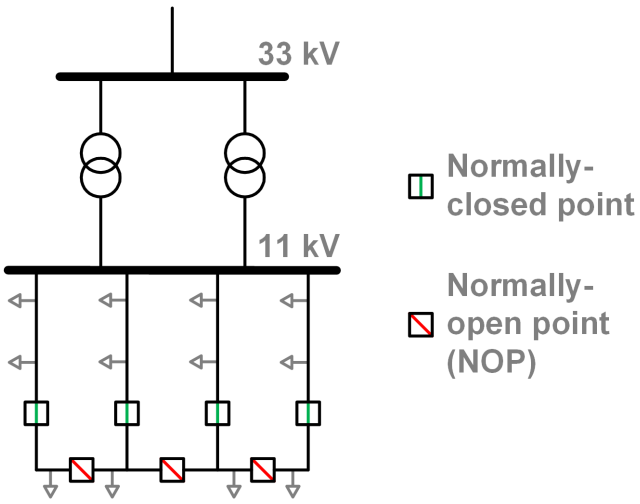


Figure 2.7: 11 kV distribution system, with potential for increased interconnection by closing NOPs

The protection issues associated with allowing electrical "loops" must be considered. In many cases, differential protection, and the associated communications, is required [Sco07].

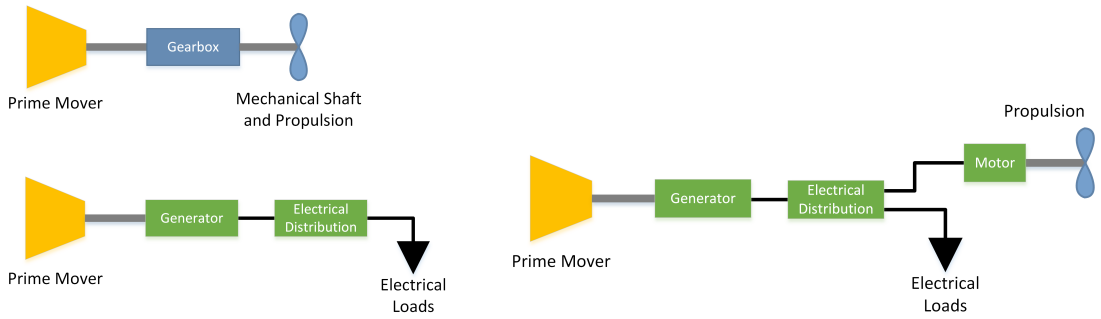
2.3.1.3 Active Network Management

ANM schemes can provide flexible, optimised operation of distribution systems. For example, ANM can facilitate the operation of networks with DG, by ensuring that constraints in fault levels (often referred to as Fault Level Management), line thermal ratings, and voltage profiles are met [MAC08a, Cof12]. Greater DG penetration is thereby possible. ANM schemes can also be used to minimise network losses, manage energy storage, and provide post-fault restoration.

2.3.2 Marine Vessel Power Systems

2.3.2.1 The Electric Ship

There has been significant motivation for full-electric designs of marine vessels [HM95], commonly referred to as Integrated Full-Electric Propulsion (IFEP) [NBS+06]. In these systems, propulsion is provided via electric motors, and all of the vessel's electrical loads share the same power distribution system. This is compared with the traditional approach in Figure 2.8.



(a) Traditional approach (b) Full-electric system

Figure 2.8: Comparison of marine vessel electrical and propulsion power systems

There are several benefits to full-electric vessel design, including [KR02, BES+08]:

- Reduced fuel use, particularly throughout the lifetime of the vessel. The unified power system allows for prime movers to be dispatched and loaded efficiently.
- Reduced space and weight requirements, because fewer generators may be needed.
- Greater flexibility in the vessel's layout, because prime movers do not need to be adjacent to propulsion devices (or coupled by long rotating shafts). Furthermore, a greater number of smaller propulsion devices can be used to improve the vessel's maneuverability.

2.3.2.2 Marine Vessel Power System Characteristics

Marine vessel power systems have the following characteristics:

- The "survivability" of the vessel is critical, particularly for naval vessels. A blackout of the power system can result in loss of propulsion, and therefore loss of control of the vessel. Electrical faults, particularly arcing faults, present a substantial risk to the operation of IFEP systems. Consequently, the electrical system must be designed for reliability [SEB+07], and DC zonal architectures have been proposed to provide greater redundancy and survivability [RBD11].

- Marine vessels need to support highly flexible levels of load, particularly for "cruise" and "boost" propulsion modes [HM95]. In some situations, the load, and the connected generation, may be as low as 10% of the full rated value [BES+08]. Vessel operations such as dynamic positioning (DP) [Rad08] and Replenishment at Sea (RAS) can involve both cyclicly varying and regenerative motor loads [ENS+07, Eld11].

- The presence of power electronic converters with high power ratings leads to severe distortion of current and voltage [SE08]. In many cases, harmonic filters are needed [CMP+07, SNG+08], with the consequent cost, weight, and space requirements, and safety issues [Mar11].

- Relatively low voltages must be used, typically no higher than 11 kV. The preference for use of low voltage marine electrical systems is driven by the costs of increased insulation associated with higher voltages, employing crew with particular operating qualifications, and increasingly stringent safety regulations.

2.3.2.3 High Fault Levels

Marine vessel electrical systems, by design, are very power-dense—in some cases with over 100 MW of generation onboard [BES+08, Roy13]. The UK Royal Navy is scheduled to become the UK's largest independent power producer by 2022, at 1.2 GW combined [Daf09]. Such power-dense, low voltage systems have the potential for extremely high fault currents [HB06].

Figure 2.9 illustrates the electrical system for a typical offshore anchor handling/supply vessel. The vessel under consideration has six synchronous diesel generators, four 2.1 MW and two 4 MW units. The 4 MW generators are associated with local propulsion and thruster motors; they are also connected to the main switchboard and are therefore capable of supplying other non-propulsive loads. The motor-generator set provides the capability for providing improved power quality—such as constant 60 Hz, 230 V output—to some 230 V loads, despite moderate variations in frequency and voltage at the 690 V switchboard.

Figure 2.10 illustrates the fault current for a short-circuit fault at the main 690 V busbar (at the location indicated in Figure 2.9).

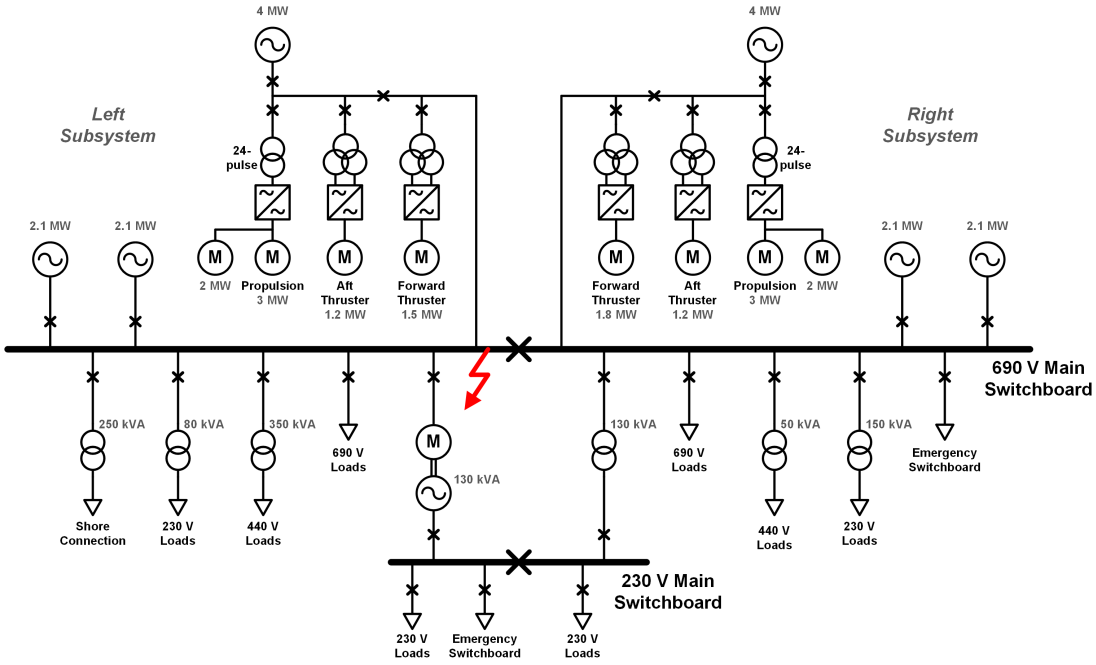


Figure 2.9: Typical marine AC electrical system

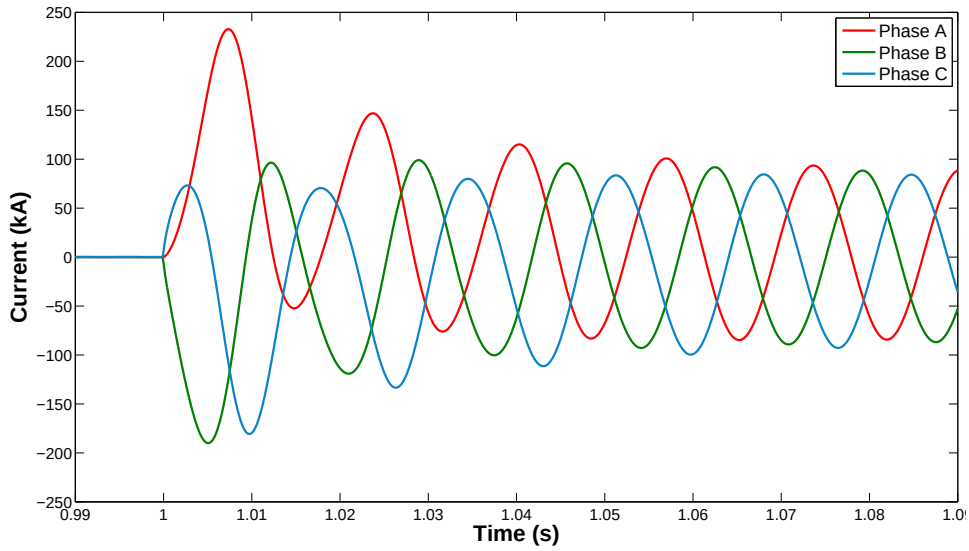


Figure 2.10: Short-circuit fault on the 690 V bus

Clearly, the prospective fault currents—with a peak value of 232 kA—are ex-

cessively high. The difficulty in procuring suitably rated circuit breakers[1] requires that the fault level must be reduced by, for example, splitting the electrical system (by opening the bus-tie circuit breakers) or inserting current-limiting reactors. These measures place operational restrictions on the vessel, such as preventing safely powering the entire system using a single generator in some circumstances; these restrictions can also reduce the security of supply.

Furthermore, high fault currents impose severe stress due to heating and electromagnetic forces [HB06, Daf09, MK01] on any equipment carrying fault current, including switchgear, cables, busbars, and transformer windings [BHH+11]. Cables must be mechanically braced to cope with the electromechanical forces [Daf09]. There is also an increase in arc incident energy [IEE02], and therefore a greater arc flash hazard, associated with higher fault currents [Bla10]. Arc flash hazard is of particular concern in marine vessels due to the confined spaces and the potential for toxic fumes [IMa11].

2.3.2.4 Other Protection Challenges

The requirements for marine protection schemes are even more stringent than for utility systems. Marine protection systems must [BES+08]:

- Be fast-acting to minimise the risk of a fault developing into a system-wide blackout.
- Operate only for faults in the desired area (unless for backup).
- Operate only the minimum number of circuit breakers needed to isolate the fault.
- Have backup protection, but which operates only if the primary protection fails.
- Adapt to highly variable fault levels, due to the large variation of load and connected generation.

[1] For example, reference [GE 13] reports a peak current rating of 108 kA and a maximum symmetrical breaking capability of approximately 40 kA RMS for 38 kV circuit breakers, and 63 kA for 15 kV circuit breakers. This is in accordance with the preferred ratings in ANSI C37.06-2000 [ANS00, Ada06]

Traditional overcurrent protection systems may be ineffective at detecting faults in all vessel operating conditions, due to the highly variable fault levels [SBBM07]. The impedances of the electrical system are typically very low due to the short cable lengths. Distance protection and current-graded overcurrent protection are impractical in these circumstances [TM06].

Chapter 3

Fault Current Limitation

References [Ada06, NS07, MF07, Eck08, Uni11] provide excellent reviews of the various methods and technologies for limiting fault currents. Section 3.1 summarises the main conventional methods, and Section 3.2 examines SFCLs in detail.

3.1 Conventional Methods of Fault Current Limitation

3.1.1 Network Strategies to Limit Fault Levels

Network operators can use several techniques to minimise fault levels. The relative merits of each method are discussed in the following subsections.

3.1.1.1 Reduce Network Interconnection

The network topology can be changed to a configuration with a lower fault current level. Typically, this involves splitting barbars by opening a busbar sectionaliser or bus coupler, as illustrated in Figure 3.1.

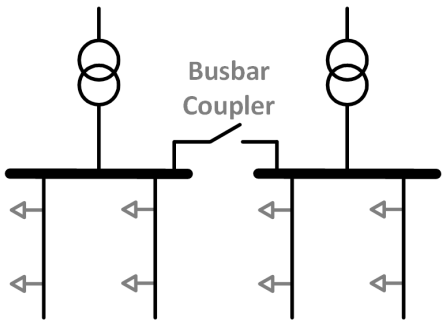


Figure 3.1: Opening a busbar coupler

This technique reduces the security of supply because it tends to separate sources from loads, increases losses, reduces voltages, and reduces grid flexibility. It can also be expensive to implement if, for example, a busbar sectionaliser does not already exist. If the busbar must be re-coupled to, for example, disconnect a supplying transformer for maintenance, generation may need to be curtailed during this period to ensure that the fault level remains within the breaking capability of the available switchgear [EA 03].

Similarly, normally-open points can be moved, such that new DG connections are made at a location with higher impedance, due to the greater electrical distance between the generator and the substation.

3.1.1.2 Increase System Impedance

Air-cooled reactors or transformers with relatively high reactance can be installed to increase the system impedance. Reactors are most commonly installed between two busbar sections [KK09]. However, increasing the system impedance leads to the following disadvantages:

- Capital expenditure for the additional equipment. However, reactors may be easier to install and operate (although they are often very large [EA 03]) and may be cheaper than SFCLs [KYT$^+$05].
- Undesirable continuous power losses, hence increasing network operational costs [Ada06].
- Power quality issues, such as increased voltage harmonic distortion and reduced transient stability margins [MF07], due to the associated voltage

drop across the additional impedance [Cer99]. This is highly undesirable in present and future networks [SB07].

Assuming the fault level increase is the result of increased DG, these disadvantages may lead to a sub-optimal supply to customers during periods where the DG is disconnected [EA 03].

Current-limiting reactors have been installed in marine vessels, such as for limiting DC current on the RMS Queen Mary 2 [Mar11].

3.1.1.3 Higher System Voltage

Higher voltage levels, where possible, can be introduced to reduce currents [Ada06]. Due to the greater cost of high voltage equipment, this option is unsatisfactory in many cases. Furthermore, this option is also not likely to be applicable to existing systems, and other methods of fault current limitation must be considered.

3.1.1.4 Sequential Circuit Breaker Tripping

Sequential circuit breaker tripping is a protection scheme which typically involves opening an upstream circuit breaker, relatively far from the fault, that is rated to handle the maximum prospective fault current. A downstream circuit breaker (ideally, the circuit breaker nearest the fault), which has a much lower rating and is cheaper, can then be opened due to the reduced, or zero, current flow. Finally, the upstream circuit breaker is re-closed.

This scheme increases the overall time required for fault clearance and load restoration. Opening an upstream breaker causes disruption to a wider area of the network (including non-faulted zones) than a downstream breaker located closer to the fault.

A similar approach, which may avoid expensive circuit breaker upgrades, involves tripping a contributor to the fault current (such as DG) to reduce the fault current such that the fault can then be cleared by the appropriate circuit breaker [EA 06]. However, fault clearance times are increased, tripping the sources of supply is undesirable, communications may be needed, and the safety repercussions are severe if the scheme fails.

3.1.2 Non-Superconducting FCL Devices

3.1.2.1 I_s-Limiters

I_s-limiters (where I_s stands for "short-circuit current") are devices which quickly route fault current through a high-impedance shunt or a current-limiting fuse, by detonating a small explosive charge. This process must be initiated by fault detection circuitry. It is particularly attractive for MV systems with high prospective fault currents, as a cost-effective and faster-operating alternative to a circuit breaker [SSM+05]. At present, devices are available to interrupt a symmetrical fault current of up to 300 kA at 15.5 kV [Aar13]. Over 2,500 devices are in operation throughout the world [Har12] and have been required for naval vessel systems [SSM+05].

However, there are concerns if the device fails to operate; the probability of failure to operate has been estimated at 1 in 1.75 x 10^{-3} [Par04]. The cost of an I_s-limiter is comparable to an equally-rated circuit breaker, but I_s-limiters are restricted to a single-use, require isolators (at additional cost) for safe replacement, require a special enclosure in the substation [EA 03], and the fault current triggering threshold cannot easily be varied after deployment. The use of I_s-limiters could increase customer interruptions and customer minutes lost if nuisance-tripping occurs.

3.1.2.2 Solid State FCLs

There are several methods for limiting fault currents using power electronic devices:

- As described in Section 2.3.1.1, converter-interfaced generation will inherently limit its contribution to fault current.
- Solid state circuit breakers (SSCBs) use power electronic switches to quickly interrupt fault currents. Nevertheless, SSCBs based on insulated-gate bipolar transistors (IGBTs) have relatively high on-state losses of approximately 1% of the rated load power during normal operation [APRP06]; switches

based on thyristors can have lower losses and faster switching [MF07]. Varistors are needed to prevent overvoltages across the IGBTs or thyristors due to the high $L\frac{di}{dt}$ experienced during current interruption [MF07]. At present, few devices are commercially available, particularly at high fault current ratings [Fle13]. The devices have a high cost and low reliability [Neu07].

- Thyristor-controlled series capacitors (TCSCs) can be used to provide both series compensation during normal conditions, and fault current limitation during faults. As shown in Figure 3.2, thyristors (or gate turn-off thyristors) can be controlled to insert a resonant LC circuit, which is tuned to impede current at the fundamental power system frequency. A mechanical circuit breaker can thereby more easily isolate the fault due to the reduced fault current. Typically, fault detection circuitry is required, although passively-triggered devices have been proposed [GF12]. Due to the cost of TCSCs, their use for fault current limitation is mainly applicable if a TCSC device already exists for series compensation.

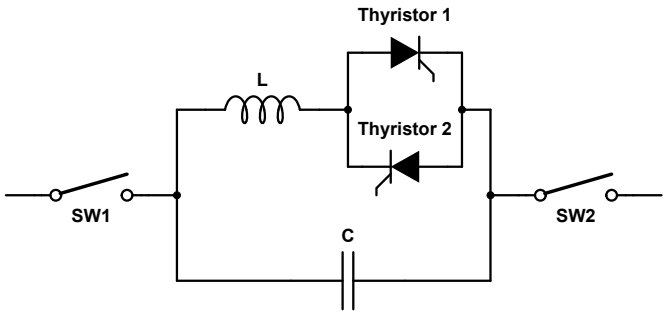


Figure 3.2: Typical resonant fault current limiter [Kar92]

- Static synchronous series compensators (SSSCs) are used to control real and reactive power flows and to dampen power swings in transmission lines, by injecting voltages using a voltage source converter [DMTH00, The13]. Similarly to TCSCs, using SSSCs for fault current limitation is only recommended if the device already exists in the system [MF07].

3.2 Superconducting Fault Current Limiters (SFCLs)

Superconductivity was first discovered by Kamerlingh Onnes in 1911 [Sta02], where mercury was found to have zero electrical resistance at temperatures below 4 K. There are several attractive applications of superconductivity in power systems, including transmission cables, transformers, magnetic energy storage, and electrical machines [Sta02]. The first superconducting fault current limiters (SFCLs) were proposed in the 1970s [GF78], and significant research and development has been undertaken, particularly since the discovery of so-called high-temperature superconductors (HTS) in 1986. HTS materials typically permit liquid nitrogen to be used for cooling the superconductor, rather than a more costly cryogen such as liquid hydrogen.

Several types of SFCL have been proposed, but this thesis focuses on the application of resistive SFCLs, as described in Section 3.2.1. For context, Section 3.2.4 describes and compares the other main types of SFCLs. Appendix A discusses the modelling of resistive SFCLs in detail.

3.2.1 Overview of Resistive SFCLs

Resistive SFCLs are the simplest and most obvious form of SFCL, because the superconductors are electrically in series with the phase conductors. Resistive SFCLs operate on the principle that passing a current, which is greater than the superconductor's rated critical current, I_c, through a superconducting wire initiates "quenching" and results in a transition to a resistive state [HB06, NS07, BSBB09]. Hence, there are virtually no electrical losses in the SFCL during normal operation, yet an SFCL intrinsically inserts impedance into the fault current path during a fault, as long as the transition threshold conditions are satisfied. Nevertheless, the superconductors may experience AC losses [Sta02] (if carrying AC), and there are power losses associated with the operation of the cryogenic system, mainly due to heat loss from the current leads which connect

the external power system to the superconducting element(s) [CK13]. Cryogenic losses are especially problematic at lower temperatures [BHH+11] and thereby have a significant bearing on SFCL design.

SFCLs are not restricted to a single current-limiting operation, but usually require a recovery period after operation, ranging from several seconds [GRS+99] to several minutes [NS07], during which the superconducting element is cooled until it returns to its superconducting state. In general, SFCLs are a much more favourable solution to addressing high fault levels than the traditional solutions discussed in Section 3.1, all of which have a number of operational and safety-related disadvantages. The operation of resistive SFCLs is described in more detail in Section 3.2.2.

Several superconductor materials have been used for resistive SFCLs, including Bismuth Strontium Calcium Copper Oxide (BSCCO), Yttrium Barium Copper Oxide (YBCO), and Magnesium Diboride (MgB_2). BSCCO is considered a first generation (1G) HTS material, whereas 2G materials such as YBCO offer higher critical current values for a given wire radius, particularly under an external magnetic field, and provide better mechanical stability. Superconductivity in MgB_2 was discovered in 2001, and the material is of interest due to its relatively low cost (approximately 2-3 USD/m) and due to its mechanical robustness [BHH+11]. However, MgB_2 has a relatively low critical temperature of 39 K, compared with 90 K for YBCO and 110 K for BSCCO.

A cross-section of a resistive SFCL device developed by Applied Superconductor Ltd., and deployed for testing in Lancashire, UK in 2009, is given in Figure 3.3 [BBE+11]. Each phase of the device consists of several superconducting "tubes" suspended in the cryogenic chamber. Each tube is made from BSCCO-2212 bulk material [BEH95, Eck09, DKH+10].

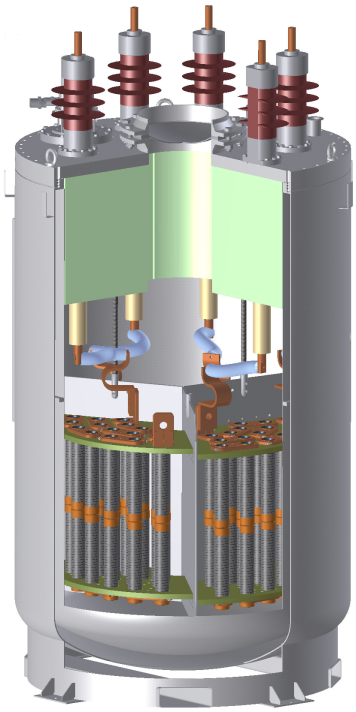


Figure 3.3: Example three-phase AC resistive SFCL device design [BBE+11]

3.2.2 Operation of Resistive SFCLs

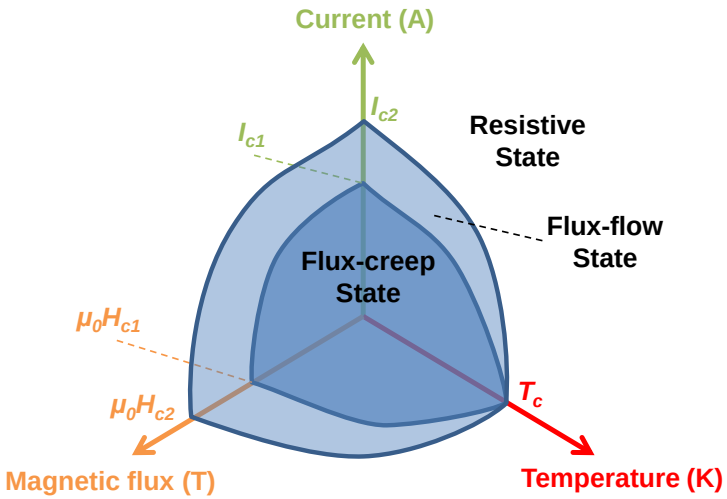


Figure 3.4: Conditions needed for superconductivity [PC98, BHH+11]

As depicted in Figure 3.4, superconductors remain in the superconducting state whilst three conditions are met:

1. The temperature is below the critical temperature, T_c.

2. The magnetic field, whether self-induced by current in the superconductor or externally applied, is below the critical magnetic field, H_c. This is due to the expulsion of flux from an externally applied field, a property of superconductors known as the Meissner effect, until the H_c threshold is reached [DH01, Sta02]. For Type-II superconductors, there are lower and upper values of H_c, as illustrated in Figure 3.4 [Cha03]. The intermediate region between H_{c1} and H_{c2} is known as the flux-flow state [PCL$^+$00] where magnetic flux vertices begin to form, but the material is still considered to be superconducting in this state. A magnetic field greater than H_{c2} will cause breakdown of superconductivity.

3. The current is below the critical current, I_c.

Items 2 and 3 relate to the same phenomena; the critical current is a consequence of the critical magnetic field [DH01] and accordingly there are two critical current thresholds, I_{c1} and I_{c2}. For a conductor with radius r carrying current I, the magnetic field at the surface of the conductor is:

$$H(r) = \frac{I}{2\pi r} \tag{3.1}$$

Therefore, the critical current is a function of the critical field value:

$$I_c = 2\pi r H_c \tag{3.2}$$

Hence, the critical current density, J_c, is:

$$J_c = \frac{2H_c}{r} \tag{3.3}$$

For simplicity and consistency, J_c is normally defined as the current density value where the electric field in the superconductor, E, is 1 µV/cm [Sta02].

These physical properties therefore allow superconductors to inherently limit fault currents in power systems. During non-fault conditions, the superconductors act as ideal conductors. During a short-circuit fault, the relatively high fault current causes the superconductor to transition to the intermediate flux-flow state. Typically, I^2R heating developed in the superconductor's flux-flow resistance causes T_c to be exceeded, resulting in a transition to the resistive state [PC98]. This increases the electrical impedance in the path of fault current, thereby reducing the fault current.

Figure 3.5 illustrates an example power system with an SFCL, where a three-phase to earth fault occurs at $t = 0.01$ s. The results are plotted in Figure 3.6. The SFCL model used for this simulation is described in Appendix A. The distorted current waveform at approximately 0.015 s illustrates that the fault current has been successfully limited from the prospective peak instantaneous value of 29.9 kA.

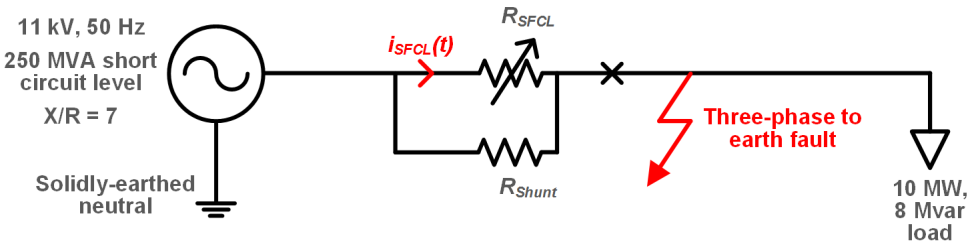


Figure 3.5: Single-line diagram with resistive SFCL

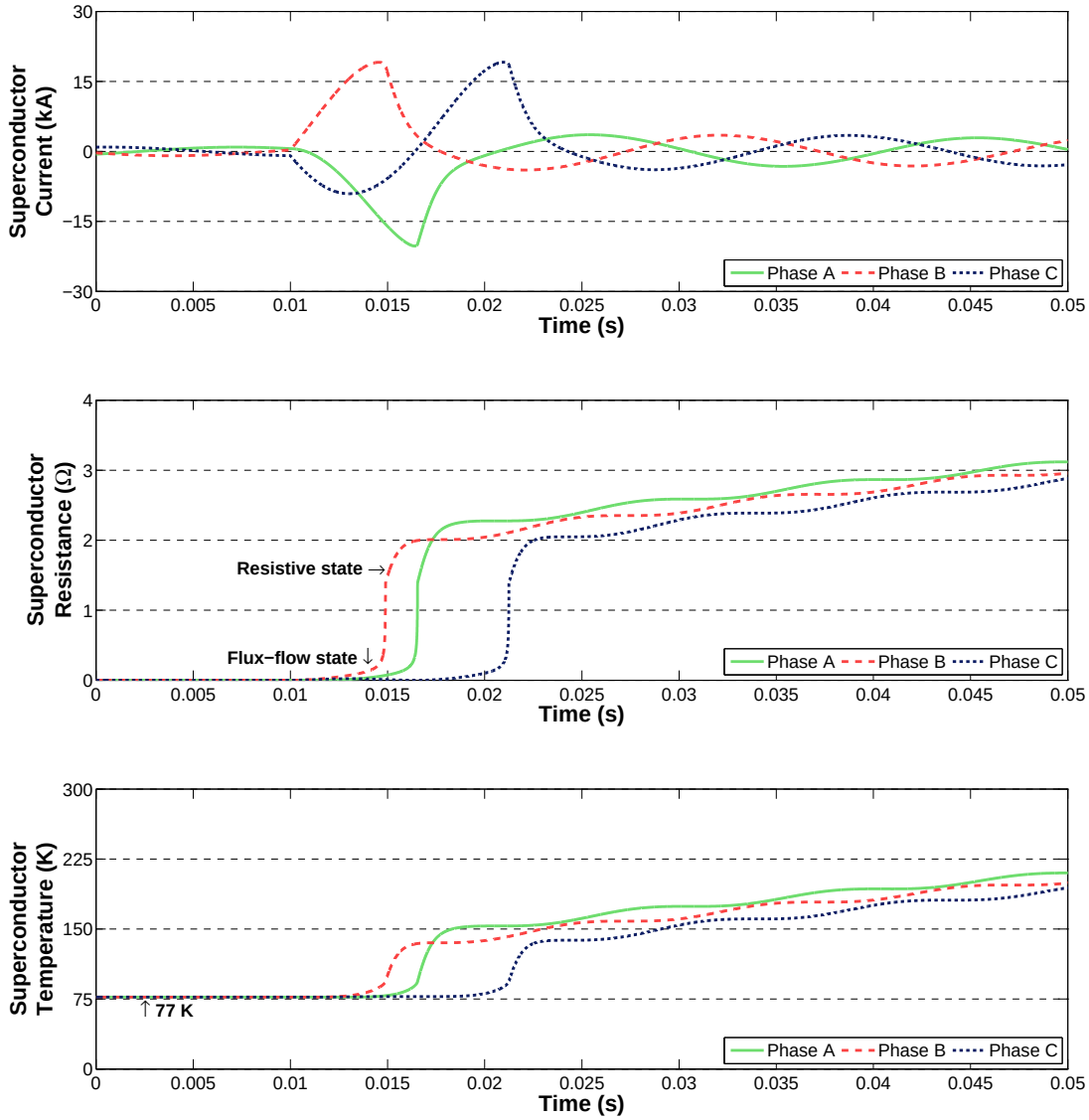


Figure 3.6: Resistive SFCL operation

3.2.2.1 Shunt Impedance

Resistive SFCLs typically have a shunt impedance that is connected electrically in parallel with the SFCL, as shown in Figure 3.5. This impedance may result from the resistivity of metal which is bonded to the superconductor during manufacturing to reduce hot-spots [NS07, DKH+10]. A resistance or inductance may be installed outside the cryogenic environment and connected in parallel with the superconductor to reduce the energy dissipated in the superconductor [SLSN09]. The shunt impedance is sometimes a combination of both bonded and external impedances [MBLR05]. A shunt resistance may also serve the purpose

of intentionally reducing the effective resistance of the SFCL, by diverting fault current through the shunt resistance when the SFCL becomes resistive, to ensure that enough fault current can be detected by existing designs of protection relays [DKH+10].

As noted in Chapter 5, there is a trade-off between the effective SFCL resistance (i.e., the parallel combination of superconductor and shunt, which dictates the level of fault current limitation) and the energy dissipated into the superconductor (which affects the superconductor temperature and the recovery time). In general, increasing the shunt resistance decreases the fault current, but increases the energy dissipated in the superconductor.

3.2.2.2 SFCL Inductance in Superconducting State

Although superconducting coils are typically wound to cancel-out inductance, some inductance remains [OSH+09] and this particularly relevant for AC applications of SFCLs. However, this inductive impedance has the important benefit of ensuring equal current sharing for multi-stranded superconducting wires. Otherwise, the current sharing would be dictated by the resistance of the joints connecting the superconductor strands and would lead to non-uniform currents in each strand. This may result in premature quenching of strands carrying a higher share of current [LL05].

3.2.3 Benefits of Resistive SFCLs

Resistive SFCLs offer the following benefits to power system operation:

- SFCLs can typically limit the first peak of fault current. An SFCL with suitably rated switchgear to interrupt fault current therefore acts much faster than a circuit breaker alone; without SFCLs, no remedial action occurs until a circuit breaker opens. This offers significantly reduced damage at the point of fault, and reduced damage or heating to any equipment carrying fault current [MK01, HB06]. Consequently, the presence of an SFCL can lead to improved overall reliability for other devices in distribution systems

[KK11], and particularly to reduced erosion in circuit breakers [MK01].

Another consequence of fast-acting fault current limitation, if multiple SFCLs are used in a network, is that the operation of one or more SFCLs will delay or block the operation of SFCLs further from the fault due to the reduced fault current; Chapter 7 examines this principle further.

- There is an opportunity to use switchgear of a lower fault current breaking capability, which is less expensive, smaller, and lighter. Alternatively, the use of fault current limitation in existing systems could delay, or even avoid, the replacement of existing switchgear, should fault levels rise due to system changes or the connection of DG [NS07].

- Increased opportunity for network interconnection. As noted in Chapter 2, this improves the security of supply, leads to lower network losses, and improves power quality due to the lower system impedance.

- Reduced voltage transients. Limiting fault current reduces the consequent voltage disturbances on the healthy parts of the system due to a fault [BBE+11, JNH+11]. Mitigating these disturbances can help both load and generation ride through the fault. In particular, fault current limitation has been shown to lead to improved transient stability of rotating machines connected to the power system [TMTK01, TI05, SPPK09a, ETS+10].

- Reduced circuit breaker transient recovery voltage (TRV). This topic is examined in detail in Appendix B. In general, resistive SFCLs will limit both the AC and DC components of fault current, and will dampen any transients (while in the resistive state). Inductive SFCLs, by comparison, will only limit the varying components of fault current, i.e., the level of limitation depends upon $\frac{di}{dt}$.

- Reduced system frequency transients during and following faults, which is especially important for the stability of relatively compact power systems such as marine vessels. This is examined in Section 4.2.4.3.

- SFCLs can be "reset" for multiple operations, unlike fuses. The recovery time for resistive SFCLs is substantially shorter than the time needed to replace a fuse in a distribution substation, and is certainly shorter than the time to repair the damage caused by a fault (such as replacing an underground cable). This avoids the cost and inconvenience of replacing fuses, as well as avoiding the extended outage of a circuit.

  For systems employing autoreclose schemes, there is an obvious concern that SFCLs may not be suitable due to their requirement to recover after operation; however, there is the possibility of using multiple superconducting elements to mitigate this, as discussed in Section 7.5.3.

- SFCLs provide intrinsic fault current limitation due to superconductors starting to quench when the current rises above a critical value. Therefore, a protection relay is not required to detect fault conditions and trigger the SFCL. Despite this, the lack of discrimination of the direction of power flow can be a disadvantage, particularly for the protection of systems with DG [Cof12].

3.2.4 Comparison of FCL Types

References [NS07, Eck08, Eck09] compare the main distinguishing features of each FCL type. This information is presented in Table 3.1. There are variations in the design of saturable-core FCLs [AKEA11]. For example, a "magnetic FCL" uses a permanent magnet to saturate the core instead of a superconducting DC winding; the losses are consequently greater.

3.2.5 Notable Trial Projects and Present Status

Several grid SFCL trials have been conducted over the past two decades [Eck08]. Figure 3.7 illustrates the main SFCL projects as of 2007, in terms of current rating and voltage level [Eck08].

Technology	**Losses**	**Triggering**	**Recovery**	**Size and weight**	**Distortion**	**Fail safe**
Resistive SFCL	AC losses (not an issue for DC use)	Passive	Superconductor must be re-cooled: several seconds [GRS+99] to several minutes [NS07]	Relatively small	During first cycle of current limitation	Yes
Hybrid resistive SFCL	AC losses (not an issue for DC use)	Passive or active	Faster than resistive SFCL due to reduced energy dissipation in superconductor	Can be smaller than resistive SFCL, but depends on sizes of additional components	During first cycle of current limitation	Yes
Saturable-core SFCL	DC power needed to saturate the iron core and heating in conventional conductors	Passive	Immediate	Large and heavy due to iron core and conventional windings	Some due to nonlinear magnetic characteristic	Yes
Shielded-core SFCL	AC losses (not an issue for DC use)	Passive	Superconductor must be re-cooled, but faster recovery than resistive SFCL	Large and heavy due to iron core and windings	During first cycle of current limitation	Yes
Fault current controller	Similar to resistive SFCL	Active	Immediate	Similar to resistive SFCL	Switching of power electronics introduces harmonics	No
Solid-state circuit breaker	Similar to resistive SFCL	Active	Immediate	Similar to resistive SFCL	Switching of power electronics introduces harmonics	No
Fuses	Negligible	Passive	Never; must be replaced	Smallest	None	Yes

Table 3.1: Comparison of FCL types

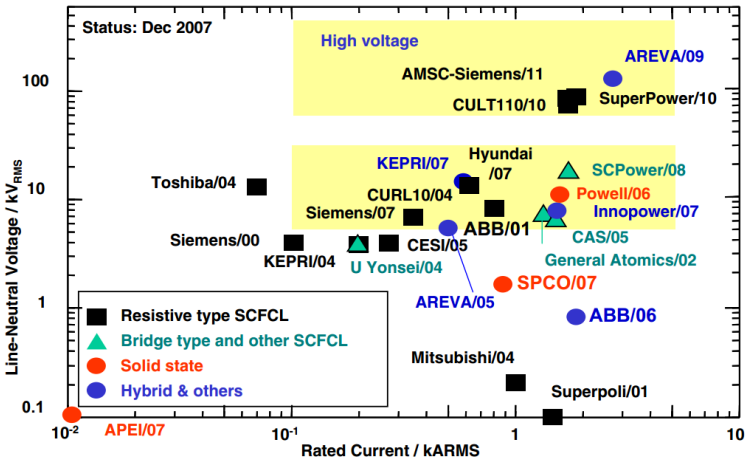


Figure 3.7: Overview of SFCL projects from [Eck08]

In 1996, ABB began testing a 1.2 MVA, three-phase shielded-core SFCL in a Swiss substation. The purpose was to test the endurance of the device, particularly the cooling system and superconductor material, after a year of operation—the first test of its kind. No faults occurred during this time. The superconductor did not degrade during the test, and the liquid nitrogen-based cooling system operated correctly. However, it was suggested that a refrigeration-based system, rather than an open system with large coolant storage, would require significantly less maintenance. The device operated normally at 77 K, with a superconductor critical current of 93 K. Its recovery time was between 2 and 10 seconds. A steel "bandage" around the superconductor provided an electrical bypass and mechanical strength [PC98].

ABB developed a single-phase resistive SFCL in 2001, rated at 8 kV, 6.4 MVA. No major SFCL developments have been announced by ABB since 2001 [Eck08].

In 2003, Siemens built and tested a three-phase, 7.2 kV, 1.23 MVA resistive SFCL. It was build with YBCO superconductor material. However, the project was abandoned due to the high cost of YBCO.

The Matrix FCL project involved SuperPower Inc., EPRI, the United States Department of Energy, and Nexans SuperConductors, with the aim of designing and building a 138 kV, 1.2 kA SFCL. A scaled single-phase prototype rated at 8.6 kV, 800 A was developed in 2004. However, no new results have been reported since 2005 [KYT+05]. SuperPower Inc. is presently pursuing 138 kV SFCLs

based on 2G HTS wires [LHD+11].

The CURL10 project was completed in 2004 after 4.5 years of research and development. It involved a three-phase resistive SFCL using BSCCO HTS and rated for 10 kV, 10 MVA, with a maximum short circuit current of 8.75 kA (for 5 ms). Tests in 2003 demonstrated that the device could almost halve the fault current between the 1st and 2nd cycles (from approximately 7.5 kA to 4 kA). It was installed in the German utility Rheinisch Westflische Energiewerke (RWE) network for one year, between April 2004 and March 2005. The device was installed at a bus-tie location. No fault current limiting operations of the device were required during this period. The CURL10 design was extended to use monofilar BSCCO-2212 coils, rather than the bifilar coils originally used, at 14.4 kV per-phase. This device was tested successfully in Korea in 2007. Nexans SuperConductors produced a 15 kV rated SFCL based on this prototype.

The CULT110 project aimed to produce a 110 kV SFCL. A normal conducting metal coil is connected electrically (but not thermally, unlike the CURL10) in parallel to protect the superconductor and to carry the majority of the fault current. The device offered good fault current limiting properties, but the manufacturing process is difficult to reproduce [Eck08]. Testing of the CULT110 device began in 2010.

In 2009, resistive SFCL devices were installed in the UK (rated for 100 A load current, and a peak fault current of 50 kA) and in Germany (rated for 800 A load current, and a peak fault current of 63 kA) [DKH+10].

Zenergy Power installed pre-saturated core SFCLs in a USA distribution system in 2009, with a 138 kV transmission system installation planned [MDD+11].

The Energy Technologies Institute (ETI) in the UK is presently supporting grid trials of both a pre-saturated core SFCL and a resistive SFCL [Ene13]. The pre-saturated core SFCL will be provided by GridON in Israel. The resistive SFCL will be build by Applied Superconductor Limited (ASL) in the UK, using MgB_2 superconductors. ASL also installed resistive SFCLs in the Electricity North West Limited distribution system in 2009 and the Scottish Power MANWEB distribution system in 2012.

Bruker Energy & Supercon Technologies, based in Germany, has recently developed a 10.6 kV, 1.25 kA shielded-core SFCL.

SFCL trials have also been undertaken, or are planned, in China, Japan, Korea, Italy, Sweden, Spain, and Slovakia [Neu07, CSL$^+$11, Int13].

Chapter 4

Challenges in the Adoption of Resistive SFCLs

4.1 Introduction

There are a number of technical issues which must be considered prior to the installation of a resistive SFCL device. Accordingly, this chapter analyses these issues, which include: location and resistance sizing of SFCLs; the potential effects of an SFCL on system voltage, power, and frequency during and after faults; the impact of SFCLs on protection systems; and practical application issues such as the potential impact of transients such as transformer inrush current.

This chapter reviews the relevant literature, and uses simulations based upon an actual marine vessel to help illustrate the main challenges in the adoption of resistive SFCLs. Many of the examples relate to both marine vessel and utility distribution systems.

4.2 Selection of SFCL Location and Resistance

For a given power system, there may be several options for the location and desired quenched resistance value of a resistive SFCL. This section compares the effect of various SFCL locations and resistance values for the marine vessel

introduced in Section 2.3.2.3. The vessel's electrical data are specified in reference [BBE+11]. Figure 4.1 illustrates four potential SFCL location strategies. These SFCL locations are analogous to those proposed for utility distribution systems [NS07, BSBB09].

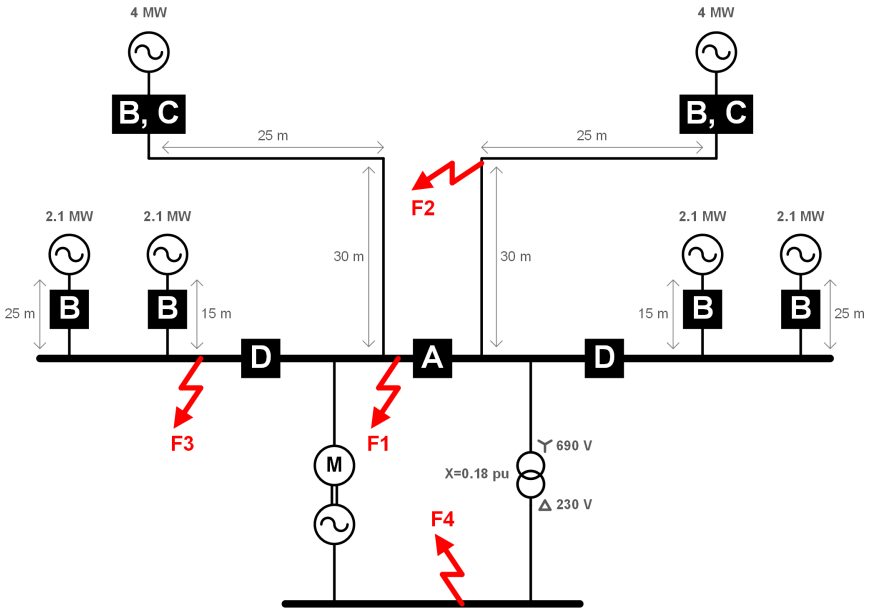


Figure 4.1: Fault locations, and possible SFCL locations (A, B, C, and D)

4.2.1 SFCL Model

The studies in this chapter use an "exponential" SFCL model, as described fully in Appendix A. The model provides a good estimate of the transient response of a three-phase SFCL, compared to empirical superconductor quenching results [Smi07], but with low computational requirements. The typical response of the model during a three-phase fault is illustrated in Figure 4.2.

4.2.2 Assessment of SFCL Location Strategies

Each SFCL location strategy has been tested with a quenched SFCL resistance of 0.2 Ω (chosen arbitrarily), for a fault at the 690 V bus-tie (fault F1). Table 4.1 compares the results and Figure 4.3 illustrates the total fault current (at the point of fault) for location strategy A, where the fault current is approximately halved in magnitude compared to the unrestricted case given in Figure 2.10. The

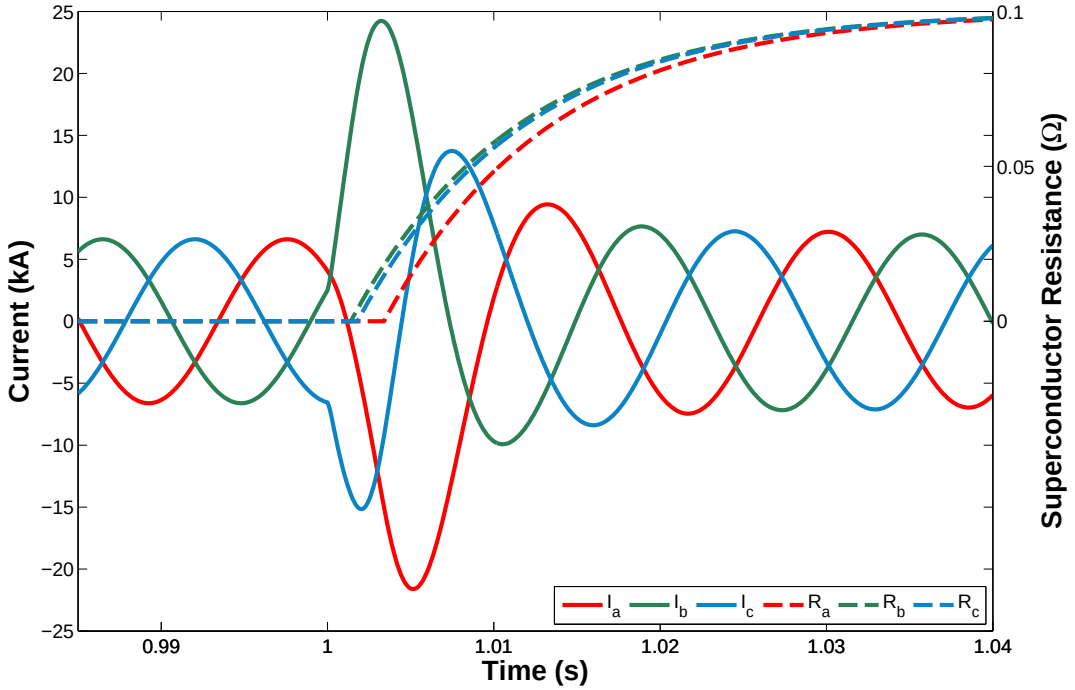


Figure 4.2: Typical per phase SFCL resistance characteristic and effect on fault current, for "exponential" SFCL model

SFCL location	**Peak fault current (kA)**	**RMS break fault current (kA)**
No SFCLs	232.4	66.02
A	120.1	34.4
B	97.8	18.8
C	175.1	44.5
D	93.6	31.9

Table 4.1: Comparison of impact of SFCL location on fault currents

"RMS break fault current" refers to the RMS fault current measured after three cycles following a fault. It is therefore representative, but not the exact value, of the steady-state, symmetrical fault current.

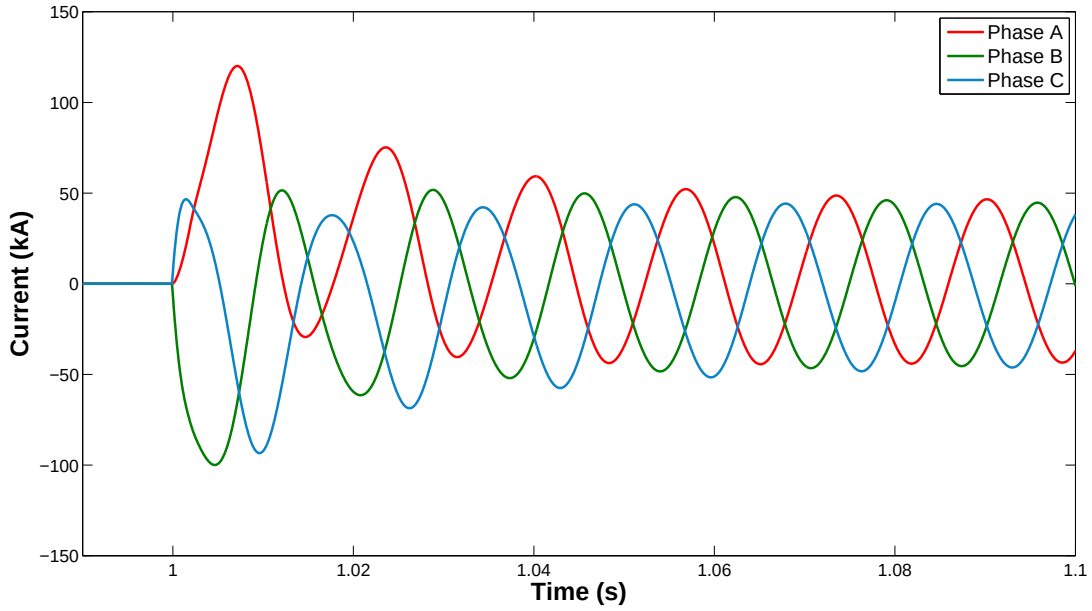


Figure 4.3: Fault current limitation for fault F1 at location A

It is important to note that even with one or more SFCLs, the peak fault current can still be very high (approximately 120 kA for SFCL location A) and this will stress the electrical system equipment, particularly the circuit breakers, during a fault; this is inherent in low voltage, power-dense systems. A further disadvantage of location A is that a single SFCL device is required to be rated to carry the current caused by the fault, and hence to absorb the energy dissipated in the superconductors during quenching.

Location strategy B limits the fault current contribution from all generators (except for faults across a generator's terminals), reducing the fault current to less than 30% of its prospective value. However, this is unlikely to be used in practice because the SFCLs may require post-fault recovery, necessitating all generation (except the emergency generator) to be removed from service. In addition, six separate fault current limiters are required, albeit of smaller current rating compared to location A.

Location strategy C is a compromise of the advantages and disadvantages of strategy B, and restricts the contribution only from the main 4 MW generators. The result in Table 4.1 for peak fault current for this SFCL location is rela-

tively high, because of the high peak fault current contribution from the 2.1 MW generators (due to their relatively small sub-transient reactance; see [BBE+11]).

Table 4.1 also illustrates that location D offers better fault current limitation than location A, and has the advantage that it can limit fault currents for all fault locations when the bus-tie circuit breakers are open.

4.2.3 Effects of Different SFCL Resistance Values

Figure 4.4 and Figure 4.5 illustrate how the quenched SFCL resistance affects the peak and RMS break fault current values, respectively. It can be observed that in most cases there is only a small reduction in fault current for resistance values greater than approximately 0.2 Ω because, at this value, only the generators supplying fault current which does not flow through the SFCL(s) contribute to the total fault current. A value of 0.2 Ω may appear to be very small, but this is a consequence of the low system impedance of compact power systems.

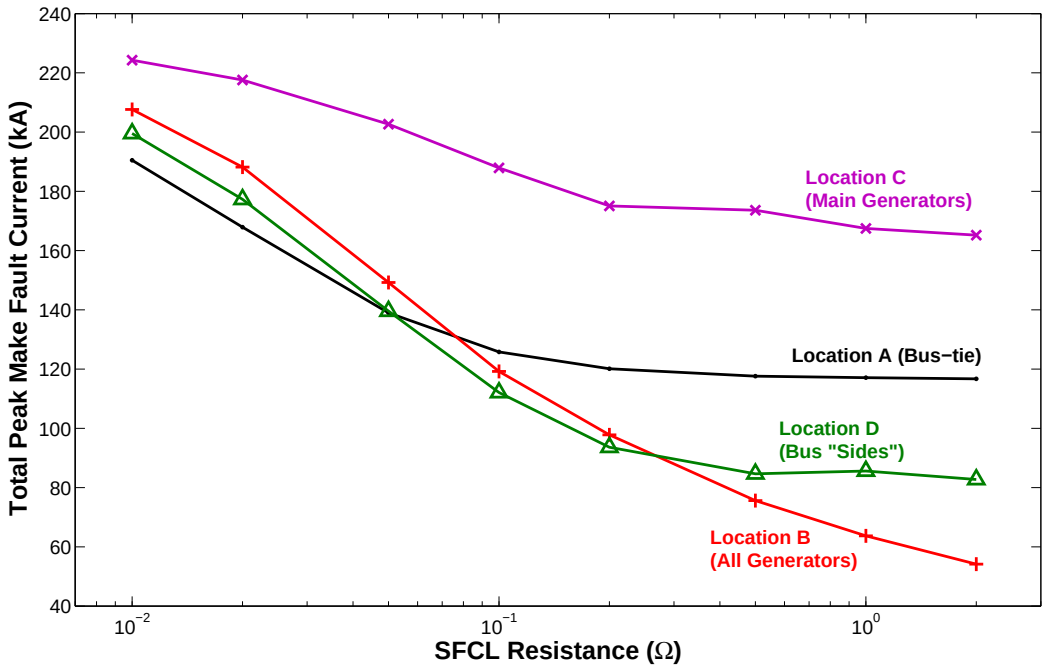


Figure 4.4: Total peak fault current for fault F1

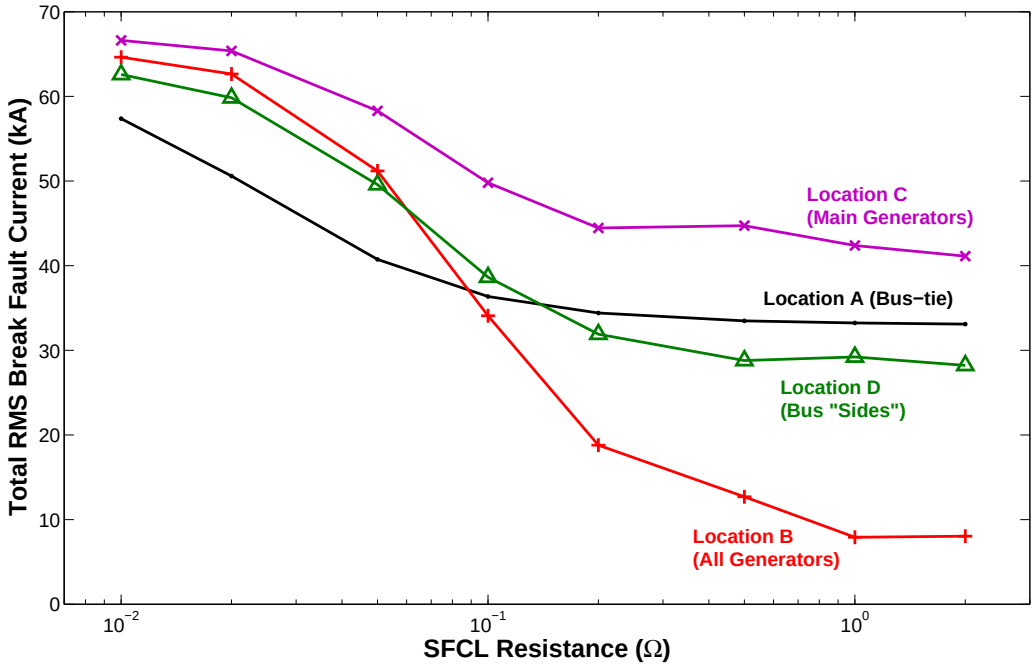


Figure 4.5: Total RMS break fault current for fault F1

For location B and with an SFCL resistance of greater than approximately 0.25 Ω, the peak fault current contribution from each generator is relatively small, and diminishes to load current levels after the first peak. Despite the disadvantages of location B due to the resistive SFCL recovery period, such severe fault current limitation could potentially lead to use of smaller, lighter, and less expensive switchgear.

The slight increase in the total fault current—for example, with location C at 0.5 Ω in Figure 4.4—is due to the fault current being limited sufficiently (below I_c) such that one phase of the SFCL does not quench. This implies that a two-phase SFCL may sufficiently reduce fault currents in unearthed electrical systems (noting that the voltage in the limited phases will rise by a factor of $\sqrt{3}$ of the nominal value), leading to further savings in size, weight, and cost [SSM+05]. Furthermore, only a certain range of SFCL resistance values will result in a two-phase quench in a three-phase SFCL, as discussed further in Sections 6.3.2 and 7.5.2.2.

By inspection, location D has the potential to limit approximately half of the

SFCL resistance (Ω)	**Peak fault current (kA)**	**RMS break fault current (kA)**
No SFCLs	141.8	53.0
0.02	129.5	50.7
0.1	108.0	38.9
0.2	98.9	34.7
0.5	92.9	32.8
1.0	93.8	32.9
2.0	91.9	32.3

Table 4.2: Comparison of limitation for SFCL location D, for fault F2

SFCL resistance (Ω)	**Peak fault current (kA)**	**RMS break fault current (kA)**
No SFCLs	232.3	66.0
0.02	118.7	35.1
0.1	81.8	21.4
0.2	78.4	20.2
0.5	76.9	19.6
1.0	77.1	19.7
2.0	76.5	19.5

Table 4.3: Comparison of limitation for SFCL location D, for fault F3

steady-state fault current for faults at the bus-tie. Figure 4.5 shows that an SFCL resistance of approximately 0.2 Ω is necessary to achieve this. In the case study system, a resistance of 0.2 Ω also reduces the peak fault current by more than half of the unrestricted value due to the relatively small sub-transient reactance of the 2.1 MW generators. However, this SFCL deployment strategy does not limit the fault contribution from either of the two 4 MW generators, for faults at the bus-tie or at one of the 4 MW generator feeders (fault F1 or F2). In the latter case, relatively large values of SFCL resistance only trim approximately one third off the fault current, as shown in Table 4.2. However, Table 4.3 illustrates that location D is highly effective at limiting faults elsewhere on the 690 V bus, such as for fault F3.

These results demonstrate that several factors must be considered before selecting an SFCL deployment strategy. In the context of a marine application, other factors must be accounted for, such as the the physical dimensions of the SFCL and its auxiliary equipment (i.e., the cryogenic system and its operational

requirements), and the corresponding naval architecture constraints of the vessel.

4.2.4 Impact of SFCLs on System Recovery

It is important to examine the effects that SFCLs have on system voltage, power, and frequency, and to help assess the nature of system recovery following a fault—and whether this recovery process is assisted by SFCLs. This is particularly important for compact power systems with relatively low inertia, such as marine vessels, aircraft, and microgrids.

For each scenario in this subsection, a bus fault (either F1 or F3) is applied to the vessel power system illustrated in Figure 4.1 at $t = 1$ s and the bus-tie circuit breaker is opened after approximately 100 ms (depending on the individual phase current zero-crossings). This clears the fault from the right subsystem. The left subsystem must open further circuit breakers, at each of its three generator feeders, to clear the fault but this is not considered further.

4.2.4.1 SFCL Location A

For SFCL location A, the voltage dip and power perturbations are reduced considerably for the operational (right) subsystem, as shown in Figure 4.6 and Figure 4.7c, respectively[1]. The voltage waveform is calculated using the equation in [BBE+11]. Note that for an SFCL resistance of 0.1 Ω the voltage initially collapses until the SFCL reaches an appreciable resistance value, and that the subsequent overvoltage (to approximately 1.05 pu of the nominal value) is due to the action of the generator exciter under certain large values of apparent "overload". Hence, for compact electrical systems such as marine vessels, it is important to investigate the generators' dynamic response to the relatively unusual scenarios presented by SFCLs, as discussed further in Section 4.3. The transient overvoltage experienced for an SFCL resistance of 1 Ω is due to the imbalance caused by

[1]Before the bus-tie circuit breaker opens, the SFCL can simply be thought of as a (serially-connected) resistive load of the appropriate power rating (i.e., $P = V^2/R = 690^2/1.0 = 476$ kW, for an SFCL resistance of 1 Ω). This explains the transient increase real power delivered by the generator, as illustrated in Figure 4.7b for an SFCL resistance of 1 Ω. The real power delivered drops sharply, from approximately 5.8 MW to 4.8 MW, while the SFCL develops resistance.

the individual SFCL phases quenching at different times following the fault occurrence; the 690 V bus voltage returns to the nominal value after approximately 10 ms.

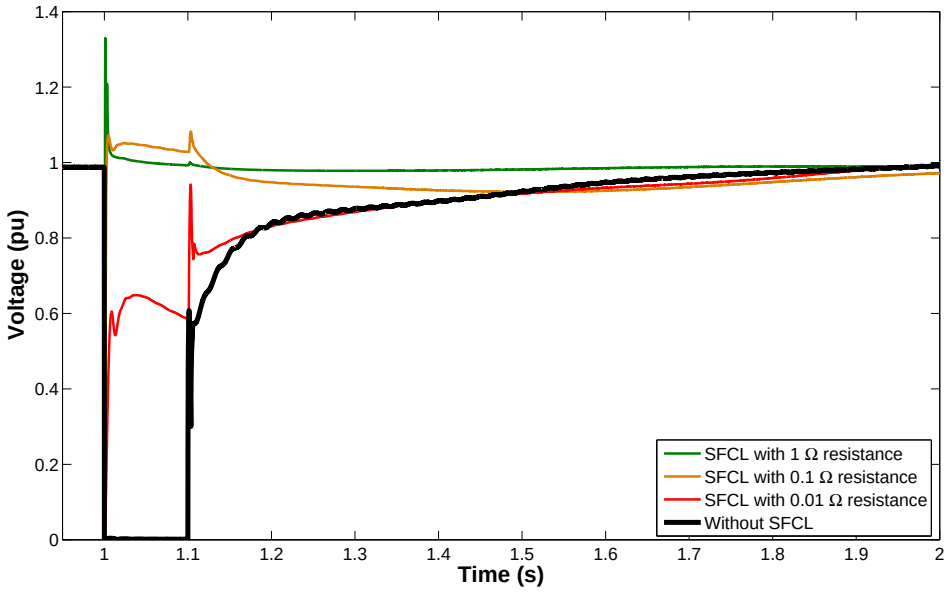


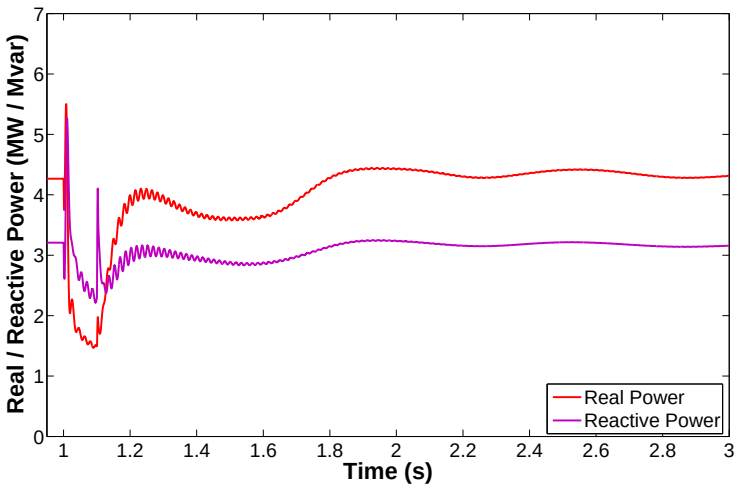
Figure 4.6: 690 V bus voltage for SFCL location A, for fault F1 (or F3)

4.2.4.2 SFCL Location D

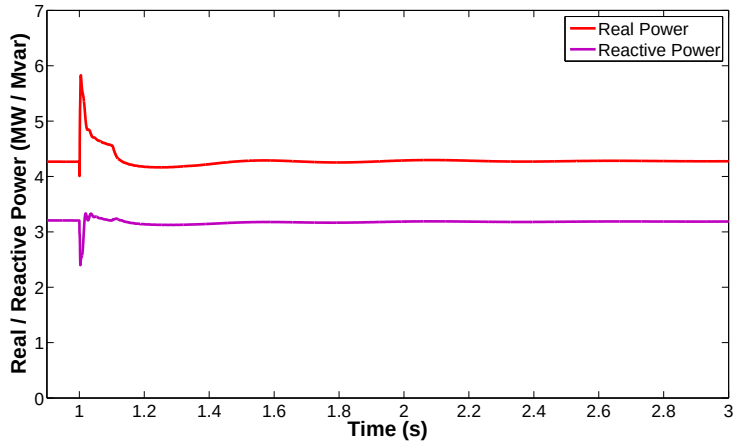
For SFCL location D, the bus-tie circuit breaker opens 100 ms after the fault and the SFCL in the right subsystem is bypassed (such that the SFCL is not in the path of load current during recovery) after a further 100 ms. This emulates a possible control action which would be necessary for the right subsystem to recover from faults F1 or F3. Figure 4.7 compares the impact of location strategies A and D and highlights that, for fault F3 (and also for F1, but this is omitted for brevity), location A is better suited for reducing the perturbations to power.

Similarly, location D results in greater disturbances to the 690 V bus voltage than location A, as is evident through comparison of Figure 4.6 and Figure 4.8[2]. Note that the voltage is measured at (the right of) the bus-tie point, but higher voltages (approximately $\sqrt{3}$ times the nominal value) can be experienced

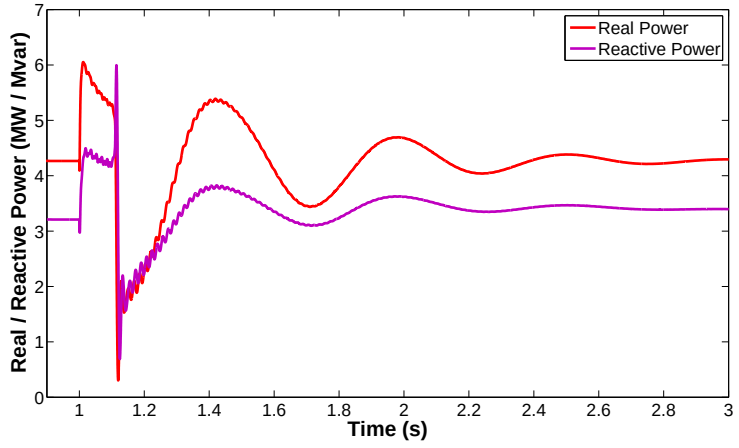
[2]The oscillations in the calculated RMS voltage for an SFCL resistance of 1 Ω during fault F3 are due to imbalance in the voltage because phase A in each of the SFCLs does not quench.



(a) No SFCL

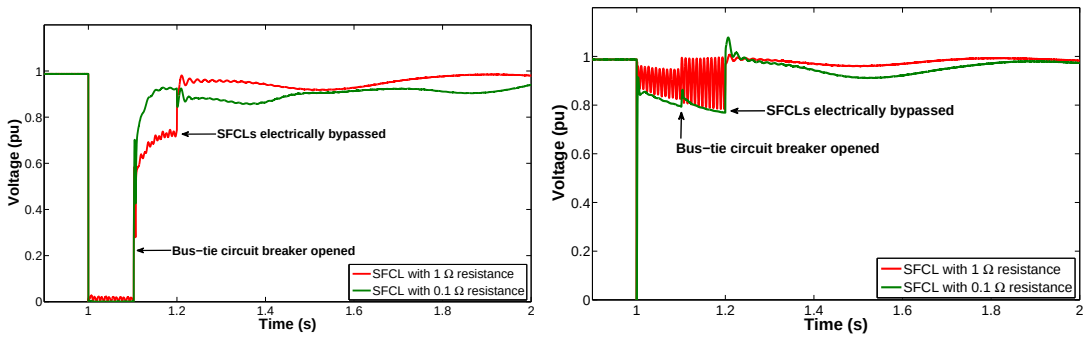


(b) SFCL location A



(c) SFCL location D

Figure 4.7: Instantaneous real and reactive power delivered by 4 MW generator in the right subsystem for fault F3, with SFCL resistance of 1 Ω



(a) Fault F1 (b) Fault F3

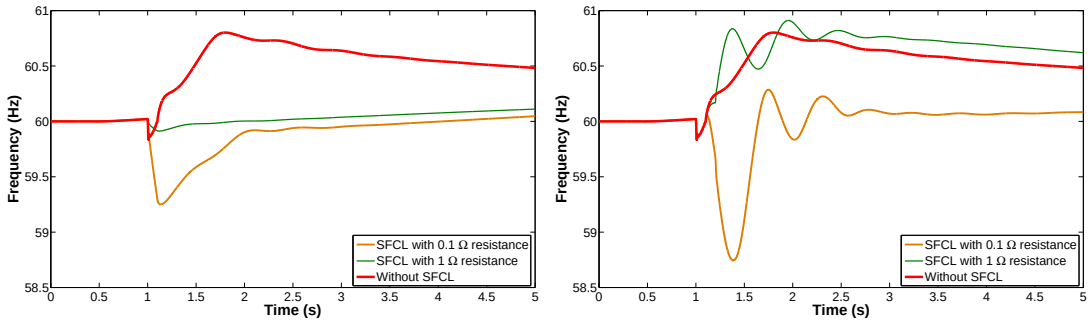
Figure 4.8: 690 V bus voltage for SFCL location D, for faults F1 and F3

elsewhere on the 690 V bus.

4.2.4.3 System Frequency

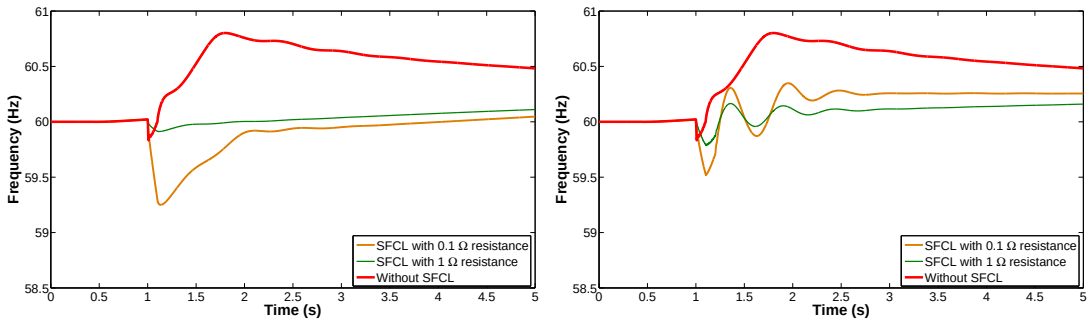
Figure 4.9 and Figure 4.10 illustrate the frequency of the power system during faults F1 and F3, respectively. With the SFCL present at location A, the generators "slow down" during the fault due to the apparent overload. It can be seen that SFCL location A, with a relatively large resistance value, is effective at reducing both the magnitude of the transient frequency deviation and the time to recover to nominal frequency after the fault is cleared. Hence the risk that generators' under-frequency protection systems would trip is also significantly reduced. Location D is relatively ineffective at reducing the frequency disturbance, especially for fault F1; this is because the fault contribution from the 4 MW generators is fed directly into the fault without limitation. The damping provided by larger values of SFCL resistance will be increasingly important for generators with lower inertia values and particularly for generation interfaced by power electronic converters.

It can be concluded that although small values of SFCL resistance such as 0.1 Ω can significantly reduce the peak and RMS break fault current values, larger values are desirable to reduce perturbations in voltage, power, and frequency. Although location D can offer greater fault current limitation than location A, it is far less attractive in terms of the effect on system stability, both during and after a fault. Accordingly, for the application of SFCLs at any location, it is



(a) SFCL location A (b) SFCL location D

Figure 4.9: System frequency for Fault F1



(a) SFCL location A (b) SFCL location D

Figure 4.10: System frequency for Fault F3

necessary to examine the dynamic effects on the electrical system.

4.3 Implications for Control Systems

The use of SFCLs in compact marine networks has the potential to create unusual, complex interactions with generator exciter and governor control systems. It has been shown in Section 4.2.4 that the presence of SFCLs can cause unusual system frequency deviations during and following faults in compact electrical systems. Further work is needed to fully understand these relationships and to assess the implications that the presence of fault current limitation may have on the design of generator and power electronic converter control systems.

4.4 Post-Fault Recovery Time

When a superconductor in a resistive SFCL quenches during a fault, its temperature is raised above the critical temperature threshold (T_c) due to the energy dissipated during the fault. To re-enter the superconducting state, a cryogenic system must cool the superconductor below the critical temperature. This recovery period may take up to several minutes [NS07]. This is a significant problem because the SFCL is inoperable during this period; the SFCL, and potentially part of the downstream network, must be disconnected. Note that this applies to resistive SFCLs; some varieties of SFCL, such as the pre-saturated core and diode-bridge devices, inherently do not require recovery.

The authors of [SYMM02, SMYM05] propose a solution using the flux-flow state exhibited by Type-II superconductors. If the fault current exceeds the critical current, but the temperature remains below the critical temperature, the superconductor presents a small resistance. Therefore, an SFCL can limit currents during abnormally-high current flow, but can return to normal operation immediately after the fault is cleared; no recovery period is necessary. However, a relatively large, and expensive, volume of superconductor (and the associated cooling system) is needed, and the AC losses will be greater. Reference [SYMM02]

estimates the volume of superconductor required for a given fault current reduction performance for a resistive SFCL to provide this behaviour. This type of device fits into the "constant temperature" classification of SFCL suggested by [PC98]. The same operating principle is also proposed in [DOP+09]. This will require careful design of the I_c parameter and energy dissipation for each situation. However, the authors do not mention issues regarding multiple faults, or faults that are not cleared quickly. The temperature may exceed T_c, thus forcing a recovery period.

The potential for a resistive SFCL to recover while carrying load current is demonstrated in [LHW09], using 2G HTS material. The recovery period is significantly longer in this configuration due to the additional I^2R heating in the superconductor during recovery.

Another solution is to install two SFCLs in parallel. The second SFCL is switched into the circuit whilst the first SFCL recovers following a quench [PC98]. Assuming the switching can occur fast enough, the fault level is not compromised during the recovery period.

For an SFCL located at a bus-tie, reference [YC06a] notes that it is acceptable to remove the SFCL during recovery. A recovery time of 60 seconds is deemed acceptable for bus-tie SFCLs [HHJ+04].

4.5 Effects of SFCLs on Protection

4.5.1 Standardisation Work

FCLs add a non-linear impedance into the system which could negatively affect protection relays or their measurement devices [Ada06]. In a survey, utilities in the USA rated protection changes as an important issue, but considered the issue of rising fault levels to be more important [Eck04]. In 2003, CIGRÉ Working Group (WG) A3.10 [Sch03] suggested four impacts of SFCLs on protection:

1. Protection relay settings may need to change, depending on the relay location: incoming feeder, outgoing feeder, or customer-side.

2. Change in selectivity (time coordination between overcurrent relays).

3. Protection blinding, particularly in the case of directional protection.

4. Compatibility with downstream fuses.

CIGRÉ WG A3.16 [Sch08] followed on from the work of WG A3.10, and produced guidelines for the impact of FCLs on protection systems. A framework was proposed, which builds on the typical FCL characteristics established by WG A3.10, and provides a comprehensive study of the impact of SFCLs on the protection scheme [Eck08]. The framework correlates specific FCL characteristics with typical protection methods (overcurrent, distance, directional, and differential). The process, which can be applied to any FCL type, outputs a report of the severity of each potential impact on protection, based on rules and heuristics. A crucial aspect is whether the FCL lies inside or outside the zone of the protection relay. For example, a bus-tie FCL may have little impact on the distance protection for a fault in an outgoing feeder zone. However, if the FCL is installed on the outgoing feeder, the impedance measured by a distance may be outside the pickup threshold, causing delay or failure of the operation of distance protection. The CIGRÉ WG A3.16 Technical Brochure does not cover situations involving multiple FCLs locations, FCL failure, or autoreclose schemes.

4.5.2 Overcurrent Protection

The impact of an SFCL on an overcurrent relay is described in [LSPO08]. As one would expect, the authors propose that a SFCL would delay overcurrent relay tripping, for a given relay current-time characteristic, because the fault current measured by the relay is reduced. The authors also demonstrate that the coordination time between upstream and downstream relays (which will have different current-time characteristics, or grading margins [Als11]) would also increase. This can be beneficial because there is more time to trip the downstream circuit breaker before the upstream relay trips.

Reference [TI05] suggests that FCLs can help overcome the overcurrent protection issues when DG is added to a traditional radial power system. The issues,

as described in Section 2.3.1.1, include: relays must be direction-sensitive due to the potential for bi-directional current flow; DG may reduce the reach of relays; and DG may disturb the coordination between relays. The authors suggest that a FCL that could be operated only if the fault current was in a certain direction—hence only limiting the DG contribution—will involve very little change in existing protection settings. However, it is concluded that SFCLs (and other passive FCLs) are not suitable because they automatically operate for fault currents in either direction.

Reference [UGGT+01] proposes that a bus-tie SFCL application requires relatively few protection changes. The authors also suggest that a careful choice of superconductor quench characteristics could mean that, during a fault on one side of the bus-tie, the healthy side could continue to supply customers. Hence the fault is not "seen" by the healthy part of the system. In addition, the SFCL should not quench when a source is disconnected and the remaining source(s) must supply all loads, because this may significantly increase the load current through the bus-tie. The paper also notes that mal-operation of a SFCL in the bus-tie location as the result of excessive voltage harmonics, while possible, is very unlikely. However, problems may arise if tap changers are used, as any voltage difference on each side of the busbar will cause current to flow through the SFCL, potentially causing a mal-operation. The authors propose a switchable bypass circuit could be used to mitigate these issues, to electrically bypass the SFCL. These results are supported in [LSW+05, YC06a, LSPO08].

Reference [UGGT+01] also compares SFCL shunt types (without a shunt; fully resistive; and fully inductive). A resistive shunt is the most effective at reducing the transient overvoltage across the SFCL during a quench; the inductive shunt is moderately effective. However, a resistive shunt reduces the ability of the SFCL to limit the first peak of fault current; no change is shown for an inductive shunt. For both resistive and inductive shunts, the next current zero-crossing point is delayed, particularly for the inductive shunt. This may lead to larger overall I^2R loses compared to a SFCL without a shunt, but can be beneficial because it may be feasible for protection to isolate the fault within first cycle of fault current.

4.5.3 Marine Vessel Protection

As described in Chapter 2, high fault levels are an emerging issue in marine power systems. The use of fault current limitation may merit a complete redesign of the protection system, because conventional overcurrent relays may not operate for significantly reduced fault current due to the presence of SFCLs, or relays may operate spuriously for non-fault transient currents. Unit protection may mitigate these issues. Reference [BES+08] proposes that faults could be located and cleared, using a fault indicator from the SFCL and "current flow detectors" at several positions throughout the system. This is a centralised protection scheme which is particularly applicable for networks with SFCLs, but which requires communications.

Furthermore, thorough investigation of the operational implications of SFCL deployment, such as the role of SFCLs during supply restoration [BSWD98, GHS08], is required.

4.5.4 Distance Protection

Reference [LSW+05] demonstrates the effects of an SFCL on distance protection. A real-time power system simulator has been used to model a simple network with a resistive SFCL, which was interfaced to a hardware distance relay. The relay failed to correctly calculate the fault distance when the SFCL is placed immediately downstream of the relay measurement location, and did not trip at all when the fault was sufficiently further downstream from the relay, because the SFCL increases the apparent impedance during a fault.

This can potentially be mitigated by measuring the SFCL impedance, by measurement of the voltage across (which can itself be used to indicate the operation of the SFCL) and the current through each phase of the SFCL. The distance relay can then compensate for the instantaneous impedance increase due to the SFCL; however, communications is needed. This is alluded to in [HBS03], but for a solid state FCL which inserts a fixed resistance during a fault. The authors of [HBS03] note that this arrangement improves the response of the distance relay.

4.5.5 SFCLs with Autoreclose

In some cases, resistive SFCLs may interfere with autoreclose schemes, because the autoreclose dead-time is typically much shorter than the recovery period for resistive SFCLs [KM04]. Ideally, SFCLs should have zero impedance before a circuit breaker is reclosed [MBC+03]. The application of an FCL device can prevent the loss of coordination between DG and existing autoreclose systems [ZES10].

4.5.6 Other Protection Issues

Reference [LSPO08] notes that the ability of SFCLs to operate before the first peak of fault current could force upstream circuit breakers to trip (to disconnect the SFCL) for faults downstream of the SFCL location, which would normally be isolated by downstream circuit breakers. This could lead to unnecessary disruption to supply.

Although resistive SFCLs are considered "fail-safe", failure of an SFCL's cooling system could introduce an unexpected impedance into the system which, apart from causing undesirable losses, could trip undervoltage protection [SB07].

The presence of an FCL at the grid connection point of a microgrid can improve protection coordination, because the same overcurrent protection settings can be used in both grid-connected and islanded modes of operation [NZW13].

The requirement for SFCL recovery time and the "automatic" nature of the operation of resistive SFCLs are also pertinent for DG connections, because DG is often required to provide "ride-through" for remote network faults [BRB+10].

4.6 SFCL Mal-Operation Due to Non-fault Transients

Typical system transients, such as transformer inrush and motor starts, have the potential to cause mal-operation of SFCLs and other protection devices. Protection relays can block protection operation during transformer inrush, by detecting

the relatively high level of second harmonic in the current waveform during the phenomenon, as shown in Figure 4.11; resistive SFCLs cannot restrain their operation.

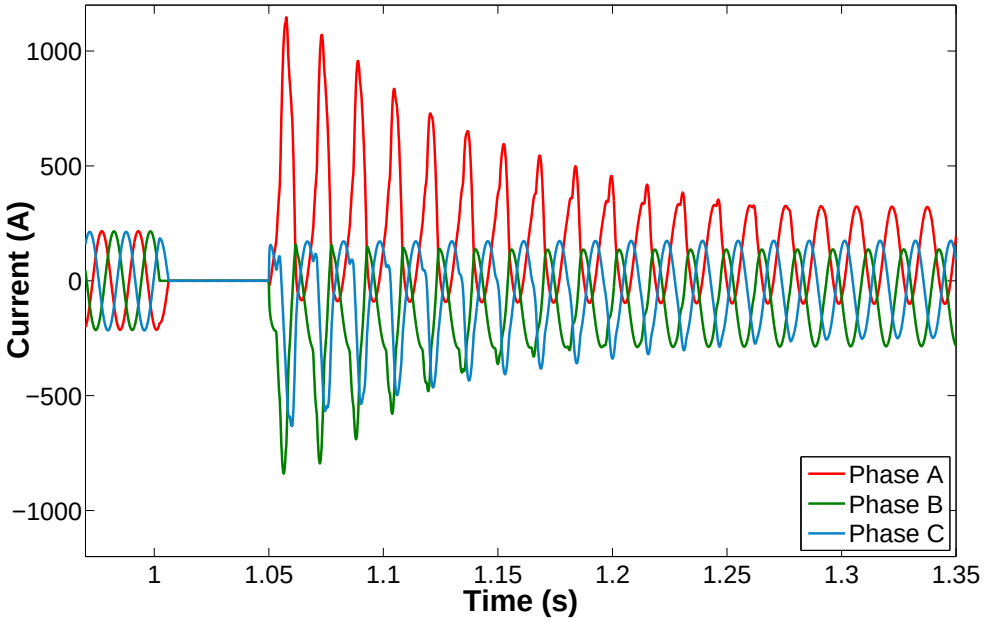


Figure 4.11: Transformer inrush current for 350 kVA marine transformer

Large motor loads are often converter-interfaced (such as for the vessel studied in Section 4.2) or use soft-start circuitry [Sch] to minimise the current transients.

However, for power systems where multiple transformers may be energised simultaneously, or where larger transformers are used, inrush studies must be carried out—for each SFCL location strategy—and the potential for SFCL maloperation must be established. The SFCL critical current rating must always be selected with careful reference to transformer inrush currents [DKH+10]. For larger transformers, inrush could be significant and might impinge on fault current levels (and therefore on SFCL operation thresholds), particularly in situations where prospective faults levels are reduced due to only partial generation being in service.

SFCLs have also been proposed for deliberately limiting transformer inrush current, and reference [SKR+10a] provides guidance on the appropriate SFCL resistance selection.

4.7 Summary

This chapter has demonstrated several issues pertaining to the use of resistive SFCLs in marine vessel and utility distribution systems:

- It has been shown that SFCLs, even with relatively small impedances, are highly effective at reducing prospective fault currents in marine vessels, yet there are trade-offs relating to the location and resistance sizing of the SFCLs. The impact that higher resistance values have on fault current reduction and maintaining the system voltage for other non-faulted elements of the system is also presented and it is shown that higher resistance values are desirable in many cases. It has been demonstrated that the exact nature of the SFCL application will depend significantly on the vessel's electrical topology, the fault current contribution of each of the generators, and the properties of the SFCL device, such as size, weight, critical current value, and recovery time.

- The recovery period associated with resistive SFCLs leads to several operational complications, including: the SFCL must be isolated from the system soon after quenching; resistive SFCL may not be suitable for use with autoreclose schemes; and transformer inrush and other transients must be considered when installing an SFCL, to avoid operation of the SFCL under these non-fault conditions.

- SFCLs have been shown to affect, and even prevent, the operation of overcurrent and distance protection relays. Consequently, differential protection—which requires costly low-latency communications—may be needed to protect power systems with one or more SFCLs, under all scenarios.

- SFCL energy dissipation must be carefully analysed to minimise the recovery period and, if required by the design of the SFCL, to ensure that superconductors remain in the flux-flow state during faults to provide instant recovery.

Chapter 5

Analysis of the Trade-Offs in Resistive SFCL Design

5.1 Introduction

This chapter describes factors that govern the selection of an appropriate resistive SFCL design.

Ideally, the resistance of an SFCL should be chosen to limit the fault current as much as possible. Not only does this benefit the electrical system through reduction in the potentially damaging effects of high fault currents, the primary purpose of an SFCL, but a higher level of fault current limitation has the consequence of shortening the recovery time of the SFCL by reducing the energy dissipated in the superconductors [DYF+08]. The SFCL recovery time affects the design, planning, and operation of electrical systems using SFCLs to manage fault levels. Furthermore, excessive heat dissipation may damage the SFCL and cause undue vaporisation of the coolant [TPL+91].

Nevertheless, fault current limitation is subject to a compromise because a significantly-limited fault current requires a high resistance SFCL and therefore a relatively greater quantity of superconducting material, which increases capital costs. Also, electrical protection elsewhere in the system requires a sufficient level of fault current in order to operate correctly through the ability to distinguish

between faults and highly loaded situations [DKH+10].

Section 5.2 examines the relationship between SFCL resistance, voltage level, and energy dissipation using simulations. The results are analytically verified in Section 5.3, which establishes a generalised equation for SFCL energy dissipation, in terms of: the duration of the fault, SFCL resistance, source impedance, source voltage, and fault inception angle. Single- and three-phase analyses are presented.

Furthermore, the volume of superconductor used in the SFCL must be sufficient to absorb the prospective energy dissipation [DYF+08]. Another requirement is that the dimensions of the superconductor must ensure that the SFCL discriminates between fault current, for which it must operate, and load current, for which it must not operate. An SFCL should not operate in response to transients such as transformer magnetic inrush. All of these considerations are included in a method for estimating the minimum volume of superconductor required. This method is independent of the type of superconducting material itself, and is described in Section 5.4.

5.2 Selection of SFCL Resistance by Simulation

5.2.1 Resistive SFCL model

To simplify the analysis, a binary SFCL model is used: the SFCL has zero impedance before fault inception, but is assumed to reach its full resistance immediately when the fault occurs. This will yield a reasonably accurate estimation of the reduction of steady-state RMS fault current (as defined in [IEC01]), but will overestimate the reduction of the peak fault current; hence the following sections only comment on the effect an SFCL has on reducing the steady-state fault current. Although this model does not account for the development of SFCL resistance during a quench, tests with a more realistic SFCL model (see Section 5.4.1) have shown that the results in this chapter only differ by approximately 6%.

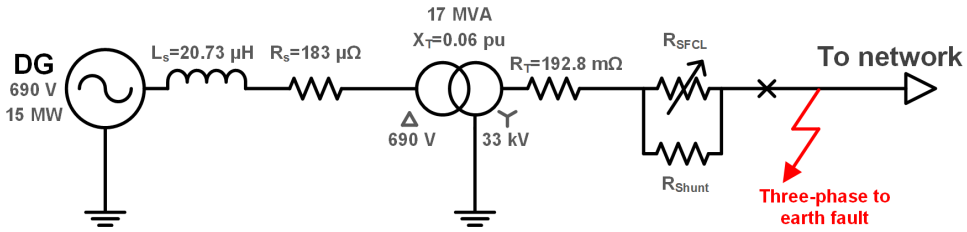


Figure 5.1: DG branch with source impedance, transformer impedance, and an SFCL

5.2.2 Comparison of SFCL Energy Dissipation at Different Voltage Levels

Figure 5.1 illustrates a representative DG connection to an existing power system. It is assumed that the fault level at the point of connection in the power system is already near the breaking capability of existing switchgear. An SFCL may be effective at several locations in the power system [NS07, BSBB09], but this chapter concentrates on a DG application in which the DG is the source of the fault level increase. Therefore, only one modification to the electrical network is required, that is, the installation of an SFCL in series with the DG, rather than installation of a number of SFCLs at different locations. Nevertheless, the analysis is relevant to SFCLs at any location. A three-phase to earth fault with negligible resistance is applied at the point where the DG is connected to the existing network.

The power system has been simulated in PSCAD [Man13], using impedance data from [SP-03] such that the X/R ratios—which are important for a fault study—are indicative of a typical UK distribution system. The unrestricted steady-state fault current contribution from the DG, i.e., without an SFCL, is approximately 1 kA RMS (at 33 kV). Initially, the shunt impedance, R_{shunt}, is ignored; this is explored in Section 5.3.3. The total energy, Q, dissipated in each phase of the SFCL during the fault is calculated in the simulation using Equation 5.1, where t_0 is the time of fault occurrence (0.0 s) and t_f is the time the fault is cleared ($t_f \approx$0.1 s, depending on the current zero-crossing required for the circuit breaker to interrupt fault current).

$$Q = \int_{t_0}^{t_f} i_{SFCL}(t)^2 R_{SFCL}\, dt \tag{5.1}$$

Figure 5.2 illustrates the level of fault current reduction and the corresponding total energy dissipation in one phase of the SFCL for the fault indicated in Figure 5.1. For the parameters used in the simulation, the following regions have been identified:

1. $R_{SFCL} < 12\ \Omega$: the steady-state fault current is slightly reduced, reaching a magnitude of approximately 3.4 times load current, but the corresponding energy dissipation rises steeply as shown in Figure 5.2.

2. $12\ \Omega < R_{SFCL} < 24\ \Omega$: the fault current reduces with increasing SFCL resistance, but the increasing resistance causes the energy dissipation to reach its maximum in this region. This large energy dissipation would lengthen the recovery time and so this range of SFCL resistances should be avoided. This result is in accordance with the maximum power transfer theorem [NR04]. The equivalent 33 kV Thevenin source has an impedance of 18.7 Ω (as derived from Figure 5.1), so maximum energy dissipation in the SFCL occurs when its resistance equals the source impedance value.

3. $R_{SFCL} > 24\ \Omega$: fault current continues to decrease with increasing SFCL resistance (almost linearly with resistance, as shown in Figure 5.2), but the energy dissipation reduces. This is the most desirable region: relatively low fault current combined with low energy dissipation. It can be observed from Figure 5.2 that an SFCL value of approximately 70 Ω reduces the steady-state fault current to the same value as the maximum load current.

If the SFCL had been located at the 690 V side of the DG transformer instead of at 33 kV then, for a given energy dissipation value, the resistance values obey the relationship $R_{SFCL_{33\text{ kV}}} \approx R_{SFCL_{0.69\text{ kV}}} (33\text{ kV}/0.69\text{ kV})^2$. Therefore, far smaller resistance values are required for equivalent levels of fault current limitation at 690 V; however the current-carrying capability of the SFCL must be increased by a factor of (33 kV/0.69 kV).

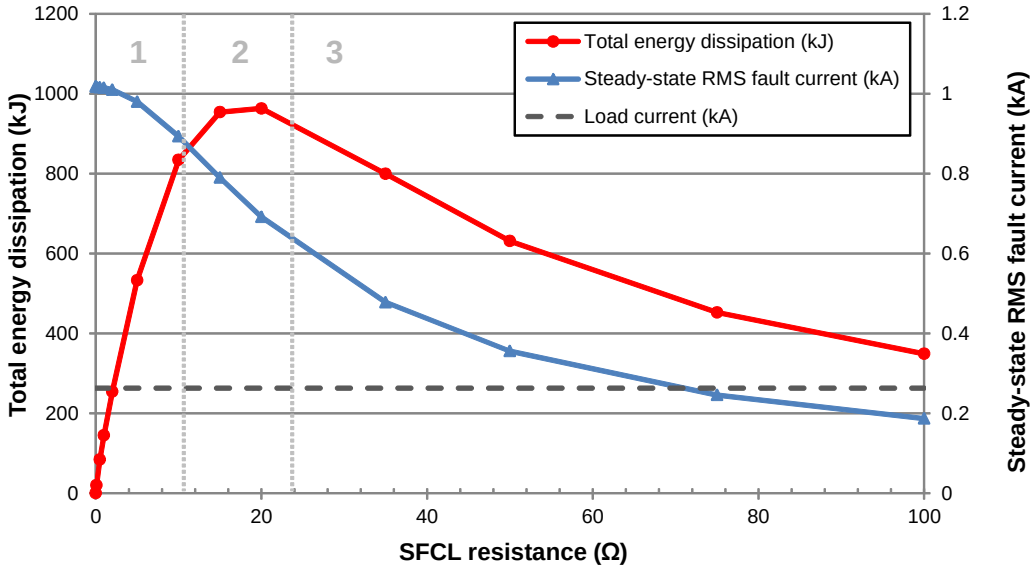


Figure 5.2: Energy dissipation and fault current limitation for various SFCL resistance values (at 33 kV side of DG transformer)

At either voltage level, the energy dissipation is approximately the same for a given level of fault current reduction relative to load current. Assuming an SFCL device is available at both voltage levels, there is a tradeoff between the quenched-state resistance of the superconductor and the current it must be rated to carry; this is explored further in Section 5.4. Although either SFCL would limit fault current, an SFCL at 690 V with a load rating of 15 MVA would be required to have a full load current rating of over 12 kA per phase which would present serious difficulties in design. By contrast, a 33 kV SFCL would have a full load current rating of 250 A and would be easier to design, despite the higher voltage rating. However, operation at lower voltages leads to higher AC losses in the superconductor when in the superconducting state [Tix94].

5.3 Analysis of Optimal SFCL Resistance Values

5.3.1 Analytical Derivation of SFCL Energy Dissipation

The SFCL resistance value for the maximum energy dissipation in the SFCL, as described in Section 5.2, can be analytically verified. At the 33 kV side of the interfacing transformer in Figure 5.1, the equivalent phase source impedance, Z_{source}, is:

$$\begin{aligned} Z_{source} &= R_{source} + jX_{source} \\ &= R_s \left(\frac{33\ kV}{0.69\ kV}\right)^2 + R_T \\ &\quad + j\left(L_s\,\omega \left(\frac{33\ kV}{0.69\ kV}\right)^2 + X_T \frac{33\ kV^2}{17\ MVA}\right) \\ &= 0.6114 + j18.74\ \Omega \end{aligned}$$

The circuit is characterised by the differential equation [STB+10, Duf03]:

$$\hat{V}\sin(\omega t + \alpha) = i(t)R + L\frac{di(t)}{dt} \tag{5.2}$$

where $\hat{V} = 33\ kV \times \sqrt{2}/\sqrt{3}$, $R = R_{source} + R_{SFCL}$, and L is the inductive component of Z_{source}. The solution for the short-circuit current, including both the symmetrical and asymmetrical components, can be stated as [PDdMN05, Als11]:

$$i(t) = \frac{\hat{V}}{Z}\left[\sin(\omega t + \alpha - \phi) - \sin(\alpha - \phi)\, e^{\frac{-Rt}{L}}\right] \tag{5.3}$$

where $Z = \sqrt{R^2 + L^2\omega^2}$, α is the point on the voltage waveform of fault occurrence, and $\phi = \tan^{-1}(\omega L/R)$. The total energy dissipated in one phase of the SFCL during the fault, Q, is calculated using Equation 5.1. Substituting Equation 5.3 into Equation 5.1 gives:

$$Q = \int_{t_0}^{t_f} \frac{\hat{V}^2 R_{SFCL}}{Z^2} \left[\sin(\omega t + \alpha - \phi) - \sin(\alpha - \phi)\, e^{\frac{-Rt}{L}}\right]^2 dt \qquad (5.4)$$

Equation 5.4 can be numerically evaluated as shown in Figure 5.3 for $R_{SFCL} = 5.0\ \Omega$, where the sum of the instantaneous power dissipation values multiplied by the time interval equals 520.5 kJ. A generic algebraic solution to the integral can be stated as shown below, when substituting $t_0 = 0.0$ and t_f:

$$\begin{aligned} Q = {} & \frac{\hat{V}^2 R_{SFCL}}{R^2 + \omega^2 L^2} \left[\left(\frac{L e^{\frac{-Rt_f}{L}}}{R^2 + \omega^2 L^2} \right) \right. \\ & (L\omega (\sin(\omega t_f + 2(\alpha - \phi)) - \sin(\omega t_f)) \\ & + R(\cos(\omega t_f) - \cos(\omega t_f + 2(\alpha - \phi)))) \\ & + \frac{L}{R^2 + \omega^2 L^2} (R\cos(2(\alpha - \phi)) - R - L\omega \sin(2(\alpha - \phi))) \\ & + \frac{L\left[\cos(2(\alpha - \phi)) - 1\right]}{4R} \left(e^{\frac{-2Rt_f}{L}} - 1\right) \\ & \left. + \frac{t_f}{2} + \frac{\sin(2(\omega t_f + \alpha - \phi)) + \sin(2(\alpha - \phi))}{4\omega} \right] \end{aligned} \qquad (5.5)$$

Hence, substituting $R = (R_{source} + R_{SFCL})$ into Equation 5.5 gives the value for the total energy dissipated in one phase of the SFCL, as a function of the SFCL resistance; all other parameters are constant. The root of the partial derivative of Q (i.e., where $\frac{dQ}{dR_{SFCL}} = 0$) determines the value of R_{SFCL} resulting in maximum energy dissipation in the SFCL, $\hat{Q}$; for $\alpha = 0$, this value is approximately 18.2 Ω, as illustrated in Figure 5.4. This differs from the magnitude of the source impedance (18.7 Ω) because the circuit is reactive and the maximum power transfer analogy is not strictly valid. Furthermore, α affects both the magnitude of the (decaying) DC offset in the fault current and the phase of the sinusoidal component; hence α has a somewhat complicated effect on the area under the fault current waveform, and the value of R_{SFCL} resulting in $\hat{Q}$ consequently varies between approximately 18.1 Ω and 18.9 Ω as α is varied.

The equivalent peak resistance value for an SFCL located at the 690 V side of

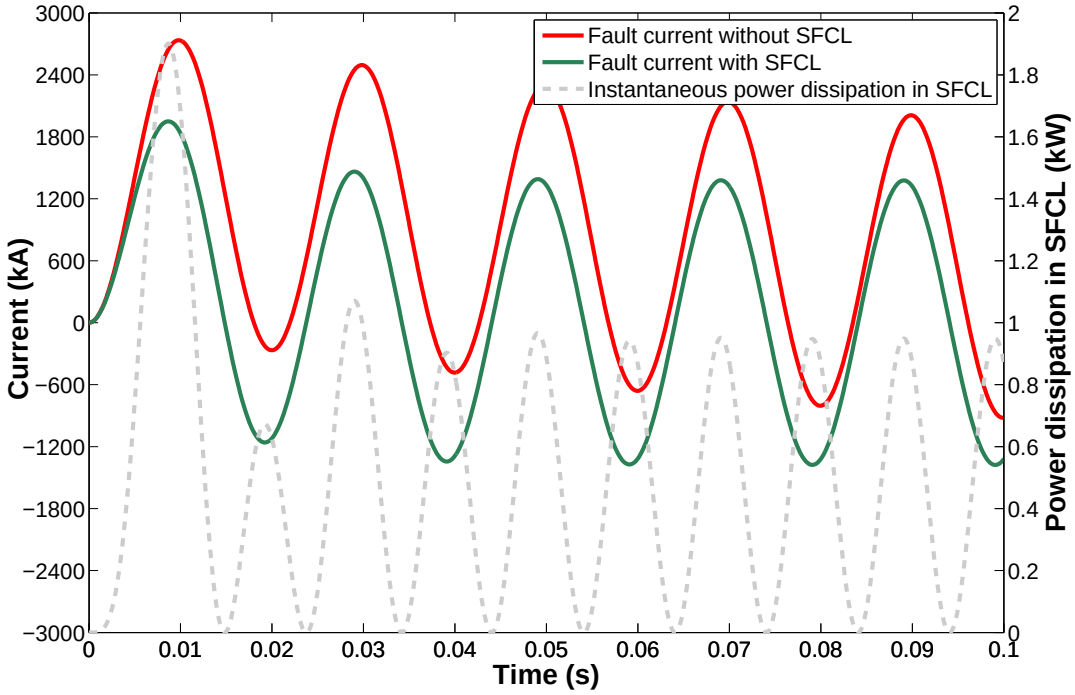


Figure 5.3: Numerical solution of power dissipation, where $R_{SFCL} = 5.0\ \Omega$

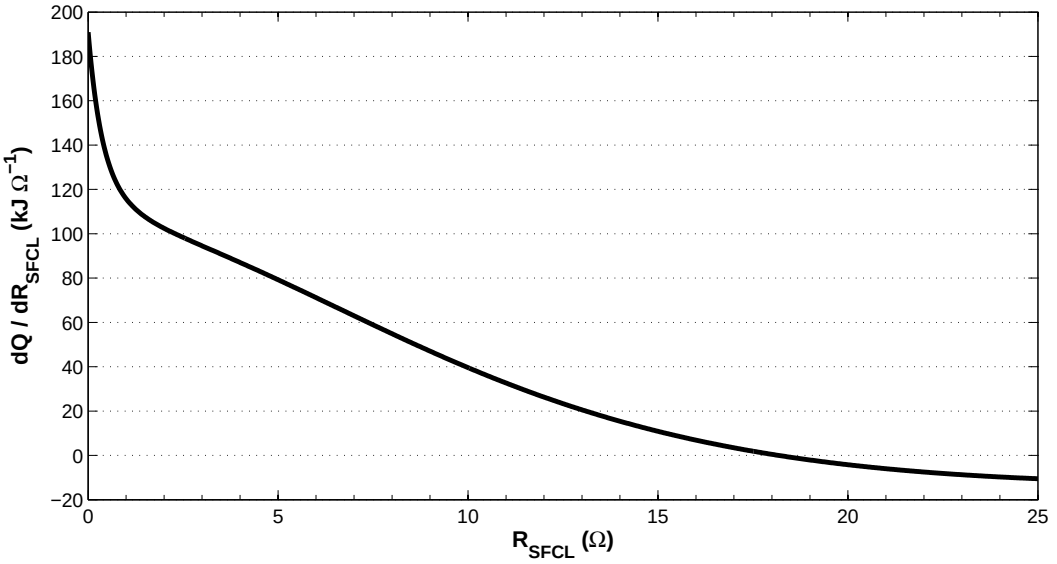


Figure 5.4: Derivative of Q with respect to R_{SFCL}, showing a root at $\sim$18.2 Ω

the DG transformer is approximately 0.00794 Ω. This is in good agreement with the simulation results in Section 5.2; the calculated values for energy dissipation differ by less than 2% from the simulation values. A small error is expected due to the delay associated with a circuit breaker interrupting fault current at a zero-crossing point, which is modelled in the simulation; in the analytical approach, the fault current is interrupted at a specified time regardless of the fault current value.

5.3.2 Effect of Fault Inception Angle

Considering Equation 5.4, if the asymmetrical component of the fault current is ignored (i.e., where $\alpha = \phi$), the equation for the total per-phase energy dissipation can be approximated as shown in Equation 5.6.

$$\begin{aligned} Q &= \int_{t_0}^{t_f} \frac{\hat{V}^2 R_{SFCL}}{Z^2} \sin^2(\omega t) dt \\ &= \frac{\hat{V}^2 R_{SFCL}}{Z^2} \left[\frac{t_f}{2} - \frac{\sin(2\omega t_f)}{4\omega} \right] \end{aligned} \tag{5.6}$$

Therefore the partial derivative of Q, with respect to R_{SFCL}, is Equation 5.7; a root of Equation 5.7 occurs when Equation 5.8 is satisfied.

$$\frac{dQ}{dR_{SFCL}} = \frac{\hat{V}^2}{Z^2} \left[\frac{t_f}{2} - \frac{\sin(2\omega t_f)}{4\omega} \right] \left[1 - \frac{2R_{SFCL}R}{Z^2} \right] \tag{5.7}$$

$$\frac{2R_{SFCL}R}{Z^2} = 1 \tag{5.8}$$

Hence, with the approximation that $\alpha = \phi$, the energy dissipation is maximised when the SFCL resistance equals the source impedance magnitude, as shown in Equation 5.9; as before, this is analogous to the maximum power transfer theorem [NR04]. Therefore, to reduce the fault current and the energy dissipation in an SFCL, the optimal SFCL resistance value is any value that is substantially

larger than the magnitude of the source impedance.

$$R_{SFCL} = \sqrt{{R_{source}}^2 + L^2\omega^2} = |Z_{source}| \tag{5.9}$$

The accuracy of this approximation is evaluated by considering the total energy dissipation in all three phases; the sum of the results of calculating Equation 5.5 for each phase is compared with the value calculated using Equation 5.10 (three times the value of Equation 5.6). Figure 5.5 illustrates that there is only a small difference in the total energy dissipation; the approximation provides an accurate representation of the average energy dissipation per phase. Furthermore, Figure 5.5 shows that the energy dissipation varies approximately linearly with fault duration, which implies that faster acting protection is desirable to minimise the energy dissipation in the SFCL. This requirement may need to be taken into account for the integration of SFCLs with time-graded protection schemes in distribution systems, which can have relatively long trip times—in excess of one second.

$$\begin{aligned} Q_{three-phase} &\approx \frac{3\hat{V}^2 R_{SFCL}}{Z^2}\left[\frac{t_f}{2} - \frac{\sin(2\omega t_f)}{4\omega}\right] \\ &\approx \frac{{V_{rms}}^2 R_{SFCL}}{Z^2}\left[t_f - \frac{\sin(2\omega t_f)}{2\omega}\right] \end{aligned} \tag{5.10}$$

5.3.3 SFCL with Resistive Shunt

As noted in Section 3.2.2.1, resistive SFCLs typically have a shunt resistance either bonded to the superconductor or external to the SFCL. It is assumed that the bonded shunt type will provide very similar energy dissipation in the SFCL as for an SFCL without a shunt (as described in Sections 5.2 and 5.3) because the total heat energy to be dissipated within the cryogenic chamber is the same. Equation 5.5 can be modified to examine the effect of an external shunt resistance by replacing $R = R_{source} + R_{SFCL}$ with:

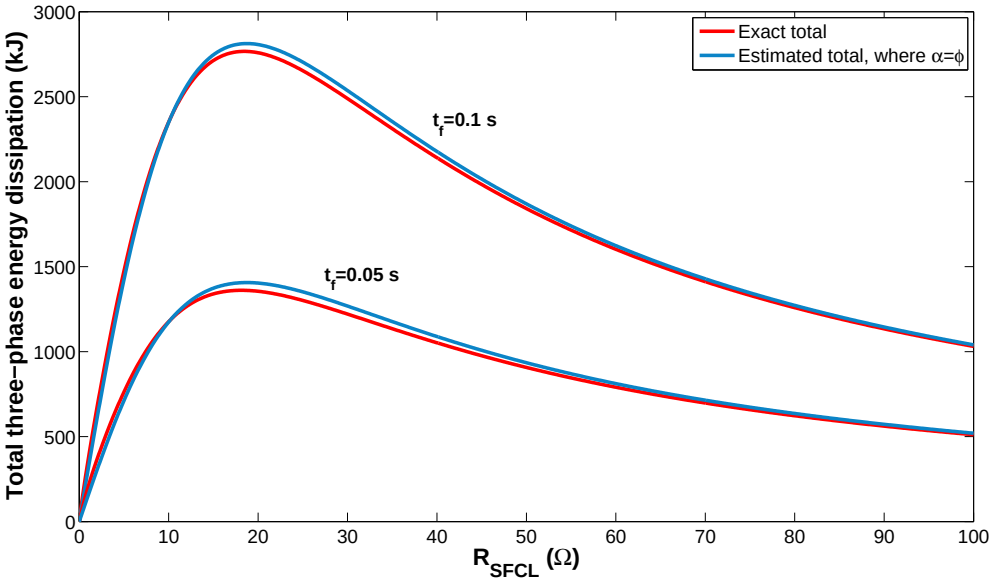


Figure 5.5: Total three-phase energy dissipation: exact vs. approximation

$$R = R_{source} + \frac{1}{\frac{1}{R_{SFCL}} + \frac{1}{R_{shunt}}}$$

and by recognising that the current in the SFCL branch is:

$$i_{SFCL}(t) = i_{total}(t)\frac{R_{shunt}}{R_{SFCL} + R_{shunt}}$$

The four-dimensional plot in Figure 5.6 illustrates the relationship between R_{SFCL}, R_{shunt}, Q, and the level of fault current limitation (in red/green). The green regions offer the best reduction in steady-state fault current. A shunt with a small resistance, relative to the SFCL resistance, can significantly reduce the energy dissipation in the SFCL—and hence reduce the recovery time—but only at the expense of a higher fault current value. The shunt would therefore carry the majority of the fault current, and would have to be designed accordingly, but this is considered feasible. The analytical results were confirmed by simulation.

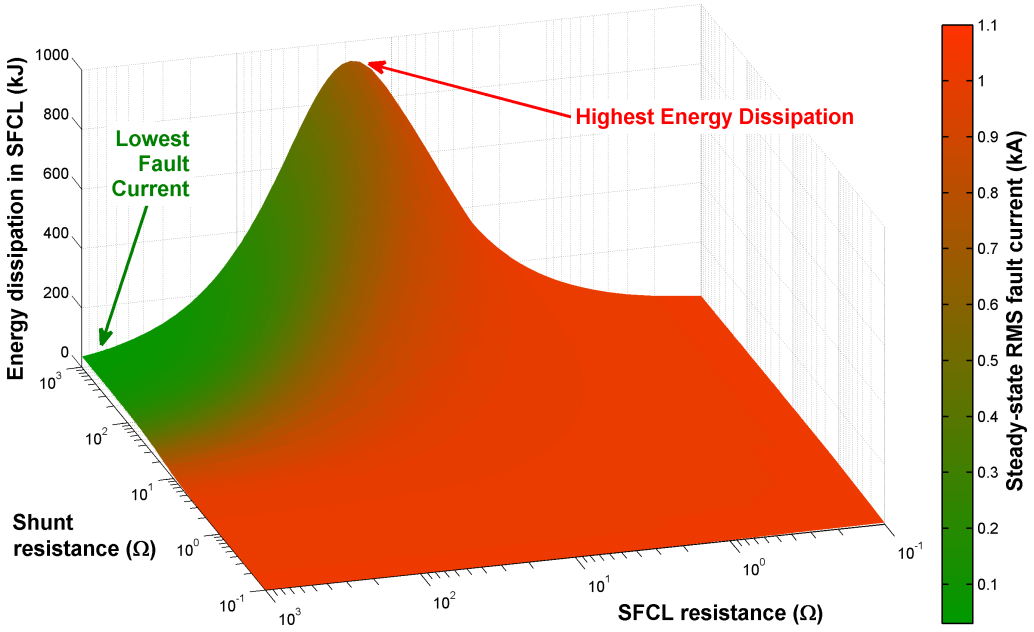


Figure 5.6: Variation of SFCL energy dissipation and current limitation (in red/green), with a resistive shunt

5.3.4 Case Study

Sharifi and Heydari [SH09] establish a multi-objective optimisation method for designing the parameters of a resistive SFCL. While this method will converge on an optimal resistive SFCL design, the work in this chapter explains why this answer is suitable. For example, for the power system parameters used in [SH09], and summarised in Table 5.1, a four-dimensional plot can be drawn, as given by Figure 5.7. As indicated in Figure 5.7, the optimisation process in [SH09] has converged on an SFCL design which results in relatively low energy dissipation in the superconductor, and which also significantly reduces fault currents. Although the shunt resistance value determined by this method is relatively large, it can be seen from Figure 5.7 that any value greater than approximately 10 Ω may be acceptable. Hence, the work presented in this chapter can be used to validate the design of a resistive SFCL.

Parameter	Symbol	Value
System frequency	f	50 Hz
Source resistance	R_s	1 Ω
Source inductance	L_s	0.01 H
Source reactance	X_s	3.14 Ω
Source impedance magnitude	Z_{mag}	$\sqrt{{R_s}^2 + {X_s}^2} = 3.297$ Ω
Phase voltage	V	$20000/\sqrt{3} = 11.55$ kV
Maximum fault current (steady-state, RMS)	I_f	$V/Z_{mag} = 3.50$ kA

Table 5.1: Power system parameters from multi-objective optimisation in [SH09]

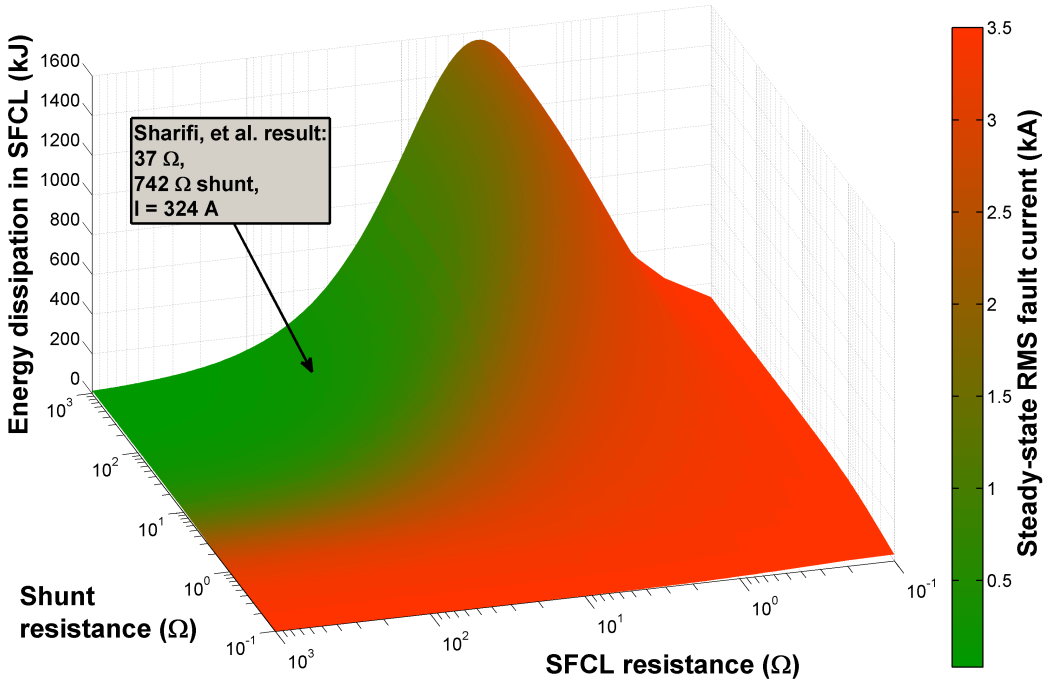


Figure 5.7: Visualisation of results from work in [SH09]

5.4 Relationship of SFCL Energy Dissipation to Minimum Volume of Superconductor Required

An SFCL must be able to absorb the prospective energy dissipation during a fault without failure, i.e., without the superconductor exceeding a thermal limit. Consider a notional superconducting wire, or "unit", with a quenched resistance of R_{unit} Ω and an RMS current carrying capability of I_{unit} A (per phase). It is assumed that the current rating is based on the prospective temperature of the wire and the permissible time for which the temperature can be experienced, as dictated by $I_{unit} = \sqrt{(dT_{unit} C_v Volume_{unit}) / (R_{unit} t_f)}$, where dT_{unit} is the temperature change and C_v is the volumetric specific heat capacity of the superconductor. This assumes an adiabatic process (where no heat is dissipated out of the superconductor) but an alternative, non-adiabatic equation is derived in [DYF+08]. The required resistance rating of an SFCL can be obtained by connecting individual superconductor units in series; the current rating can be increased by connecting units in parallel, equivalent to increasing the cross-sectional area of the wire and thereby reducing the total resistance. Hence, the minimum number of superconductor units required per phase—a material-independent indication of the total superconductor volume—can be calculated using Equation 5.12. Note that $I_{limited}$ depends upon R_{SFCL}.

$$
\begin{aligned}
total\ units &= units_{parallel} \times units_{series} \\
&= \left(\frac{I_{limited}}{I_{unit}}\right)\left(\frac{R_{SFCL} units_{parallel}}{R_{unit}}\right) \\
&= \left(\frac{I_{limited}}{I_{unit}}\right)\left(\frac{R_{SFCL} I_{limited}}{R_{unit} I_{unit}}\right) \\
&= {units_{parallel}}^2 \left(\frac{R_{SFCL}}{R_{unit}}\right) \qquad (5.11) \\
&= \frac{{I_{limited}}^2 R_{SFCL}}{{I_{unit}}^2 R_{unit}} \qquad (5.12) \\
&= \frac{total\ power\ dissipation}{unit\ power\ dissipation}
\end{aligned}
$$

Equation 5.12 implies that the minimum volume of superconductor required is proportional to the total power dissipation. This suggests that it is significantly more efficient, in terms of superconducting material, to limit the fault current as much as possible, as described in [SYG+03]. This is, of course, advantageous from the point of view of the electrical system because a lower fault current reduces the fault current interruption duty imposed on switchgear, and also reduces the fault current carrying requirements of other equipment in the fault current paths. Higher SFCL resistances may also limit the voltage depression "upstream" of the SFCL from the fault and therefore reduce the upstream impact on other loads, and the potential for consequential and unwanted voltage-based protection during a disturbance.

However, to avoid spurious operation of the SFCL, the superconductor units must be arranged such that the effective critical current, I_c, of the SFCL is greater than load current, I_{load}, and the contribution from non-fault transients [DKH+10, BRB+10]. Equation 5.13 states the minimum I_c for the required headroom factor of λ.

$$
I_c \geq \lambda I_{load} \qquad (5.13)
$$

If $I_{c_{unit}}$ is the critical current of one unit, I_c can be calculated using Equation

5.14:

$$I_c = units_{parallel} \times I_{c_{unit}} \tag{5.14}$$

Equation 5.15 can be obtained by substituting Equation 5.14 into Equation 5.13:

$$\begin{aligned} units_{parallel} \times I_{c_{unit}} &\geq \lambda I_{load} \\ units_{parallel} &\geq \frac{\lambda I_{load}}{I_{c_{unit}}} \end{aligned} \tag{5.15}$$

Substituting Equation 5.15 into Equation 5.11 provides a more realistic estimate than Equation 5.12 for the minimum number of superconductor units, as described by Equation 5.16; the number of units required increases linearly with SFCL resistance.

$$total\ units \geq \left(\frac{\lambda I_{load}}{I_{c_{unit}}}\right)^2 \frac{R_{SFCL}}{R_{unit}} \tag{5.16}$$

Figure 5.8 compares this relationship with the initial estimate described by Equation 5.12, where $I_{load} = 250$ A, $R_{unit} = 1\ \Omega$, $I_{unit} = 200$ A, and $I_{c_{unit}} = 100$ A. It is assumed that $\lambda = 2$. This is based on fusing factors for fuses because the manufacture of superconducting wire may be subject to similar tolerances, but values of λ such as 4 or 5 may be more appropriate [DKH$^+$10]. When I_c is not considered as in Equation 5.12, Figure 5.8 illustrates that the required number of superconductor units for a given fault current reduction is substantially underestimated. Furthermore, the number of superconductor units required does not depend on whether the SFCL is located at the 33 kV or 690 V side of the transformer in Figure 5.1 and, as noted in [SYG$^+$03, SH09, TPF$^+$01, KM04], is independent of superconductor resistivity. This is valid for a constant power rating.

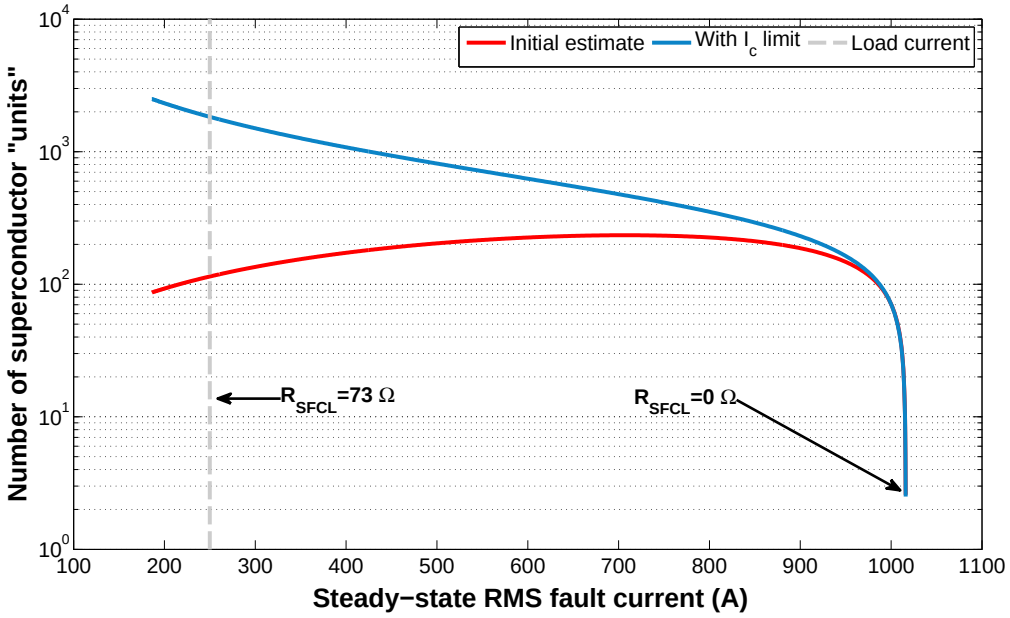


Figure 5.8: Number of notional superconductor units required for a given level of fault current limitation

The manufacturing process of the superconductor may dictate additional constraints, such as the minimum cross-sectional area of the wire. The SFCL must be rated to handle the peak limited fault current which may be substantially larger than the steady-state fault current; this may increase the required number of notional superconducting units because the thermal limit, dictated by $\int i(t)^2 R_{SFCL} dt$, must not be exceeded.

5.4.1 Comparison with Exponential SFCL model

Having shown that the analytical calculation for energy dissipation is valid by comparison with simulation results, the simulation model can be improved by approximating the development of the SFCL's resistance over time, using the exponential SFCL model described in Appendix A. In this model, τ is the time constant which determines the rate at which the SFCL develops its full resistance.

Figure 5.9 compares the total energy dissipation using the binary model and the exponential model. $\alpha = 0$ in each case. For relatively large values of τ such as 10 ms, because the value of R_{SFCL} varies with time, the value of R_{SFCL} which

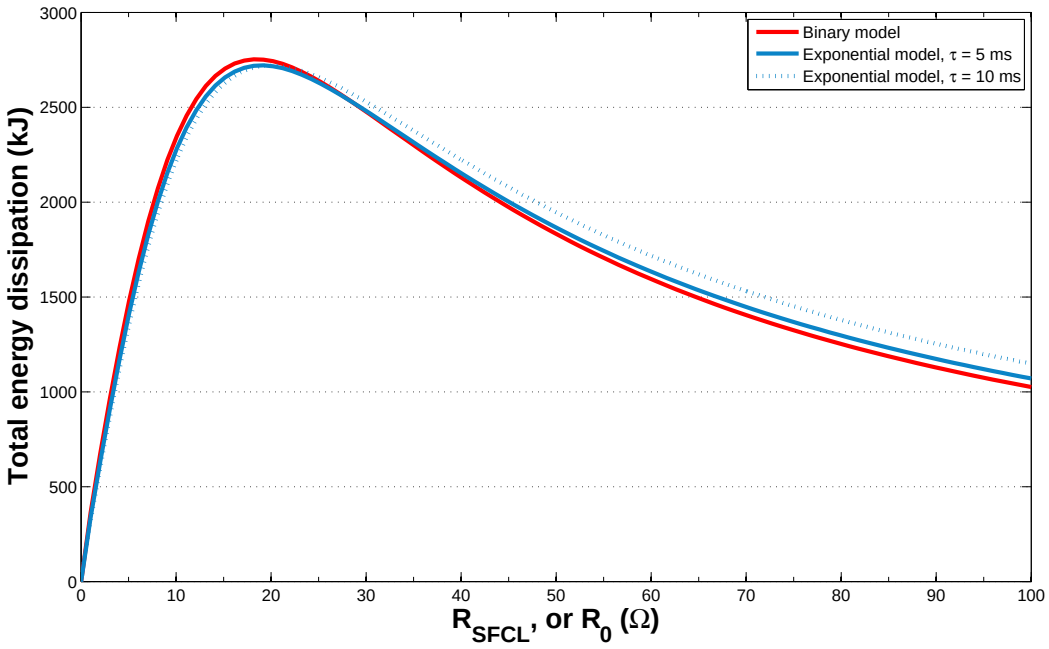


Figure 5.9: Comparison of total energy dissipation between binary and exponential SFCL models

maximises Q changes: it is approximately 20.1 Ω rather than 18.2 Ω as derived in Section 5.3.1. Similarly, the binary SFCL model will also underestimate Q when $R_{SFCL} \lessapprox \hat{Q}$ and will slightly overestimate Q when $R_{SFCL} \gtrapprox \hat{Q}$. However, the binary model still provides a satisfactory approximation of the total energy dissipation. For $\tau = 5$ ms, the maximum difference between the two models shown in Figure 5.9 is 6.03%.

5.5 Relationship to Other Research

Several studies advise on the optimal selection of the impedance of an SFCL, in terms of: reducing the impact on existing protection schemes [KT99]; minimising the power exchanged between regions of a power system during a fault [SPPK09b]; finding the smallest SFCL impedance to maintain fault levels in marine vessels within circuit breaker ratings; and analysing the transient stability of induction machines [ETS+10] and synchronous generators [TMTK01, SPPK09a]. As described in Section 5.3.4, a multi-objective optimisation technique is presented in

[SH09]. Reference [ZX11] proposes an optimisation method for selecting FCL impedance values to counteract the additional fault current contribution from DG. References [DYF+08, SKN08] provide experimental results of the typical energy dissipation in resistive SFCLs.

5.6 Conclusions

The focus of this chapter has been to thoroughly analyse the relationship between energy dissipation and SFCL resistance, to highlight the compromises between the factors that affect the choice of SFCL resistance, and to illustrate why a particular SFCL design is appropriate (or inappropriate).

This chapter has presented a guide for selecting the resistance value of a resistive SFCL, taking into account energy dissipation and the necessary volume of superconductor material. It has been established that the volume of the superconducting material is proportional to the resistance of the SFCL.

It also has been established that the maximum energy dissipation occurs when the SFCL resistance approximately equals the magnitude of the source impedance, a result that would be expected from the maximum power transfer theorem. Therefore, to reduce energy dissipation and therefore shorten recovery times, the SFCL resistance should be much larger than the source impedance. A larger SFCL resistance requires a larger volume of superconducting material. Consequently, it has been shown that there is a compromise between lower energy dissipation, and therefore faster recovery times, and superconductor volume, which incurs capital costs. The application of SFCLs in 11 kV and 33 kV distribution systems, compared to transmission systems, is especially cost-sensitive due to the relatively lower costs of circuit breakers and other equipment.

Chapter 6

Current-Time Characteristics of Resistive SFCLs

6.1 Introduction

For SFCLs to be effectively applied in power systems, it is important to understand their transient properties in order to coordinate their operation with power system protection devices and to ensure that, in a system with multiple SFCLs, only the SFCL(s) closest to the fault location operate in order to avoid unnecessary disturbance to healthy elements of the system. This chapter analyses a typical transient SFCL model, and determines its current-time characteristics. Section 6.2 introduces the SFCL model, and the model is analysed mathematically in Section 6.3.

6.2 SFCL Model

6.2.1 Requirements

For this study, it is important to realistically model an SFCL's resistance characteristics, in particular:

- In a three-phase power system, each phase of the SFCL must be modelled

independently because they will operate independently, particularly during unbalanced primary system faults, which represent the predominant mode of fault in power distribution systems (particularly in overhead systems) [Als11]. Each phase will have a dedicated superconducting wire (or several wires) which form a superconducting element. This means that within the first cycle of fault current during a three-phase to earth fault, each phase of the SFCL will develop resistance at a slightly different time, hence creating a momentary phase unbalance. Unbalanced faults may only cause a quench in only one or two phases of the SFCL. Independent operation of each phase must be represented such that the effects on the overall power system can be evaluated for all fault types at various locations.

- The SFCL model should be a reasonable approximation of transient SFCL behaviour during faults, and therefore should consider thermal properties [DYF+08]. The model should be adaptable, with little or no modification, for different types of faults or other scenarios. It should be able to model the effects of different fault durations, different times of fault occurrences, different fault current magnitudes, and cater for any point of fault occurrence with respect to the voltage waveform. The model should execute without excessively long simulation times.

- The dimensions of the superconducting wires must be known. A given superconducting wire will have a full load current rating. To achieve a higher full load current rating, several wires may be connected in parallel, as described in [DKH+10] and Chapter 5.

6.2.2 Implementation

Based on the requirements in Section 6.2.1, SFCLs have been modelled using the equations from [PCL+00], as given in Figure 6.1 and described in Appendix A. The model has been implemented for Simulink/SimPowerSystems [Mat11], and is available at [Bla12a]. An independent, single-phase superconductor model has been replicated to create a three-phase SFCL. Table 6.1 defines the symbols and

values used.

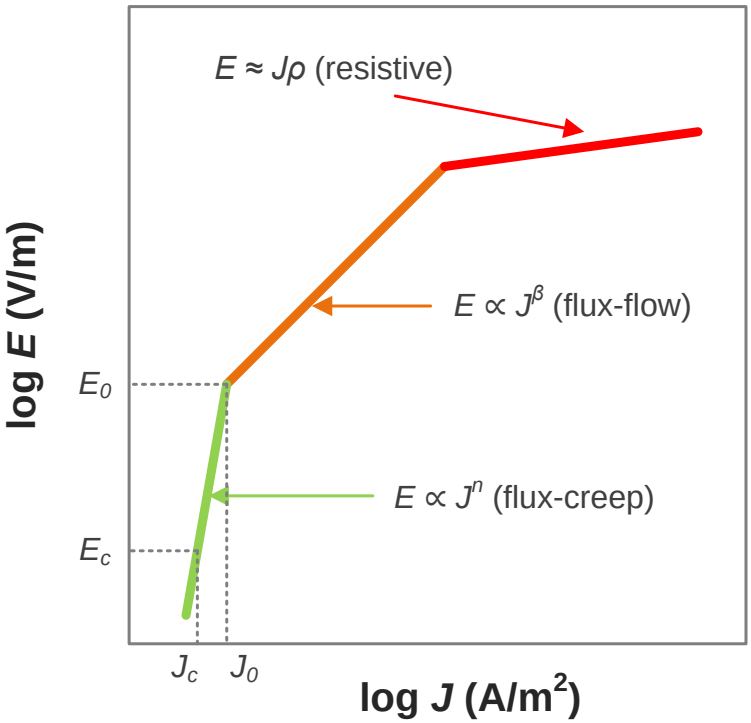


Figure 6.1: Superconductor E-J characteristic (from [PCL+00])

The thermal sub-system has been modelled as follows:

$$T(t) = T_a + \frac{1}{c_{sc}} \int_0^t [Q_{sc}(t) - Q_{removed}(t)]\, dt. \tag{6.1}$$

It is assumed that the superconductor resistivity varies linearly with temperature, when $T(t) \geq T_c$, as given by Equation 6.2. This is a reasonable assumption and is justified and supported by the experimental results in [LLG+11]. The variation of J_c with temperature is also assumed to be linear, as shown in Equation 6.3. Reference [KJKK+05] illustrates this property for BSCCO, and reference [OSH+09] for MgB_2; it is this variation of J_c (and J_0) with temperature which allows the operating current for an SFCL to be adjusted.

$$E(t,T) \approx \rho \left(\frac{T}{T_c}\right) J(t), \qquad T(t) \geq T_c \tag{6.2}$$

$$J_c(T) \approx J_{c_{77K}} \left(\frac{T_c - T(t)}{T_c - 77}\right) \tag{6.3}$$

Parameter description	**Symbol**	**Value**	**Units**
Length of the superconductor wire	l_{sc}	50	m
Diameter of the superconductor wire	d_{sc}	4.0 x 10^{-3}	m
Cross-sectional area of the superconductor wire	a_{sc}	$\pi \left(\frac{d_{sc}}{2}\right)^2$	m^2
Superconductor temperature	$T(t)$	—	K
Superconductor current	$i_{sc}(t)$	—	A
Ambient (starting) temperature of the superconductor and cooling reservoir	T_a	77	K
Superconductor critical temperature	T_c	95	K
Flux-creep region exponent (at 77K)	n_{77K}	6	—
Flux-flow region exponent	β	3	—
Current density	$J(t)$	$\frac{i_{sc}(t)}{a_{sc}}$	A/m^2
Critical current density (at 77K), i.e., current density where $E = 1\mu V/cm$	$J_{c_{77K}}$	1.5 x 10^7	A/m^2
Electric field at transition from flux-creep state to flux-flow state	E_0	0.1	V/m
Normal conducting state resistivity (at T_c)	ρ	1.0 x 10^{-6}	Ωm
Coefficient for heat transfer to cooling reservoir	κ	1.5 x 10^3	W/Km^2
Superconductor volumetric specific heat	c_v	1.0 x 10^6	J/Km^3
Superconductor heat capacity	c_{sc}	$l_{sc}a_{sc}c_v$	J/K
Thermal resistance from superconductor to cooling reservoir	θ_{sc}	$\frac{1}{\kappa l_{sc}\pi d_{sc}}$	K/W
Heat dissipated in the superconductor	$Q_{sc}(t)$	$\int i_{sc}(t)^2 R_{sc}(t)dt$	J
Heat removed by the cooling system	$Q_{removed}(t)$	$\int \frac{T(t)-T_a}{\theta_{sc}}dt$	J
Instantaneous superconductor resistance	$R_{sc}(t)$	$\frac{E(t,T)l_{sc}}{J(t)a_{sc}}$	Ω

Table 6.1: Summary of SFCL model parameters

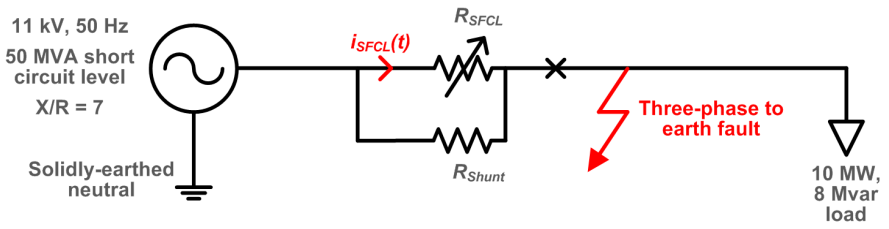


Figure 6.2: SFCL fault current limitation test network

Many of the parameter values given in Table 6.1 are taken from [LSW+05]. The resistivity at T_c, ρ, was selected as 1 $\mu\Omega$m and the length, l_{sc}, was varied to limit fault current to approximately the same root-mean-square (RMS) value as load current. This results in an SFCL phase resistance of approximately 4.0 Ω at 95 K, and 12.6 Ω at 300 K. The diameter, d_{sc}, was chosen such that the superconductor does not enter the flux-flow state during normal load current, but that each SFCL will enter the flux-flow state during the first cycle of fault current. In reality, the wire diameter may be fixed, but several wires may be connected in parallel to achieve a particular current rating, as discussed in Section 5.4. β was reduced to a value of 3 to reduce the rate of increase of flux-flow resistance. A cylindrical superconductor wire geometry is used, rather than the cuboid shape modelled in [LSW+05].

6.2.3 Example Operation

To test the fault current limitation properties of the model, the circuit in Figure 6.2 was simulated. Figure 6.3 illustrates the response of the model for a three-phase to earth fault, with negligible fault resistance. The SFCL quenches in each phase during the first peak of fault current. If the fault is cleared 0.1 s after occurrence, each phase of the SFCL takes between 2 and 4 s to drop below T_c. This SFCL design corresponds to the "slow-heating" category described in [PCL+00], because the quench time is in the order of 10 ms.

To simplify the analysis in this chapter, it is assumed that the SFCL does not have a shunt impedance. The effect of the shunt impedance will be most prominent after an SFCL fully quenches to the resistive state, which does not affect the analysis in the following section.

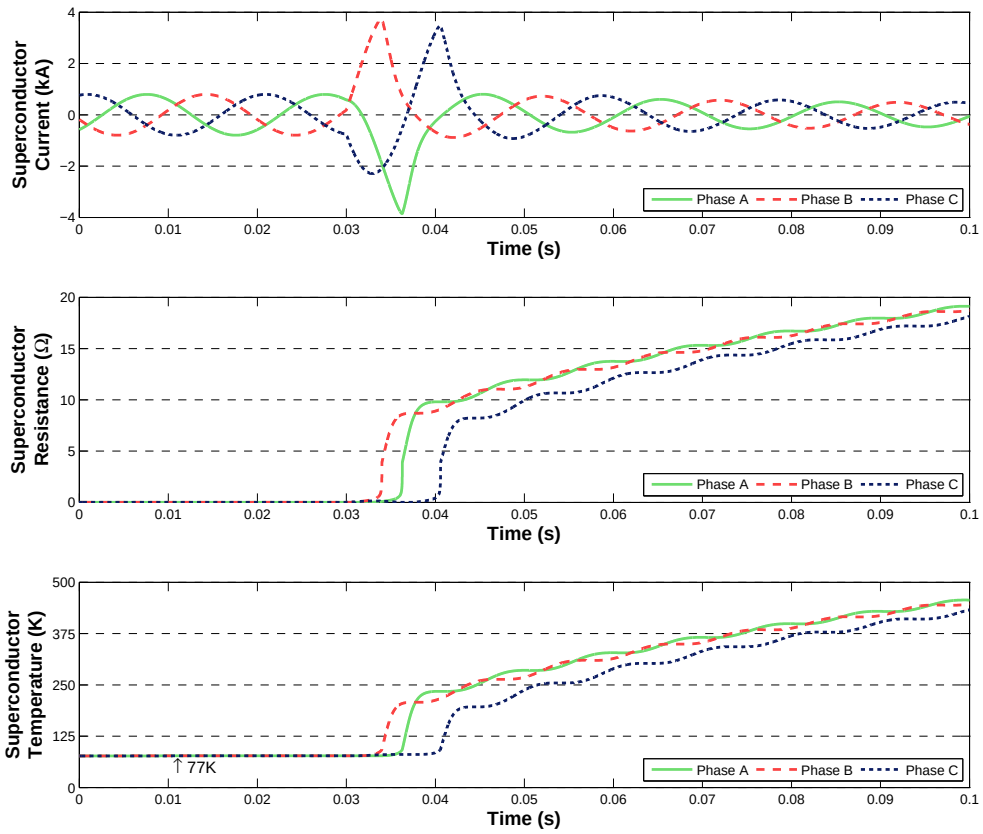


Figure 6.3: SFCL model response for a three-phase to earth fault

6.3 Analysis of SFCL Current-Time Characteristics

6.3.1 Analytical Solution

The SFCL model equations can be analysed to approximate the current-time grading, i.e., the time taken to quench for a given fault current. The temperature of the superconductor is calculated using Equation 6.1, where $E(t,T)$ (within $Q_{sc}(t)$) is calculated according to [PCL+00], in the flux-flow region (where $E(t,T) \geq E_0$ and $T(t) < T_c$). When $T(t) \geq T_c$, it is assumed that the superconductor quenches. Equation 6.1 can be differentiated and manipulated as follows:

$$
\begin{aligned}
\frac{dT}{dt} &= \frac{1}{c_{sc}}\left[Q_{sc}(t) - Q_{removed}(t)\right] \\
\frac{dT}{dt} &= \frac{1}{c_{sc}}\left[i(t)E(t,T)l_{sc} - \frac{T(t)-T_a}{\theta_{sc}}\right] \\
dt &= \frac{dT}{\frac{1}{c_{sc}}\left[i(t)E(t,T)l_{sc} - \frac{T(t)-T_a}{\theta_{sc}}\right]}.
\end{aligned}
$$

To simplify the analysis, a constant DC fault current, I, is assumed. Therefore, E can be simplified to be only a function of temperature:

$$
\int dt = \int \frac{dT}{\frac{1}{c_{sc}}\left[IE(T)l_{sc} - \frac{T(t)-T_a}{\theta_{sc}}\right]} \tag{6.4}
$$

where $E(T)$ is [PCL+00]:

$$
E(T) = E_0 \left(\frac{E_c}{E_0}\right)^{\frac{\beta}{n_{77K}}} \left(\frac{J_{c_{77K}}}{J_c(T)}\right) \left(\frac{J(t)}{J_{c_{77K}}}\right)^{\beta}. \tag{6.5}
$$

Substituting Equation 6.3 into Equation 6.5 gives:

$$
\begin{aligned}
E(T) &= E_0 \left(\frac{E_c}{E_0}\right)^{\frac{\beta}{n_{77K}}} \left(\frac{T_c - 77}{T_c - T}\right) \left(\frac{J(t)}{J_{c_{77K}}}\right)^{\beta} \\
&= E_0 \left(\frac{E_c}{E_0}\right)^{\frac{\beta}{n_{77K}}} \left(\frac{T_c - 77}{T_c - T}\right) \left(\frac{I}{J_{c_{77K}} a_{sc}}\right)^{\beta}.
\end{aligned}
$$

For convenience, the non-temperature-dependent part of $E(T)$, along with I and l_{sc} from Equation 6.4, can be combined as k as follows:

$$
\begin{aligned}
IE(T)l_{sc} &= k\frac{T_c - 77}{T_c - T} \\
k &= IE_0 \left(\frac{E_c}{E_0}\right)^{\frac{\beta}{n_{77K}}} \left(\frac{I}{J_{c77K}a_{sc}}\right)^{\beta} l_{sc} \\
k &= E_0 \left(\frac{E_c}{E_0}\right)^{\frac{\beta}{n_{77K}}} \frac{I^{\beta+1}}{\left(J_{c77K}a_{sc}\right)^{\beta}} l_{sc}.
\end{aligned}
$$

This provides an expression for t, the time for the superconductor to reach a particular temperature, T, as given by Equation 6.6 [YXWZ05]. t represents the time the superconductor spends in the flux-flow state.

$$
t = c_{sc} \int \frac{dT}{\left[k\frac{T_c-77}{T_c-T} - \frac{T-T_a}{\theta_{sc}}\right]}. \tag{6.6}
$$

Equation 6.6 can be solved by Equation 6.7. The constant, C, given in Equation 6.8, can be calculated by substituting $T(0) = T_a$ into Equation 6.7.

$$
\begin{aligned}
t = \; & c_{sc}\theta_{sc} \left(\frac{\arctan\left(\frac{T_a - 2T + T_c}{\sqrt{-(T_a-T_c)^2 + 4\theta_{sc}k(T_c-77)}}\right)(T_a - T_c)}{\sqrt{-\left(T_a - T_c\right)^2 + 4\theta_{sc}k\left(T_c - 77\right)}} \right. \\
& \left. - \frac{\ln\left(T^2 + \left(-T_a - T_c\right)T + T_aT_c + \theta_{sc}k\left(T_c - 77\right)\right)}{2} \right) + C
\end{aligned} \tag{6.7}
$$

$$
C = c_{sc}\theta_{sc} \left(\frac{\arctan\left(\frac{T_a - T_c}{\sqrt{-(T_a-T_c)^2 + 4\theta_{sc}k(T_c-77)}}\right)(T_a - T_c)}{\sqrt{-\left(T_a - T_c\right)^2 + 4\theta_{sc}k\left(T_c - 77\right)}} + \frac{\ln\left(\theta_{sc}k\left(T_c - 77\right)\right)}{2} \right) \tag{6.8}
$$

In the common case, using liquid nitrogen as the cryogen, where $T_a = 77$ K, $T_c = 95$ K, and $T = 95$ K, Equation 6.7 can be simplified to Equation 6.9 as follows:

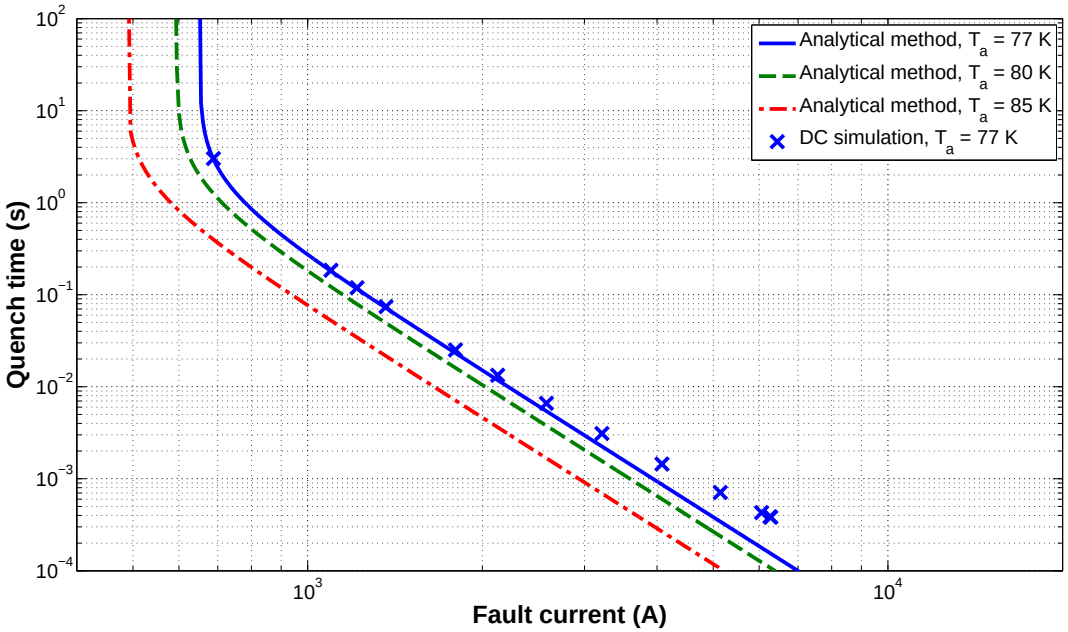


Figure 6.4: SFCL model current-time characteristics (analysis and simulation). Fault current for DC simulation is the initial fault current from a constant DC voltage source.

$$t = 6c_{sc}\theta_{sc}\frac{\arctan\left(\frac{3}{\sqrt{2\theta_{sc}k-9}}\right)}{\sqrt{2\theta_{sc}k-9}}. \tag{6.9}$$

Figure 6.4 illustrates the current-time characteristics for three different values of the initial temperature, T_a. For example, for $T_a = 77$ K, a fault current of at least 1.9 kA (RMS or DC) is required to ensure SFCL quenching within the first AC cycle (20 ms), compared with 1.4 kA when $T_a = 85$ K. The cut-off current for which quenching would not occur is shown by the vertical asymptotes. It can be noted that varying the initial superconductor temperature, T_a, affects both the critical current and the position with respect to the y-axis of the current-time curve, as illustrated in Figure 6.4, i.e., varying T_a shifts the curve to the left or to the right. Although this analysis excludes factors such as the instantaneous values of AC current and the point on wave of fault inception (see Section 6.3.2), it does show that an SFCL will inherently act in a manner that is consistent with an inverse current-time graded protection system.

It should be noted that, unlike inverse current-time protection relays, the flux-

flow resistance will reduce fault current before a circuit breaker opens, thereby slightly delaying quenching, compared with the quench time predicted by Equation 6.9. For simplicity, this is ignored in the analysis above, but Figure 6.4 also illustrates simulation results, using a single-phase constant DC voltage source. The fault current only drops by approximately 1-5%, until very close to the quench point. Very short quench times, in the order of 1 ms or less—where there is the largest difference between the analytical method and the DC simulation—may be unrealistic in practice because of the potential for transient overvoltages due to the high rate of change of current through the circuit inductance, L, with voltage given by $L\frac{di}{dt}$ [PCL+00].

6.3.2 Effect of the AC Point on Wave of Fault Inception

As described in Chapter 5, the instantaneous AC current during a fault can be modelled using Equation 6.10:

$$i(t) = I\left(\sin(\omega t + \alpha - \phi) - \sin(\alpha - \phi)e^{\frac{-Rt}{L}}\right) \tag{6.10}$$

where I is the peak current magnitude, $\omega = 2\pi f$, $f = 50$ Hz, α is the point on wave of fault inception, and $\phi = \tan^{-1}\left(\frac{\omega L}{R}\right) = \tan^{-1}\left(\frac{X}{R}\right)$. The X/R ratio is kept constant with a value of 7. Figure 6.5 illustrates how I and α affect the quench time.

The point of wave can delay a quench by 5-10 ms, depending on the current magnitude. The sharp transition between $\frac{\pi}{2}$ and $\frac{3\pi}{4}$ is due to the combination of DC offset and current phase $(\alpha - \phi)$ which results in a relatively small area under the current curve (and therefore low energy dissipation in the superconductor) during the first half cycle. If quenching does not occur within the first half-cycle of fault current, then there is a relatively long delay until quenching may occur at some point during the second half-cycle. This is illustrated in Figure 6.6; the DC offset is ignored for simplicity. SFCLs must therefore be carefully applied such that quenching will occur within the first cycle of fault current (at the required fault current magnitude), for any possible point on wave of fault inception. In

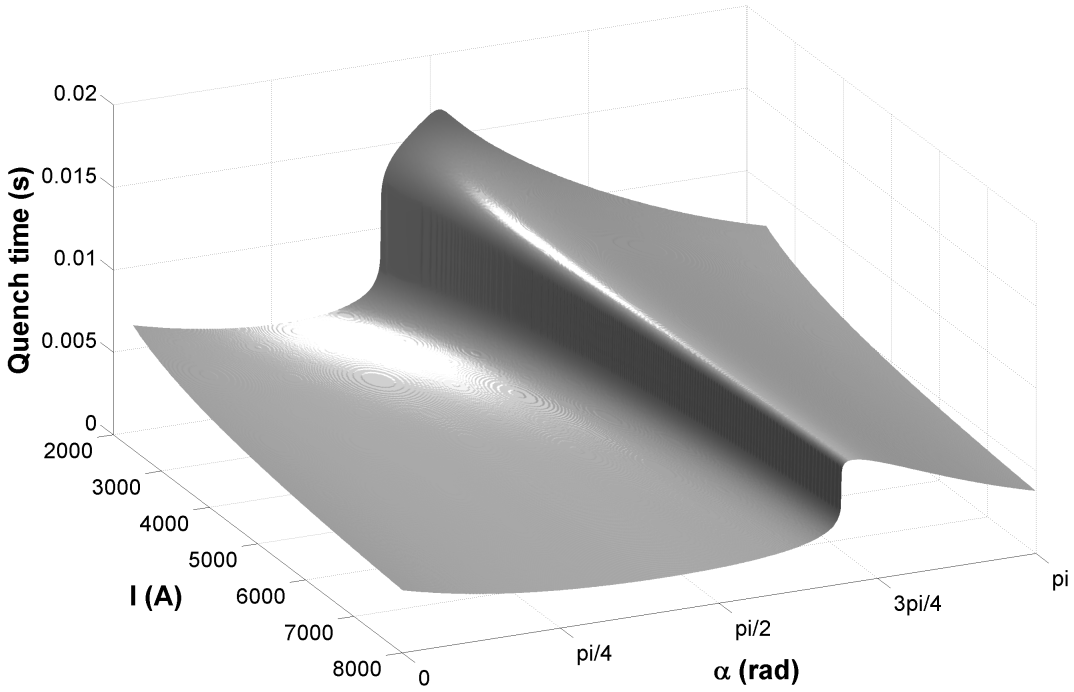
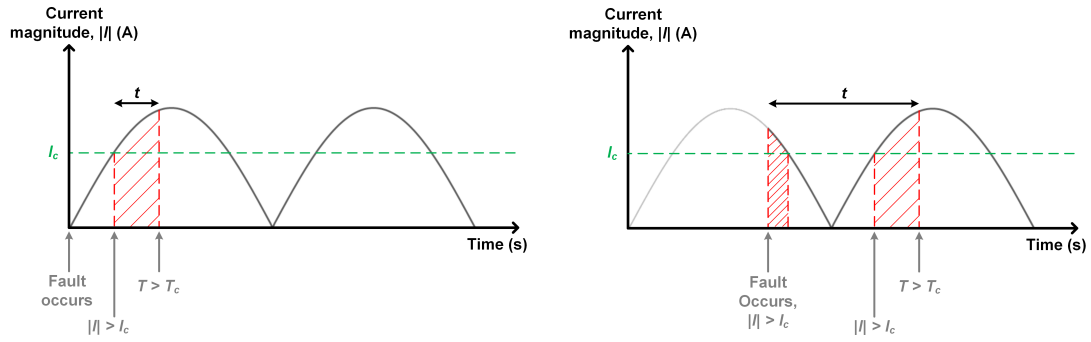


Figure 6.5: Effect of current magnitude and α on quench time

other words, the choice of critical current should be based on the symmetrical fault current which does not include the DC offset.



(a) Sufficient energy dissipation for quenching during first cycle

(b) Quenching in first cycle "missed" due to low energy dissipation

Figure 6.6: Explanation of delay due to fault inception angle

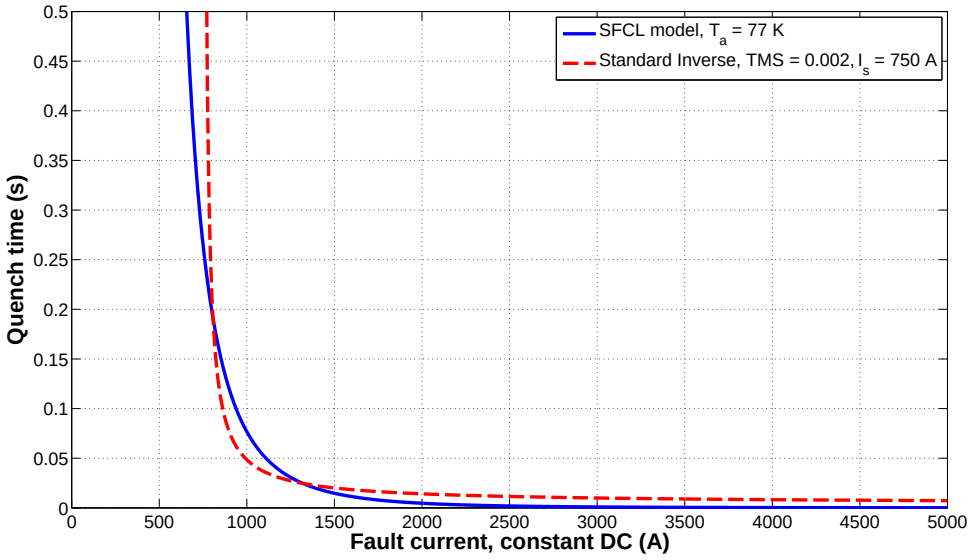


Figure 6.7: SFCL model current-time characteristics vs. Standard Inverse curve

6.3.3 Comparison of SFCL and Overcurrent Protection Current-Time Characteristics

To place the SFCL current-time curves in Figure 6.4 into perspective, they can be compared with an equivalent inverse definite minimum time (IDMT) curve, commonly used for overcurrent protection. Figure 6.7 compares the SFCL characteristics with the Standard Inverse curve [Als11], given by Equation 6.11:

$$t = TMS \frac{0.14}{{I_r}^{0.02} - 1} \tag{6.11}$$

where TMS is the time multiplier setting, $I_r = \frac{I}{I_s}$, and I_s is the setting current. For Figure 6.7, $TMS = 0.002$ and $I_s = 750$ A. Clearly, the curves differ, especially at higher currents, but this does demonstrate that an SFCL has similar characteristics to IDMT protection, albeit with a TMS value that would be extremely small in practice. This information could be used to coordinate the operation of multiple SFCLs in a power system in a similar fashion to the method used to coordinate overcurrent protection relays.

6.4 Conclusions

This chapter has established, through analysis of an existing SFCL model, that resistive SFCLs have an inverse current-time characteristic: they will quench in a time that inversely depends upon the initial fault current magnitude. The timescales are shown to be much shorter than those typical for inverse overcurrent protection. This has been verified mathematically. A generic equation has been derived which allows the quench time to be estimated for a given prospective fault current magnitude and initial superconductor temperature, and for various superconducting device and material properties. The analysis approach thereby represents a generic design tool which could be of value for the following:

- Quickly investigating the effect that modifying parameters, such as superconductor length and diameter, has on the current-time characteristics and the critical current value. An example of this has been implemented at [Bla12b], with the source code available at [Bla12c]. Figure 6.8 illustrates this tool. The tool allows various parameters to be varied, and the effect on the SFCL current-time characteristic and critical current is visualised.

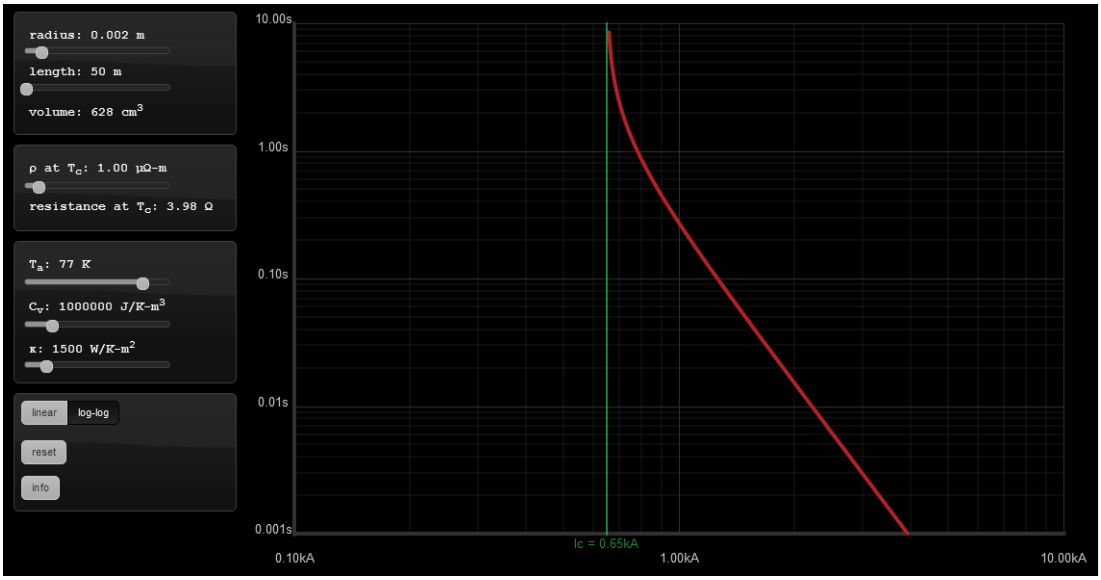


Figure 6.8: SFCL design tool

- To be used by power system designers in understanding the impact of SFCLs

on network protection systems during faults, and for planning the relative positions of multiple SFCLs.

- The coordination of multiple SFCLs, especially if they have different designs, e.g., from different manufacturers. In particular, it will also consequently permit the coordination of SFCL devices to ensure that only the device(s) closest to the fault location will operate.

- As a guide for adjusting the superconductor temperature, while the SFCL is in service, to cater for different system conditions and fault current reduction requirements.

- To determine the required superconductor volume for a desired current-time characteristic (i.e., solving for k, or a particular component of k).

Note that these results are closely linked to this particular SFCL model; nevertheless, the technique is valid as long as the SFCL characteristics are well known. The following chapter extends this work to examine the coordination of multiple SFCLs, and the associated implications for existing protection systems.

Chapter 7

Using Multiple Resistive SFCLs for Fast Fault Detection

7.1 Introduction

This chapter analyses the application of multiple resistive SFCLs to locate and rapidly isolate faulted circuit sections, as well as offering the typical benefits to power system performance from fault current limitation. This protection scheme uses an approach which is radically different from typical proposed applications of fault current limitation, and which does not require communications. The technique is based upon the intrinsic inverse current-time characteristics of resistive SFCLs, as established in Chapter 6, which ensures that only the SFCLs closest to a fault operate.

Section 7.2 introduces the principle of operation and summarises the potential benefits. Section 7.3 describes the SFCL and power system models, and Section 7.4 illustrates typical simulation results. Section 7.5 assesses the effectiveness of this technique under a variety of scenarios and Section 7.6 thereby concludes with recommended applications and caveats.

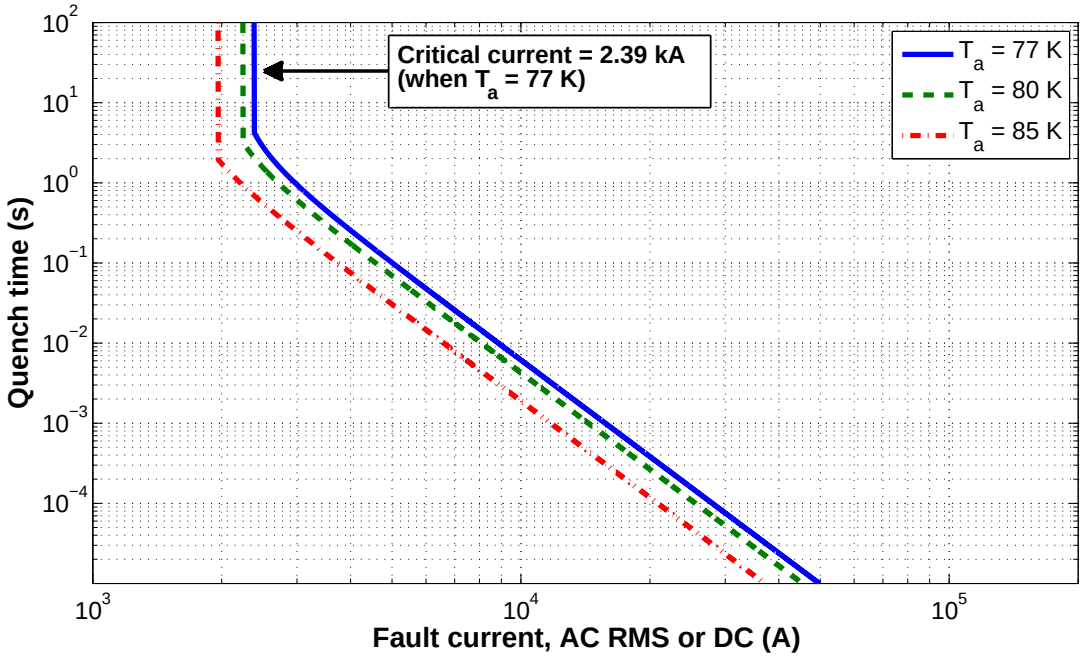


Figure 7.1: Typical SFCL model current-time characteristics, from method in Chapter 6

7.2 Principle of Operation

Generally, in interconnected systems, circuit sections nearer to a fault will carry more fault current than distant sections. This is a consequence of Kirchhoff's current law. If each circuit section is fitted with a protective device with the same current-time characteristic, devices closer to a fault will operate instead of devices further away, achieving the discrimination required to correctly isolate only the faulted section, with backup being provided in the event of the failure of a protection device close to the fault. This principle, which will be referred to as current division discrimination (CDD), was first used in interconnected low-voltage networks protected by fuses [IEE95], and has been extended to protection relays which control circuit breakers [Bri10]. CDD is well suited to meshed networks and networks with significant DG, and will typically still operate correctly despite system reconfiguration due to outages caused by faults or otherwise.

The analysis in Chapter 6 illustrates that a resistive SFCL will exhibit an inverse current-time characteristic, albeit operating much faster than overcurrent

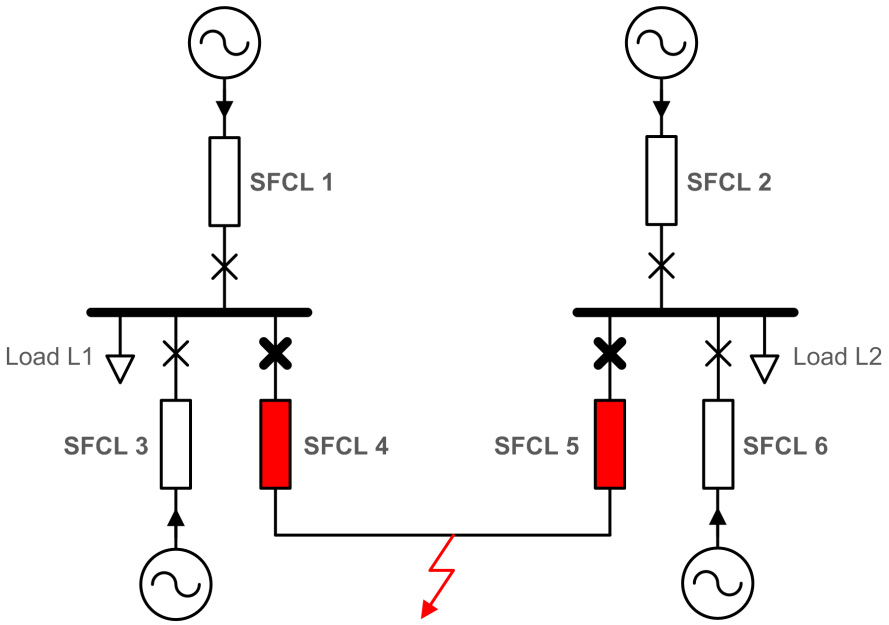


Figure 7.2: SFCL CDD operation example

protection relays (which also typically use an inverse current-time characteristic). Typical quench times, i.e., the time for the superconductor to transition from the superconducting state to the resistive state, are illustrated in Figure 7.1, where T_a is the initial superconductor temperature. This intrinsic inverse current-time characteristic therefore enables resistive SFCLs to be used in a CDD scheme.

An example of CDD operation is illustrated in Figure 7.2. If a short-circuit fault occurs on the bus-tie circuit section, SFCLs 4 and 5 would be required to operate. The circuit breakers in series with SFCLs 4 and 5 should then open to interrupt the fault current. These circuit breakers could be operated by, for example, trip coils supplied by voltage transformers connected across the SFCLs. Note that this method only identifies the faulted circuit section for protection purposes, not the exact position of the fault along the faulted circuit.

7.2.1 Benefits of CDD

A CDD scheme has the following benefits:

- Inherently locates (and isolates) the faulted circuit, because protective devices closest to the fault operate instead of devices further away. This is achieved without protection signaling, avoiding the cost of the required

telecommunications and their vulnerability to failure, especially during adverse circumstances which may have caused the power system fault in the first place.

- CDD is suitable for meshed power systems, whereas conventional protection schemes such as current-time graded inverse definite minimum time (IDMT) overcurrent are difficult, or even impossible, to coordinate, especially if the system suffers the loss of one or more circuit sections due to faults, or following network reconfiguration due to maintenance or otherwise.

- CDD is well suited to circumstances where the network topology, and therefore the paths of fault current, may change, especially without notice. CDD should be significantly simpler, more reliable, and easier to verify than a solution involving adaptive protection, where overcurrent relay settings are updated in response to network changes.

- Intrinsic, fast-acting back up: if a protection device close to the fault fails to operate or is out of service, the scheme will still apply to devices further from the fault. These devices will operate after a much shorter time grading margin, or time delay, than traditional overcurrent schemes. Shorter time grading margins help to maintain overall power system stability, and could be particularly beneficial in marine vessel electrical systems, where a fault that is not promptly and correctly isolated presents a high risk of causing total blackout of the power system [BSWD98, MV11, Mar11].

7.2.2 Advantages of Using SFCLs for CDD

The benefits of using SFCLs for CDD, further to the general benefits of SFCLs described in Section 3.2.3, include the following:

- The fast operation of SFCLs, when used in a CDD scheme, means that the fault current in any circuit section will never reach the prospective short-circuit fault current, i.e., the fault current that would flow without SFCLs in service. This is demonstrated in Section 7.5.1. This allows the use of

switchgear and other equipment with lower fault current ratings, offering savings in cost, weight, and space.

An SFCL will typically operate within the first cycle of fault occurrence (as established in Chapter 3), followed by one or more circuit breakers opening several cycles later. Without SFCLs, no remedial action occurs until a circuit breaker opens.

- In some circumstances, CDD will mitigate the inconvenience of the recovery period for resistive SFCLs. However, in systems with overhead line circuits which use autoreclose, CDD with resistive SFCLs may not be suitable. Section 7.5.3 discusses these issues in detail.

7.3 Simulation Models

7.3.1 SFCL Model

As described in Appendix A, references [PCL+00, LSW+05] describe a practical, generic resistive SFCL model for transient power system studies. The implementation and parameters of the SFCL model are documented in Chapter 6 and Table 7.1. To simplify the analysis in this chapter, it is assumed that the SFCL does not have a shunt impedance.

7.3.2 Power System Model

In order to test the SFCL model with the proposed CDD scheme, part of an 11 kV AC distribution system has been modelled, as illustrated in Figure 7.3. The power system and SFCLs have been simulated using Simulink/SimPowerSystems [Mat11] and, with some approximations, a Real-Time Digital Simulator (RTDS) [RTD11]. The RTDS has the advantage of being able to investigate many scenarios relatively quickly, compared to using an offline simulation package; SimPowerSystems is useful for exploring a smaller number of scenarios in greater detail.

Parameter description	**Value**	**Unit**
System voltage (line to line, RMS)	11	kV
Nominal system frequency	50	Hz
Source short-circuit power (each)	200	MVA
Source X/R ratio	7	—
Load real power (each)	20	MW
Load reactive (inductive) power (each)	4	Mvar
Neutral earthing resistance	16	Ω
Cable resistance (per metre)	0.083 x 10^{-3}	Ω/m
Cable inductance (per metre)	0.387 x 10^{-6}	H/m
Fault resistance	1 x 10^{-6}	Ω
Superconductor critical temperature (T_c)	95	K
Superconductor ambient (initial) temperature (T_a)	77	K
SFCL phase wire diameter	0.008	m
SFCL phase wire length	100	m
SFCL critical current rating per phase (I_c)	2.39	kA
SFCL resistance per phase at T_c	1.99	Ω

Table 7.1: Summary of power system parameters

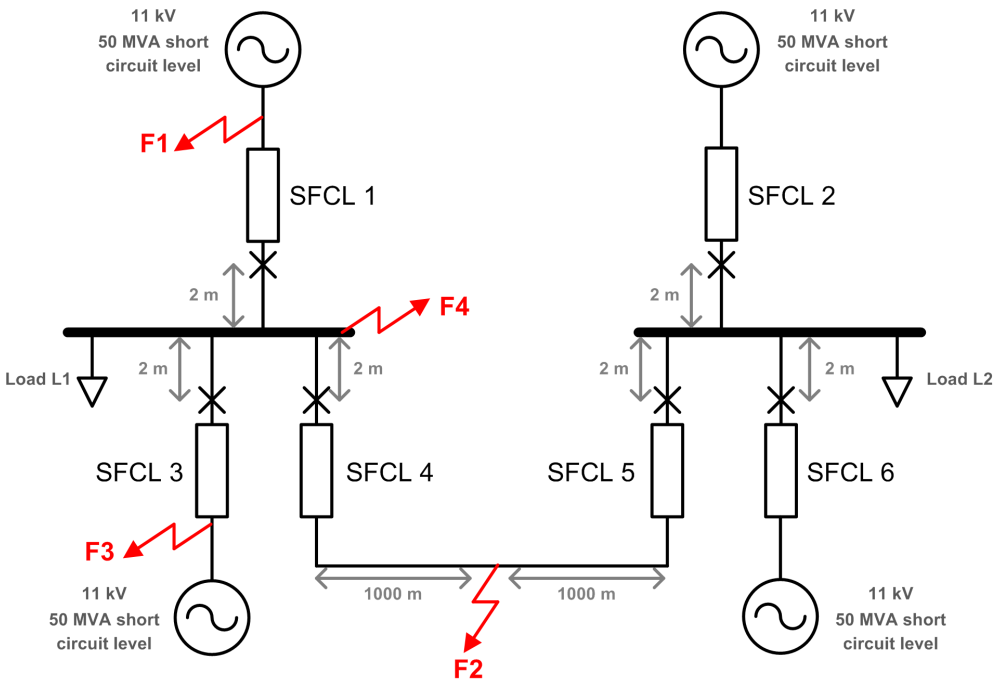


Figure 7.3: Example 11 kV AC distribution system

The power system model is intended to represent two interconnected substations, where each substation has two fault current infeeds, modelled as voltage sources. Each of the sources shown in Figure 7.3 could represent a grid infeed, DG, or the infeed from another distribution substation. A load is connected at each substation bus. The system parameters are summarised in Table 7.1, unless stated otherwise for a particular test. These parameters are representative instead of specific, and they serve the purpose of testing the SFCL model for a given critical current rating (i.e., the current value which initiates superconductor quenching). In this case, the critical current of each SFCL is approximately 2.39 kA RMS, as illustrated in Figure 7.1.

The neutral earthing resistance, when required, has been chosen to limit the single-phase to earth fault current to approximately 1 kA RMS, according to typical utility practice [IEE01]. The capacitive coupling to earth for the cables is not modelled. Due to the relatively short lengths, cable impedances are represented as a series resistance and inductance, using per-length values from [FEN+09].

Four fault locations, F1–4, are examined in this chapter, as shown in Figure 7.3. All faults occur at 0.03 s. Without SFCLs in service, a three-phase to earth

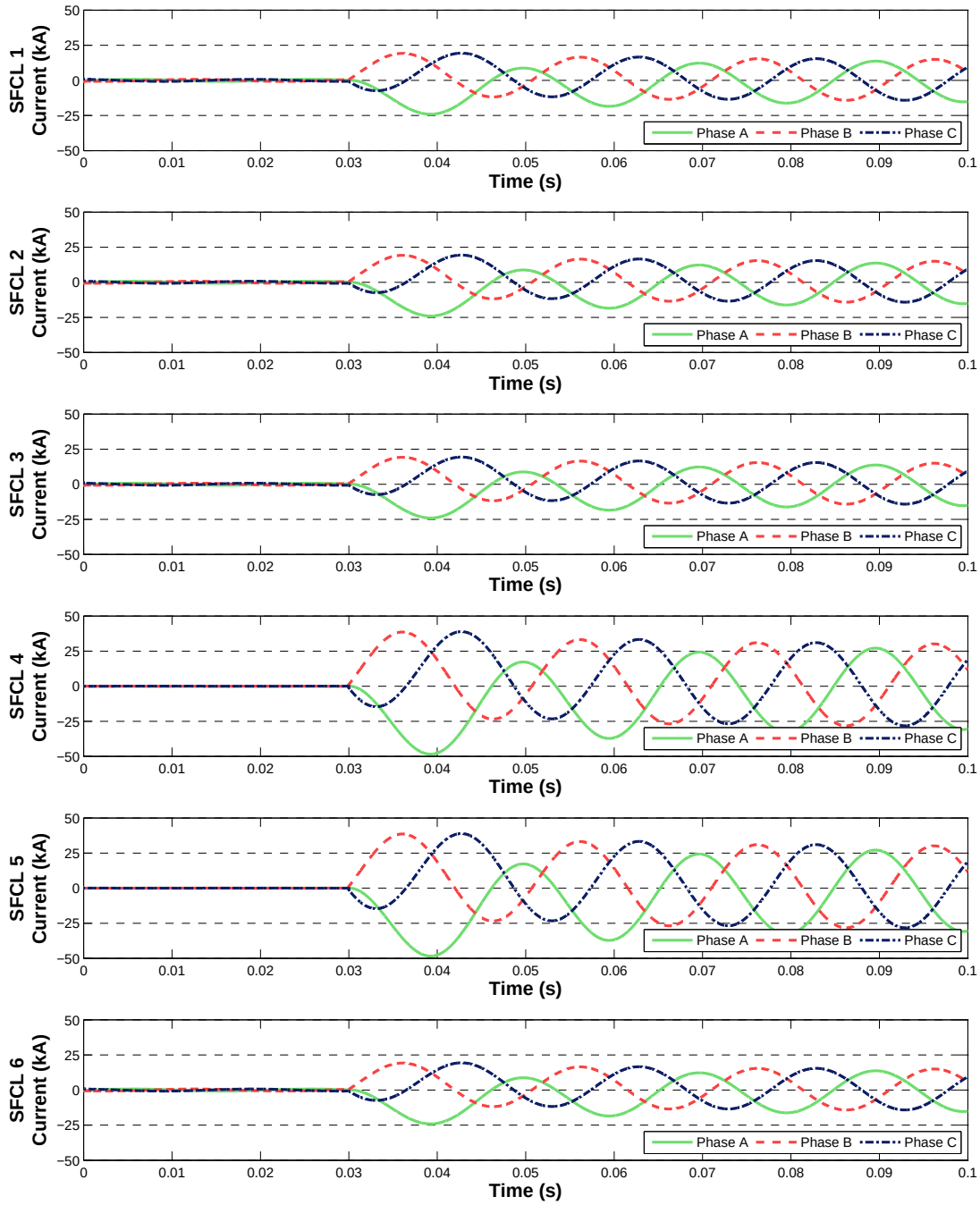


Figure 7.4: Fault currents without SFCLs, for three-phase to earth fault at F2

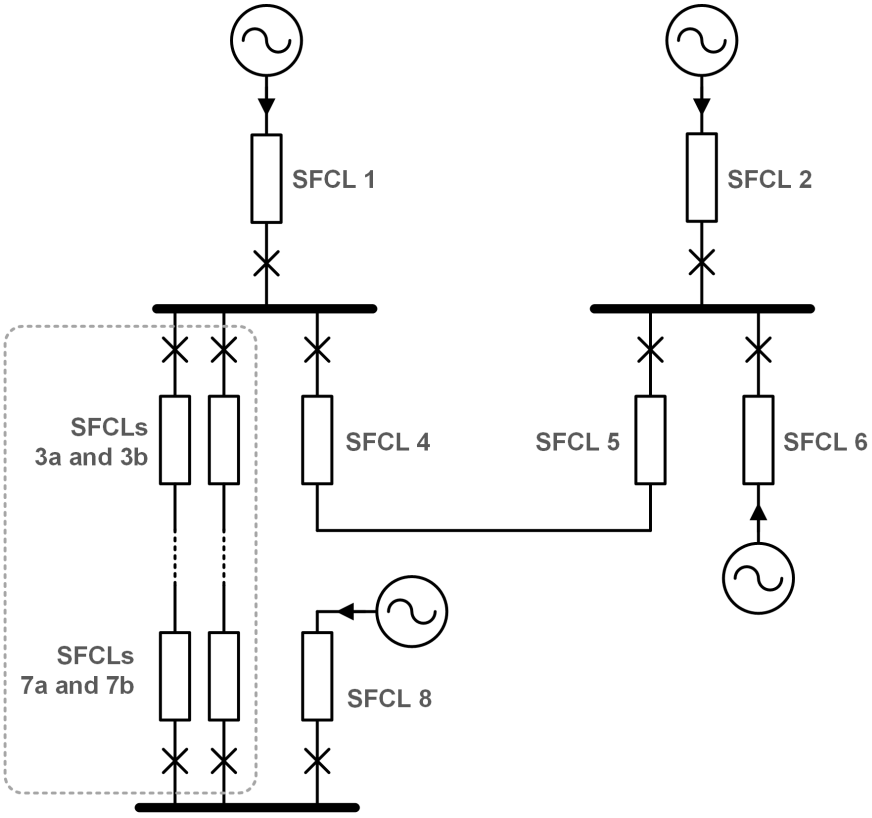


Figure 7.5: Double circuit application of CDD (in dashed box)

fault at the middle of the interconnecting feeder (fault F2) results in a fault current contribution from each source with a maximum peak of approximately 24.1 kA and a steady-state value of 10.0 kA RMS, as illustrated in Figure 7.4.

7.3.3 Application to Double Circuits

The power system model used in this chapter is, for illustrative purposes, the simplest example of a network which supports the application of CDD. The concept is generic and can be applied to more complex meshed systems. Figure 7.5 shows how the scheme could be used to protect a double circuit configuration. Preferably, SFCLs should be installed at both ends of each circuit which interconnects two buses.

7.4 Simulation Results

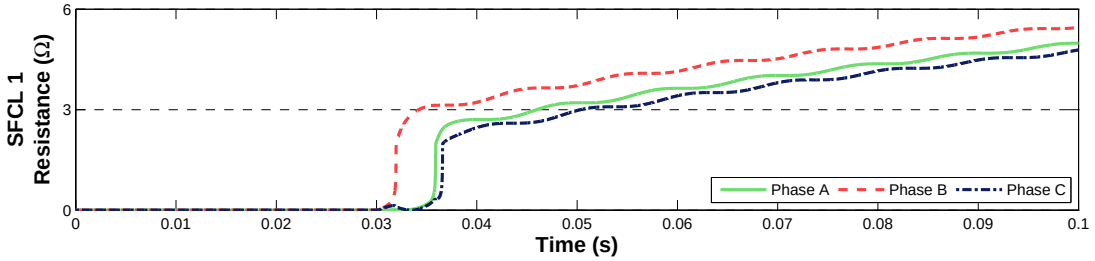
7.4.1 Typical CDD Results

The tests described in this subsection demonstrate that CDD correctly locates the faulted circuit section. These tests also provide the reference case for other tests. Figure 7.6a plots the SFCL 1 resistance for a fault at F1, and Figure 7.6b plots the corresponding currents in each SFCL. As expected, only SFCL 1 quenches, and no other SFCLs develop resistance during the fault. Fault F3 produces similar results.

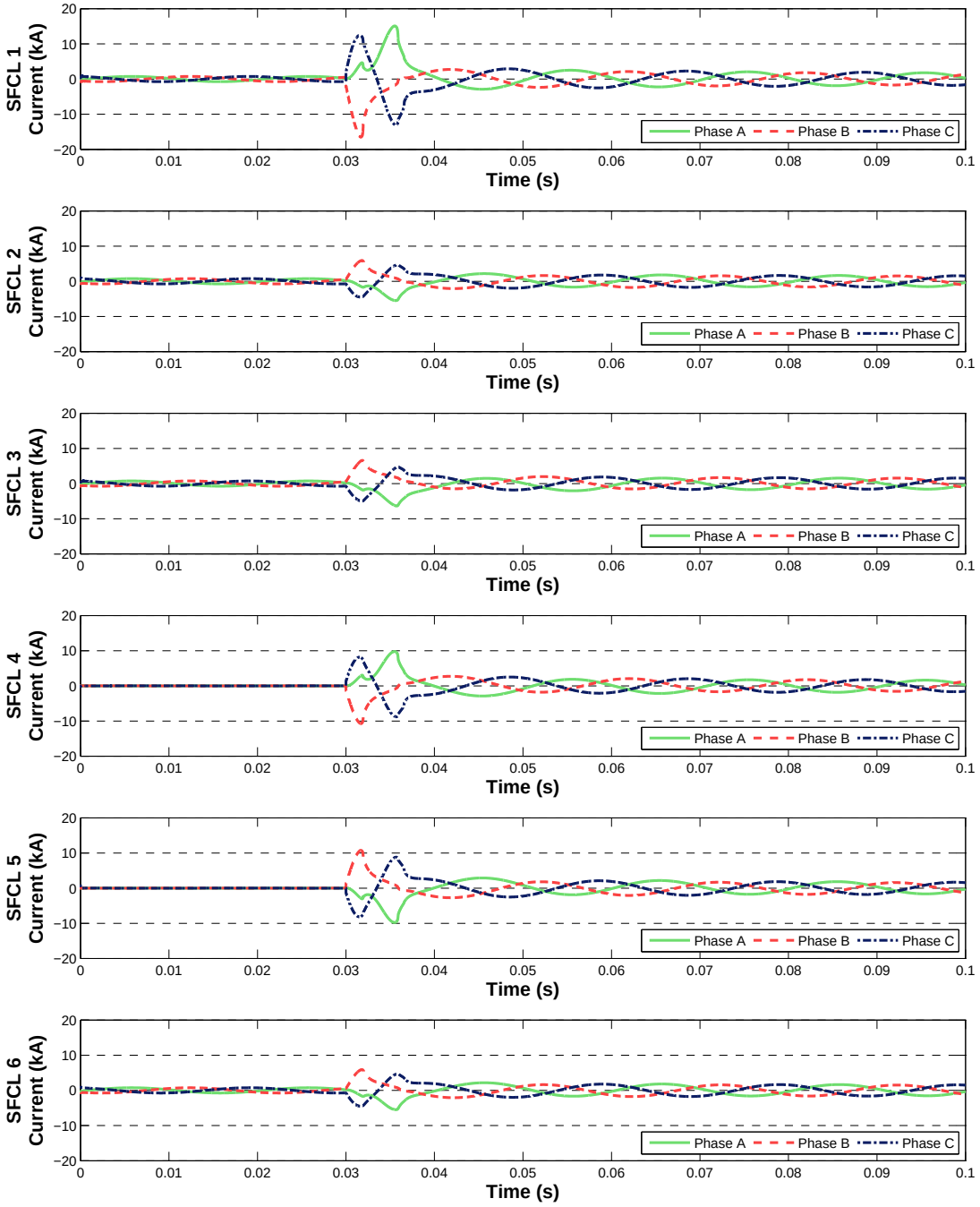
The resistances of SFCLs 4 and 5 for fault F2, at the middle of the bus-tie circuit, are shown in Figure 7.7. For brevity, the other SFCLs (which do not quench) and the fault currents are not shown. Again, the SFCLs quench in a manner that unambiguously identifies the faulted circuit. Discrimination is achieved regardless of the precise position of fault F2 between the two substations.

For faults located at F4, at the bus in the left substation, it is inevitable that both SFCL 4 and SFCL 5 will carry the same fault current. Therefore, both of these SFCLs quench. The quench of SFCL 5 is undesirable, but not particularly problematic because it would not cause any interruption in supplies beyond that caused by the fault at the substation in question. Furthermore, following such a serious fault at a busbar, the bus-tie circuit would not be restored to service until the busbar at the substation was also restored to service, a process that would take far longer than the time for both SFCLs to recover. The operation of both SFCL 4 and 5 for this fault would give an ambiguous indication of the faulted circuit location, suggesting it might be in the middle of the associated circuit instead of at the faulted bus. This ambiguity would be resolved by taking care to note the operation of all other protective devices within each substation before deciding on the location of the fault. Therefore, post-fault automation may be required within substations which implement a CDD scheme.

It should be noted, however, that a fault on any circuit section which is not protected by an SFCL, i.e., which is external to the CDD scheme, would be



(a) SFCL 1 resistance, for three-phase fault at F1



(b) SFCL currents, for three-phase fault at F1

Figure 7.6: SFCL resistances and currents for three-phase fault at F1

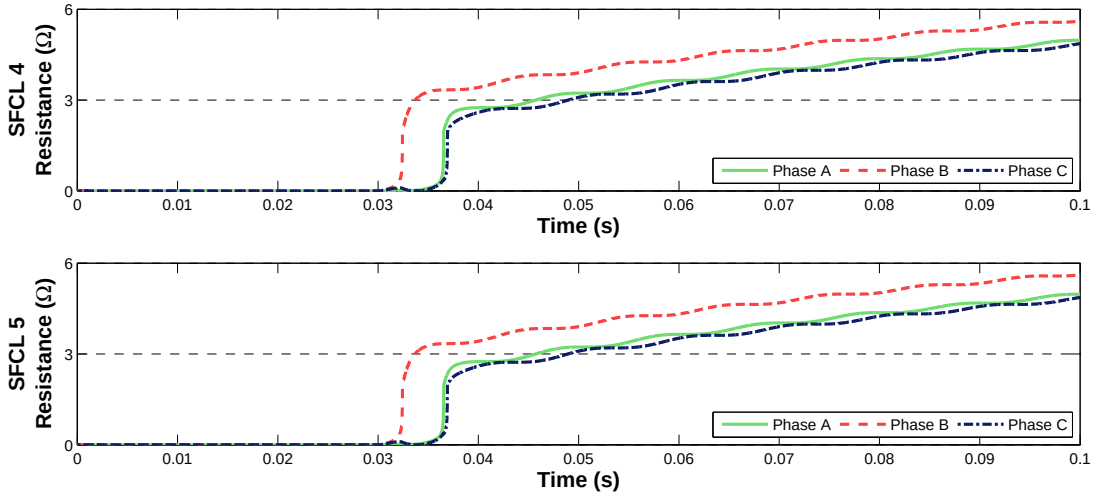


Figure 7.7: SFCL 4 and 5 resistances, for three-phase fault at F2

electrically equivalent to a bus fault (e.g., fault F4) and therefore may cause several SFCLs to quench.

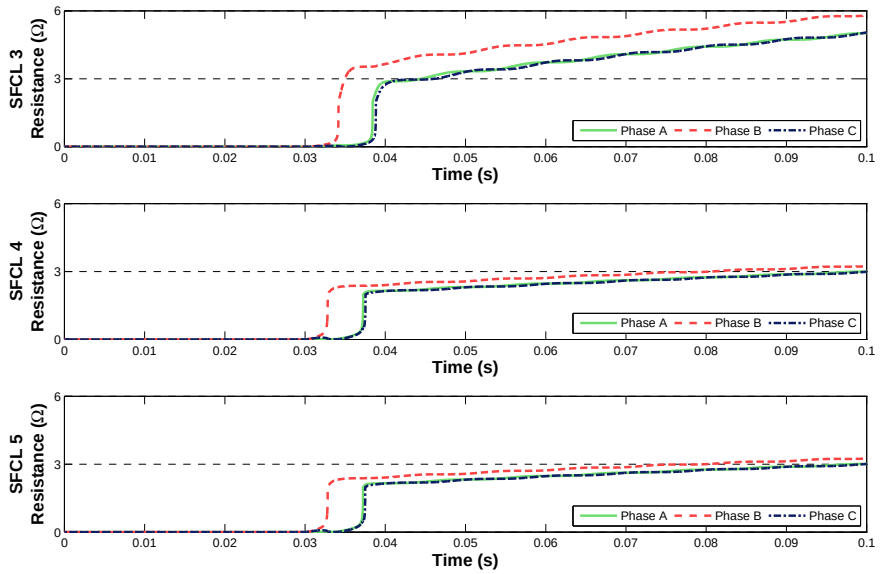
7.4.2 Backup Operation

Figure 7.8a illustrates backup operation for fault F1, where SFCL 1 has been electrically bypassed or otherwise taken out of service. SFCLs 3, 4 and 5 quench within the first half-cycle of fault current, providing a very fast-acting form of backup which still significantly reduces fault currents, as illustrated in Figure 7.8b.

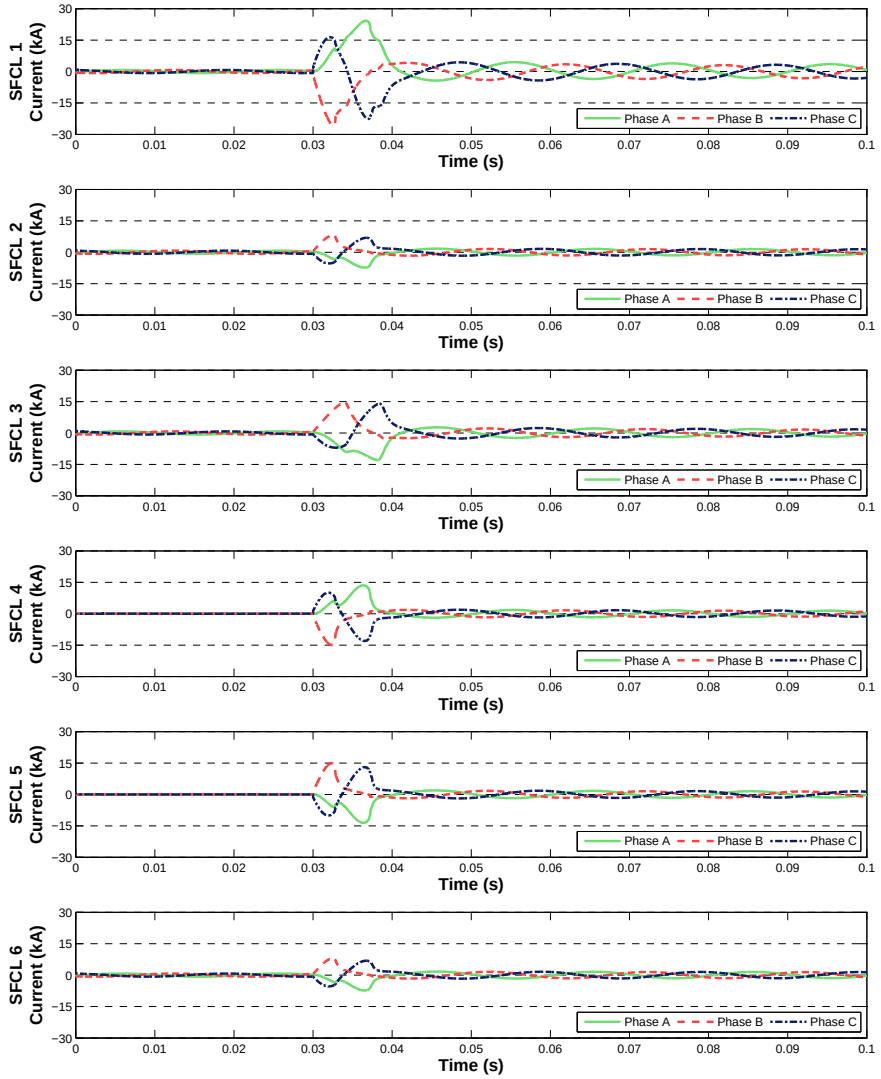
Nevertheless, it is difficult to readily use the information about which SFCLs quenched to accurately locate the faulted circuit; the protection system is still responsible for detecting the fault and, ideally, opening the circuit breaker adjacent to SFCL 1. Provided SFCL outages are uncommon, however, some loss of discrimination may be acceptable in practice.

7.4.3 Fault Types and Neutral Earthing Type

Correct coordination for all fault types and all fault locations is achieved regardless of the point on wave of fault occurrence. This has been determined using an automated script with the RTDS, to test a wide number of scenarios relatively quickly. The point on wave value does, however, dictate which phase of



(a) SFCL 3-5 resistances, for three-phase fault at F1, during backup operation



(b) SFCL currents, for three-phase fault at F1, during backup operation

Figure 7.8: SFCL backup operation for three-phase fault at F1

the SFCL will quench first for two- or three-phase faults. No SFCLs quenched in response to single-phase to earth faults with high-resistance neutral earthing, or with the neutral unearthed, because of the relatively low fault current which has been deliberately limited by other means. In solidly-earthed systems, however, there was enough earth fault current for the correct operation of the SFCLs closest to the fault. SFCLs also provide backup for failure of the neutral earthing impedance, e.g., by flash-over, although this is an unlikely event and is not normally considered in the design of utility electrical systems.

7.5 Discussion of Potential Issues

This section addresses factors which may influence the operation of CDD with SFCLs, and other practical concerns.

7.5.1 Comparison with Single Bus-tie SFCL

A system-wide implementation of the scheme proposed in this chapter would clearly require many SFCL devices (one or two SFCLs per circuit). Installing an SFCL at a bus-tie location in a power system, as illustrated in Figure 7.9, is often preferred to other locations [BBE+11]. In the general case, for a meshed system, techniques have been developed for determining the best placement of SFCLs, considering the rating of circuit breakers and the amount of fault current limitation [TL10], and for selecting the optimal SFCL specification [SH09, HS10]. Although a single SFCL at a bus-tie does not help locate faults in the manner achieved by CDD, which requires many SFCLs, the reduction in fault current can be substantial. The total fault current in some circuit sections is approximately halved, with only one SFCL being required. Furthermore, with an SFCL located at a bus-tie, few protection changes are required compared with other SFCL locations [BSBB09].

Nevertheless, CDD not only locates faulted circuits but also has another significant advantage over the use of a single SFCL: the fault current in any circuit section will never reach the prospective short-circuit fault current. Table 7.2 il-

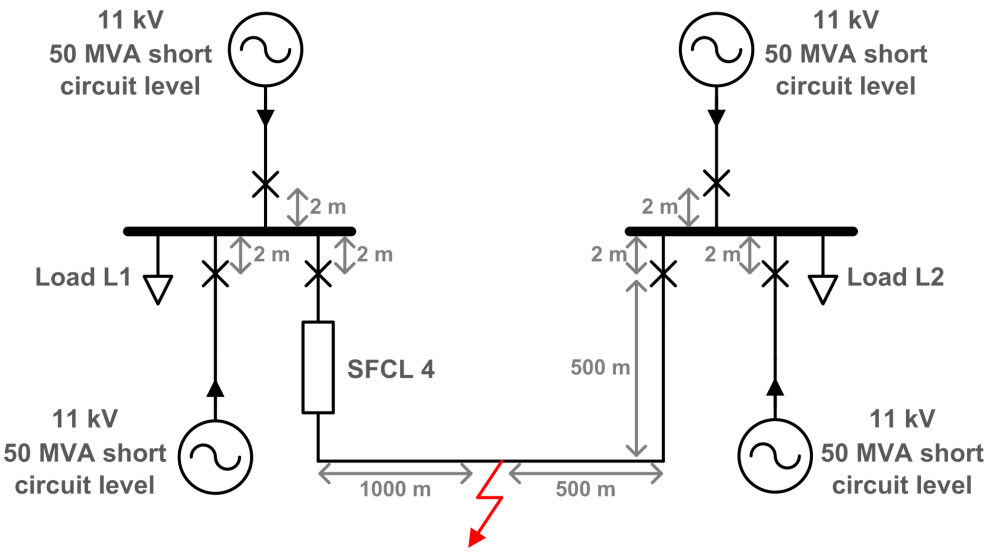


Figure 7.9: Single bus-tie SFCL location

Current measurement location	Peak fault current for fault F1 (kA)		Peak fault current for fault F2 (kA)	
	Single SFCL	Six SFCLs	Single SFCL	Six SFCLs
SFCL 1	33.2	17.7	9.09	9.05
SFCL 2	9.10	6.40	24.1	9.06
SFCL 3	24.1	6.78	9.09	9.05
SFCL 4	17.3	11.7	48.4	17.2
SFCL 5	17.3	11.7	48.4	17.2
SFCL 6	9.10	6.40	24.1	9.06

Table 7.2: Difference in peak fault current between six SFCLs and single SFCL

lustrates the significant reduction in peak fault current that is possible with six SFCLs (Figure 7.3), compared with a single SFCL (Figure 7.9).

7.5.2 Variable Fault Levels

The following circumstances will change fault levels: the connection or disconnection of circuit sections, and the connection or disconnection of generation. Each case is discussed below.

Figure 7.10 illustrates the effect of the disconnection of the feeder connected to SFCL 1, for fault F2. SFCLs 3 and 4 carry almost exactly the same fault current,

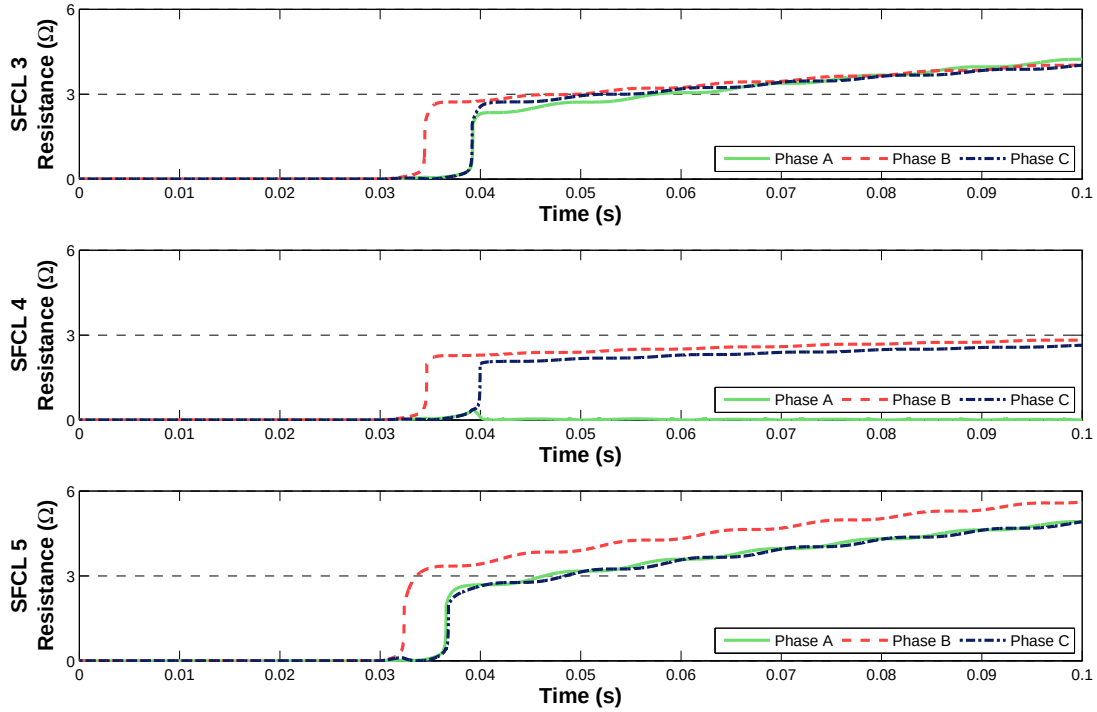


Figure 7.10: SFCL 3-5 resistances, for three-phase fault at F2, without the incoming feeder at SFCL 1

and therefore poor discrimination occurs due to SFCL 3 quenching when the fault occurs. Similar results are obtained for other fault types and fault locations. In general, this problem will exist if any bus has only two (possible) fault current infeeds. In other words, for correct discrimination, each bus must have at least three possible infeeds that can supply fault current. Hence, CDD is best suited to highly-interconnected electrical systems.

For moderate changes in fault level (i.e., changes in source impedance magnitude) for a single infeed, the scheme operates correctly, that is, as observed in Section 7.4.1. If more significant variations in fault level are expected, two SFCL design factors must be considered: the superconductor critical current, and the superconductor length (which typically defines the quenched resistance [BBS+11]).

7.5.2.1 Critical Current

SFCLs must be carefully specified at the design stage to ensure that the critical current value caters for all operating conditions. If the amount of connected

generation changes significantly over time, as could be the case for renewable generation such as wind, it may be desirable to modify the SFCL characteristics to better suit the load current and prospective fault current values. This can be achieved while the SFCLs are in service by varying the operating temperature of the superconductor T_a [OSH$^+$09, BBB12]. For example, at times of relatively low demand, and consequently low levels of connected generation, it may be useful to increase T_a for each SFCL, thereby decreasing the critical current value, as illustrated in Figure 7.1. Regular adjustment of the characteristics of the SFCLs may be particularly relevant in industrial or marine applications.

7.5.2.2 Superconductor Length

In circumstances where the fault level from an infeed is significantly reduced, yet the fault current is higher than the SFCL critical current rating, there is a risk that SFCLs other than those closest to the fault will operate, and this threatens discrimination. Low prospective fault current results in lower energy dissipation in the superconducting elements, and therefore lower superconductor temperature, and lower resistance in the quenched state. Consequently, if the superconductor length is too short, the fault current is not limited sufficiently by the appropriate SFCL(s) and one or more additional SFCL(s), further from the fault, may quench also, resulting in the disconnection of healthy circuits.

Figure 7.11 illustrates this issue for Fault F2, where the fault level contribution for the source at SFCL 1 has been reduced by a factor of 10, and for a reduced superconductor length of 50 m. The lower quenched resistance of SFCL 4, compared to the example presented in Figure 7.7, results in phase B of SFCL 3 quenching. When the superconductor length is restored to 100 m, the CDD scheme operates correctly, i.e., SFCL 3 does not quench, despite the lower fault level.

To avoid this risk, each SFCL must be designed with sufficient superconductor length for appropriate SFCL resistance in the quenched state. Alternatively, CDD should only be applied to highly-interconnected systems where such significant changes in fault level are unlikely.

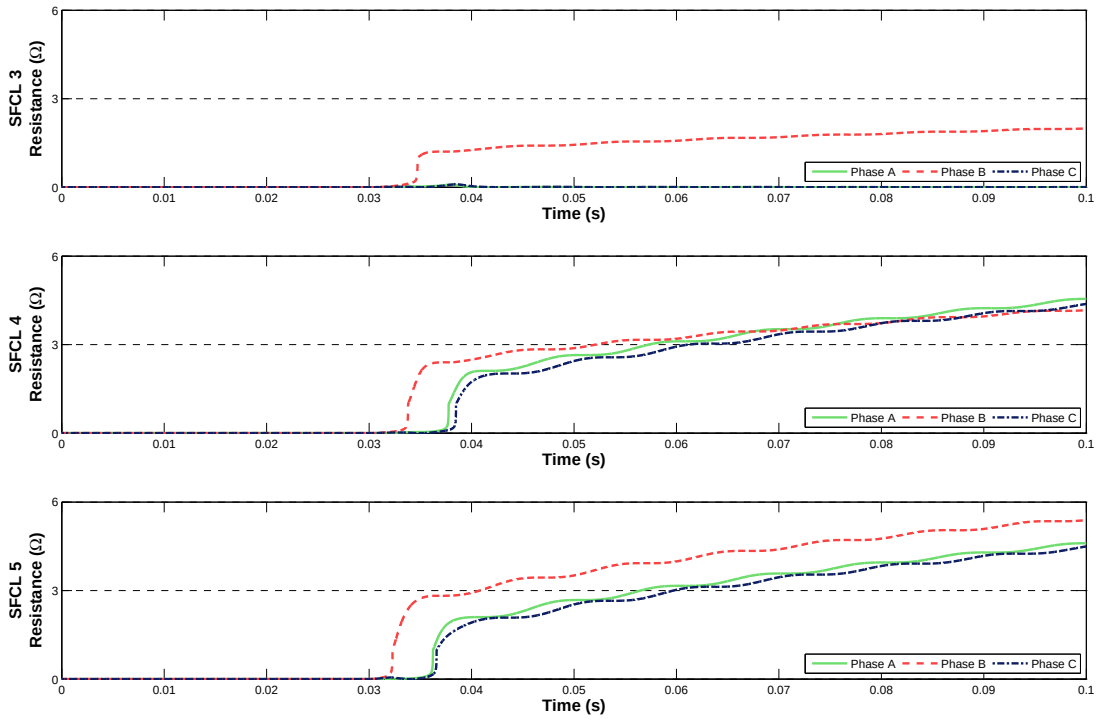


Figure 7.11: Incorrect quench of SFCL 3 for Fault 2, during reduced fault level

7.5.3 Mitigating Resistive SFCL Recovery Time

The fault location scheme described in the chapter permits increased interconnection due to SFCLs reducing fault levels. This means that a faulted circuit section typically can be taken out of service while the SFCLs recover, without undue risk to system security. Furthermore, if the circuit is a cable conductor, the fault is likely to be permanent, requiring repairs that will take far longer than the SFCL recovery time. However, CDD is less suited to overhead lines where autoreclose is commonly used to mitigate the effects of transient faults. The autoreclose dead time (typically 1–5 seconds) is much shorter than the likely SFCL recovery time (typically up to several minutes).

This drawback could be overcome by using a second SFCL (or another FCL device) that could be switched into service during the dead time to replace the quenched SFCL. In compact power systems, such as marine vessels, two or more superconducting devices—which may include SFCLs, motors, generators and cables—could share a common cryogenic system to improve space and weight efficiency [ZD11b]. Alternatively, the quenched SFCLs could be electri-

cally bypassed and protection would rely upon other SFCLs, further from the fault, which did not quench. This would provide a lower standard of protection until all quenched SFCLs recover and can be restored to service. Further work is needed to assess whether or not the improved protection offered by using multiple SFCLs justifies the consequent operational limitations on autoreclose schemes, or whether other types of FCL, which do not require a recovery period, could be used instead.

7.5.4 High-Impedance Faults and Earth Faults

The proposed CDD scheme with SFCLs is aimed at dealing with short-circuit faults that produce excessively high fault currents. It is assumed that without fault current limitation, the power system could not be operated safely in the required manner. For example, it may not be safe to connect DG or to have as many interconnections. However, an SFCL will not quench for fault currents less that its critical current rating. There are practical limits for the critical current of an SFCL to prevent quenching during normal power system transients such as motor starts and transformer inrush, as analysed in Chapter 5.

Therefore, it is not possible to rely upon CDD with SFCLs alone for protection, because SFCLs will not respond to high-impedance faults which produce fault current below the SFCL critical current rating. Furthermore, the use of protection devices with inverse current-time characteristics involves the risk that faults with relatively low fault current can require far longer clearance times and thereby can cause greater damage (i.e., higher I^2t) than short-circuit faults [Lou10], and these faults may develop into high-current short-circuits [SZM+11]. Other well-established techniques, such as voltage-controlled overcurrent and sensitive earth fault protection [Als11], could be employed to address high-impedance fault scenarios. In a scheme with multiple SFCLs, traditional protection could be set to be more sensitive and faster acting than would normally be the case, due to the SFCL operating time being relatively much faster for low-impedance faults. This would be beneficial because high-impedance faults would be cleared more quickly from the system than is presently possible without SFCLs. The stability

of traditional protection to transient phenomena such as motor starts would still need to be accounted for, as discussed in [Bri10].

Many distribution systems are earthed via an impedance and this will limit the earth fault current to a value below the critical current of the SFCL. This is particularly true of high-impedance faults such as a tree branch touching a phase conductor of an overhead line. However, the use of SFCLs and CDD could negate the requirement for impedance earthing, because the SFCLs would inherently limit fault currents for all combinations of phase-phase and phase-earth faults.

7.5.5 Implications of Several Different Types or Designs of SFCL

This study has assumed that all SFCL are identical. Retrofitting or replacing SFCLs may result in SFCLs of different designs being on the same network if, for example, a manufacturer discontinues a particular design. It should also be noted that superconducting materials may contain impurities or defects [ZTE+03] which will affect the current-time characteristics of an SFCL—no two SFCLs will be exactly identical. Further work is needed to examine the effects of a mixture of SFCL designs within the same network, because the SFCLs may have different current-time characteristics, resulting in poor discrimination of fault location.

7.5.6 Application to Networks with Superconducting Cables

Superconducting cables offer attractive benefits of reduced losses [OOLT01] and greatly increased power capacity [OTO99]. It is possible to use the intrinsic fault current limiting properties of superconductors to design a superconducting cable that has a fault current limiting feature such that the cable itself limits fault current through it. This would be particularly advantageous in underground DC superconducting cable networks because DC is more difficult to interrupt than AC, and because the superconductor will not experience AC losses. A network comprising interconnected superconducting cables would therefore possess intrin-

sic CDD protection. Circuit breakers or other means would still be needed to interrupt fault current and provide electrical isolation.

7.6 Conclusions and Recommendations

This chapter has shown that multiple SFCLs are suitable for implementing a fast system-wide fault detection and isolation scheme, without needing communications between substations. This has been demonstrated by applying a thermal-electric SFCL model within a representative distribution system simulation. CDD is especially suited to highly-interconnected utility systems, with significant amounts of DG. Furthermore, the scheme is applicable to marine vessel electrical systems, which are increasingly power-dense and require high power system availability to avoid ship-wide blackouts. Although this chapter has focused on distribution applications, CDD can also be applied to transmission systems, whether AC or DC, and particularly to those involving superconducting cables.

A CDD scheme with SFCLs will limit all sources of fault current, which ensures that no circuit ever suffers its prospective short-circuit fault level. Factors such as fault type, earthing system, and fault point on wave have no significant adverse effects on the scheme. CDD is better suited to applications involving underground cables rather than overhead lines which typically use autoreclose.

Nevertheless, three important practical caveats have been identified in this chapter. First, the fault level must be sufficient to ensure that the prospective fault current exceeds the critical current of each SFCL in the path of fault current. This requires appropriate design of the dimensions of the superconducting elements, and may require online adjustment of the superconductor temperature to fine-tune the critical current. The analysis in Chapter 6 describes a methodology for selecting an appropriate temperature, according to a particular fault current level. Second, for correct discrimination, each bus must have at least three fault current infeeds. The proposed scheme is intended for meshed networks, which usually satisfy this requirement. Third, all SFCLs must have the same current-time characteristic to ensure correct discrimination and location of the faulted

circuit section.

Chapter 8

Conclusions and Further Work

8.1 Conclusions

Chapter 1 presented evidence for the growing need for fault current limitation in present and future power systems. High fault levels are already a challenging issue for system designers and network operators, and this trend is expected to continue in the future due to natural growth in demand, the increasing presence of DG, increased interconnection, and the growing interest in multiterminal DC systems.

Chapter 2 introduced power system protection, and described the relevant protection needs for utility distribution and marine vessel systems. The benefits and difficulties associated with increased interconnection and greater penetration of DG have been emphasised. The high power-density and safety-critical nature of full-electric marine vessels demands ever more stringent protection systems.

An overview of fault current limitation has been provided in Chapter 3, with a focus on the operation, benefits, and present status of resistive SFCLs. Chapter 4 elaborates on this topic to highlight the challenges associated with the application of resistive SFCLs. In particular, it has been shown that there are compromises based on the SFCL location and quenched resistance rating, and there are issues relating to the recovery period and the interaction of SFCLs with conventional protection systems.

Following on from these challenges, Chapter 5 establishes guidance on the interaction of the following resistive SFCL design factors: quenched resistance; shunt resistance; the level of fault current limitation; and the expected energy dissipation, and hence the recovery time. There is a compromise between a shorter recovery time, which is desirable, and the cost of the volume of superconducting material needed for the resistance required to achieve a shorter recovery time. A generic methodology has been proposed for easily validating the design of a resistive SFCL, and this method has been shown to successfully validate work by other researchers.

If SFCLs are to play a role in future electrical systems, it is important to understand their dynamic characteristics. This will allow the behaviour of multiple SFCLs in a system to be fully understood during faults and other transient conditions, and will allow SFCL behaviour and impact to be taken into account when coordinating network protection systems. Chapter 6 provides this knowledge by analysing the current-time characteristics of resistive SFCLs.

Chapter 7 builds on the contributions of Chapter 6 to propose a novel protection scheme involving multiple resistive SFCLs, dubbed current division discrimination (CDD). CDD offers a number of very compelling advantages which, despite the relatively high cost of SFCLs, merit serious consideration for the design of any new power system. These advantages are:

- Sub-cycle response to faults.
- Automatic isolation of the minimal faulted circuit, or "zone", without communications.
- Automatic backup if an SFCL is out of service.
- The scheme remains applicable if the electrical network topology changes.
- No circuit which is protected by SFCLs ever experiences its full short-circuit fault current, which encourages the use of meshed systems and the connection of DG, and potentially allows circuit breakers with a lower rating to be used (thereby avoiding or reducing replacement costs). A highly-meshed

power system can help mitigate the recovery period of resistive SFCLs because alternate paths for load current may be available, whilst the quenched SFCLs are disconnected following a fault.

- The scheme has the potential for online adjustment of the SFCL operating threshold to cater for different network configurations and varying fault levels.

The operation of CDD has been analysed under a number of network scenarios and several application recommendations have been established. Nevertheless, the scheme is a relatively radical approach to protection—and protection is, understandably, a conservative field.

This thesis has established and reviewed the state of the art in resistive SFCL technology and knowledge, and has provided research-based guidance which will be critical for the application of resistive SFCLs in future power systems.

8.2 Further Work

8.2.1 Further Analysis of CDD

The potential benefits of a CDD scheme with resistive SFCLs demands further study, and merits a laboratory or field trial with multiple SFCLs. In particular, the conditions where the scheme may result in the quenching of more SFCLs than needed to isolate the fault, as discussed in Section 7.5.2, should be quantified. A trial will ensure that a CDD scheme is effective despite slight differences in SFCL characteristics, due to impurities in the superconducting materials.

The impact, if any, of resistive and inductive shunts on the operation of CDD should be investigated. It is of particular interest whether or not a variable shunt impedance can yield any advantage for dynamically altering the current-time characteristics of a resistive SFCL. The effects of temperature on resistive shunts must be considered. Furthermore, the applicability of CDD across different voltage levels, and the requirements for SFCL current-time characteristics, should be investigated.

The use of CDD in DC systems is of considerable interest, particularly for offshore multiterminal systems where protection and fault current interruption will prove very challenging [JvHL+11]. As noted in Section 7.5.6, CDD may be applicable to networks with AC or DC superconducting cables, and this also merits further investigation.

8.2.2 Integrated SFCL Analysis and Design Tool

The analysis work in Chapter 5 could be combined with the resistive SFCL current-time characteristic tool presented in Chapter 6. The unified software tool should allow the effect of any resistive SFCL parameter to be investigated and visualised. Work by other researchers could be integrated for finding optimal SFCL parameters to automatically—and with confidence—satisfy the requirements of a particular SFCL installation. It would also be valuable for the tool to assess the likely effect of specific SFCL parameters on regulatory limits for system voltage during and following faults.

8.2.3 Centralised Protection

The difficulties involved with protecting marine vessel systems, as identified in this thesis, has prompted research into alternative protection methods which require a central device to detect and locate faulted circuits [MGBM05, TM06, BES+08]. In particular, the protection schemes proposed in [BES+08]—in contrast with conventional differential protection—do not require very low-latency communications and are tolerant of jitter. Further research is needed to fully evaluate these centralised protection schemes, particularly for power systems with SFCLs.

8.2.4 SFCLs and Arcing Faults

Fault current limitation may help extinguish arcs present at the point of fault due to the reduced arc current, thereby clearing arcing faults without the need for a circuit breaker. Work is needed to assess the feasibility of this, and to determine if this method conflicts with traditional autoreclose schemes. For example, this

may reduce the potential for multi-shot autoreclose schemes to "burn out" semi-permanent faults.

8.2.5 Analysis of Characteristics of Different Types of FCL

The work in Chapters 6 and 7 only applies to resistive SFCLs. The application of this methodology is of interest for other FCL types, such as the pre-saturated core SFCL. Some work exists in this area for inductive SFCLs [MM08, ZD11a].

8.2.6 Faster-Acting Backup Protection with Multiple SFCLs

It has been proposed in Chapter 7 that, in the presence of primary protection using multiple SFCLs, the operating times of backup protection could be improved—without sacrificing coordination. This may apply to voltage-controlled overcurrent protection and earth fault protection. The feasibility and potential caveats of this should be investigated.

Appendix A

Literature Review: Modelling Resistive SFCLs for Power System Applications

A.1 Introduction

This appendix reviews the different types of resistive SFCL models that are described in the literature, and highlights those which are practical for power system simulation studies.

A.2 Simplified Models

A.2.1 Without SFCL Recovery

Reference [SB08] describes two simple methods for modelling resistive SFCLs for power system studies: a "binary" model, and a non-linear look-up table of resistance values. The binary model involves switching a resistance into the system immediately after a fault occurs. This is useful for estimating the steady-state reduction in fault current, but does not faithfully represent the dynamic characteristics of superconductors; the superconductors will take a finite time to heat up

and thereby develop resistance. This model will tend to overestimate the reduction in peak fault current and lead to inaccurate transient results until the final SFCL resistance value is reached. The non-linear look-up table method (used in [STB+10, ETS+10, BBE+10]) attempts to correct this shortcoming by dictating the value of an SFCL's resistance over time. This technique is introduced in [Smi07], where a generic quench characteristic equation has been established:

$$R(t) = R_{max}\left(1 - e^{\frac{-t}{\tau}}\right) \tag{A.1}$$

where R_{max} and τ define the properties of the curve. This is known an "exponential" SFCL model type. Values for τ, for a given prospective fault current magnitude and the initial superconductor temperature, are suggested in [Smi07], and have been obtained from experimental data of a MgB_2-based SFCL prototype. Similar exponential curves are described in [MDN+03, LCH06, LKY06, KVJM+08, SSLC09], where [LKY06] proposes a similar equation for approximating the recovery time. This is useful for a first order approximation, with low computational requirements, of the likely effect of a resistive SFCL in a power system. However, this approach does not "automatically" react to fault currents; it must be programmed to enter the resistive state at a specific time in a simulation. This is inconvenient, but moreover it leads to uncertainty as to precisely when the quenching should be initiated relative to the inception of the fault, for each phase. If the type of fault or the fault impedance is changed, then the SFCL model must be reconfigured.

In order to avoid this drawback, the quenching process can triggered when the instantaneous current in each phase first exceeds the critical current value, I_c [OSH+09]. Hence, the SFCL model intrinsically reacts to the current magnitude in each individual phase and does not have to be configured to operate at a specific time [BBE+11]. The model is thereby effective at estimating the peak fault current reduction, yet it avoids the complexities of thermal-electric models such as those described in [DYF+08], [PCL+00], and [LSW+05].

Equation A.2 describes the modified exponential model, where: R_0 is the maximum SFCL resistance value; τ is the time constant which determines how

quickly the SFCL reaches R_0; and $i(t)$ is the instantaneous phase current in the SFCL.

$$R_{SFCL}(t) = \begin{cases} 0, & \text{before } |i(t)| < I_c \\ R_0 \left(1 - e^{\frac{-t_0}{\tau}}\right), & \text{after } |i(t)| \geq I_c \end{cases} \tag{A.2}$$

where the process is initiated when the phase current exceeds the critical current:

$$t_0 = t - t_{|i(t)| \geq I_c} \tag{A.3}$$

For this model, the typical per-phase SFCL resistance characteristic and the effect on fault current, for τ=0.01 s and R_0=0.1 Ω, are illustrated in Figure A.1. Note that any current transient which exceeds I_c will trigger the quench operation of this model.

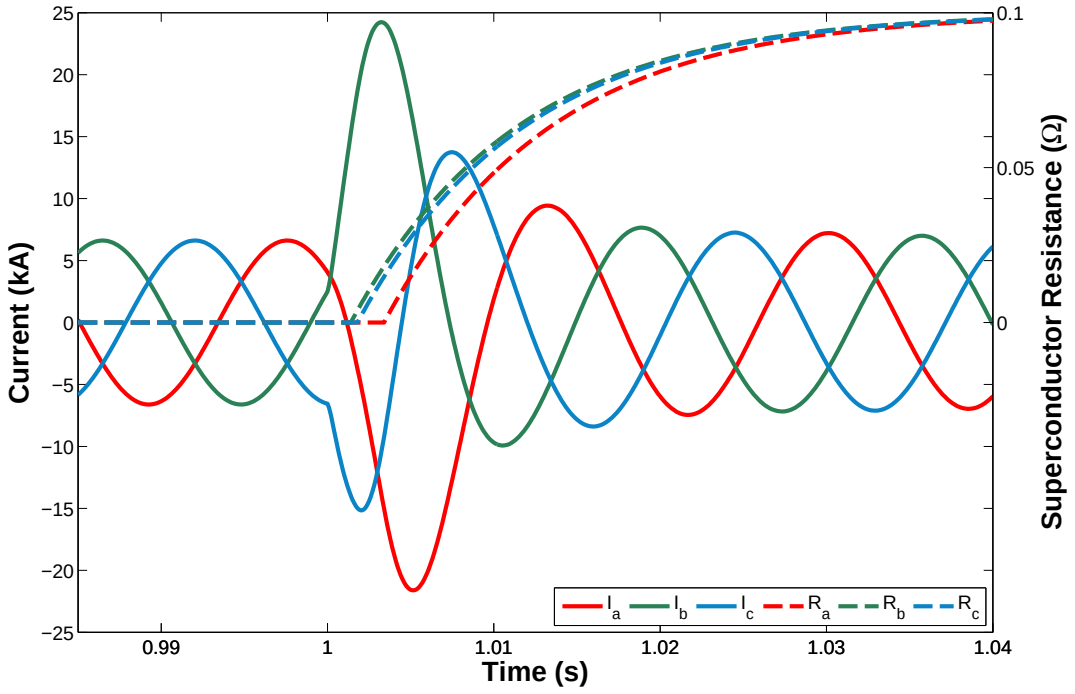


Figure A.1: Typical per phase SFCL resistance characteristic and effect on fault current

Another model is proposed in [YXWZ05], and relatively simple equations are provided for estimating the resistance of the superconductor depending on the state of the superconductor: flux-creep, flux-flow, or normal conducting.

Clearly, these simplified methods do not model the thermal-electrical properties of superconductors, and do not cater for the following phenomena:

- As the fault current increases, the proportion of energy dissipated into the cryogenic environment tends to decrease [KJKK+05, DYF+08], hence increasing the rate that resistance is developed in the superconductor.
- The resistance of the superconductor will continue to increase due to heating after quenching, until the resistive SFCL is disconnected from the system.
- In most cases, the superconductor recovery period is not modelled.
- Current in an AC power system is sinusoidal, and hence ohmic heating in the superconductor will be cyclic (i.e., two half-cycle "pulses" during each current cycle, ignoring the decaying DC offset which may be present during a fault), which should result in minor "dips" in an SFCL's temperature and resistance during the quenching transition. This effect can be seen in [WCC+99] and [KKH+05].
- Design factors, such as increasing the superconductor length to increase the quenched resistance, will affect the thermal properties of the superconductor.

Nevertheless, the main motivation for using an exponential type of resistive SFCL model is the simplicity and the close fit with empirical quenching results, as given in [Smi07].

A.2.2 With SFCL Recovery

Reference [Dud04] presents a model which uses a current threshold to activate the SFCL resistance, as shown in Figure A.2. The resistance value increases or decays linearly, according to configurable time constants. Although very simple, this model can represent the recovery time, and it automatically reacts to the current magnitude applied to the model. A similar model is presented in [SKR+10b] and [KT99, KT08].

A possible improvement to this model is to make the recovery time depend on the total energy absorbed during the resistive mode. This type of "macroscopic" model avoids the complicated thermal and physical aspects of a real SFCL device; hence there are fewer parameters to configure. Nevertheless, the disadvantages discussed in Section A.2.1 still apply.

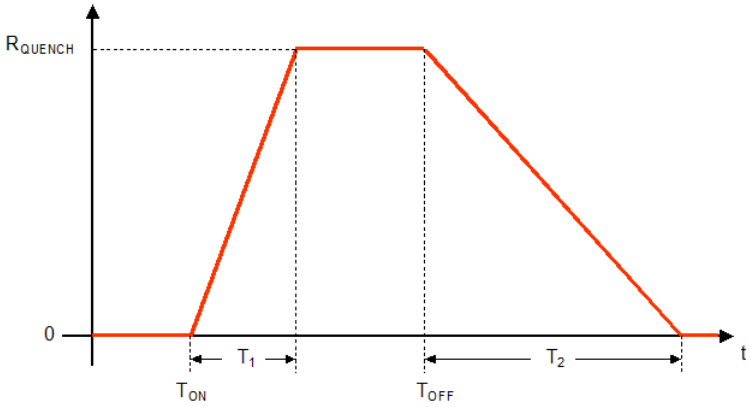


Figure A.2: Resistance characteristic for the model in [Dud04]

A.3 Hardware in the Loop Models

References [KPK+07, KPA+08] describe an experimental apparatus which allows for power system simulation studies to incorporate an SFCL or a superconducting cable. The arrangement involves a real-time digital simulator (RTDS), and a hardware superconductor wire. A current amplifier takes an output signal from the RTDS and passes the corresponding current through the superconductor wire. The wire's resistance is measured, and this value is fed back into the RTDS simulation. This approach will accurately represent the dynamic properties of the superconductor, including the recovery characteristics. The limitations associated with having access to a superconducting wire and the associated cooling system make this type of model suitable only for verification purposes. This method does benefit from the merits of the RTDS's real-time execution; other hardware devices such as protection relays can also be tested, which is potentially more realistic than using purely software models. A similar hardware in the loop arrangement is described in [SLSN09].

A real-time hardware in the loop demonstration, scaled for testing purposes, of a superconducting cable is presented in [DJK+12].

A.4 Neural Network Models

Reference [MSH07] demonstrates that it is possible to model the non-linear, multi-variable nature of a superconductor using a constructive neural network (CNN). However, this type of model must be trained with suitable data. Obtaining this data may be difficult, and the CNN may have to be re-trained for different parameters, e.g., for different values of superconductor length. These models are thereby impractical for power system studies.

A.5 Finite Element Analysis Models

Several resistive SFCL models have been developed using detailed finite element analysis (FEA) [LM97, KJKK+05, DGA+06, DDG+07, DGA+07, OLVV08, TDC+07, RDGS08, GBM07, SO03, FSS08].

Due to the time consuming process of implementing such a model, the specialised software which is needed, and the relatively long simulation times, this approach is not suitable for power system simulation studies. Nevertheless, the results from the existing FEA models can be used to help verify other models, as demonstrated in [CM13].

A.6 Thermal-Electric Models

A thermal-electric SFCL model must consider two, inter-related physical phenomena [DDG+07]: the thermal characteristics, and the electrical characteristics. For an FEA approach, references [TDC+07, DGA+07, DDG+07] note that there are two ways to couple the potentially complicated interactions between the thermal and electrical sub-systems:

1. Combined, and solved as one complex system.

2. Solved independently; the outputs from one sub-system are used as the inputs to the other sub-system, where this process alternates each time step.

The "power-law" is commonly used to describe the non-linear relationship between electric field and current density in Type-II superconductors [PCL+00, SGD+02]:

$$E = E_c \left(\frac{J}{J_c(T)} \right)^n \tag{A.4}$$

where n is known as the n-value of the superconductor, which defines the "sharpness" of the superconducting-state to normal-state transition. J_c is the critical current density which is defined as the current density when $E = E_c = 1$ $\mu V/cm$; $J_c(T)$ hence models the temperature dependence of J_c. References [PCL+00, SGD+02, CTWC02, Muk03, SO03, YJ04, vWvdEW+05, YC06b, Sut06, TDC+07, OLVV08, Mal08, Elm09, SH09, dSPS+12, CD12] have developed SFCL models based on the power law equations, or variations.

The equations in [PCL+00], which are based on a BSCCO "Bi-2212" superconductor, define the how the electric field varies with current density, recognising that this characteristic depends on the state of the superconductor (flux-creep, flux-flow, or normal conducting). Figure A.3 illustrates the typical relationship between electric field, E, and current density, J, for these three states. Note that, after entering the flux-flow state, the superconductor heats up significantly, which in turn shifts the E-J curve to the left; i.e., E increases further. The superconductor will enter the flux-flow state at J_0 (and at the corresponding E_0 value) which will be a larger value than J_c [PCL+00]. The model is demonstrated to fit well with experimental results.

A differential equation is given in [PCL+00] to calculate the heat diffusion from the superconductor into its liquid nitrogen bath. The models in [YJ04, YC06b, Elm09] are based on power law equations, but they assume an adiabatic thermal process; however the thermal transfer to the coolant should not be ignored, as shown in [DYF+08]. A simplified, yet practical, thermal model (compared to

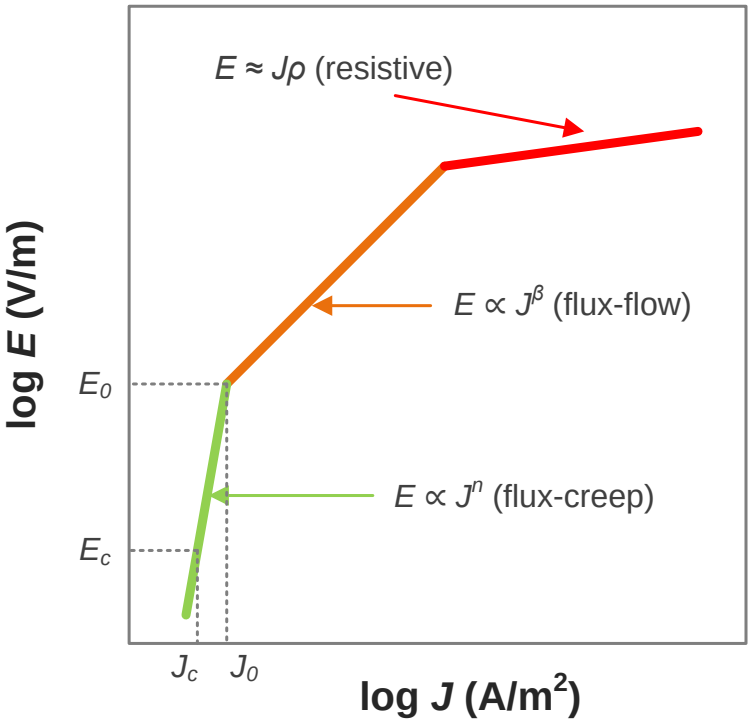


Figure A.3: Superconductor E-J characteristic (from [PCL+00])

equation provided in [PCL+00]) is introduced in [LSW+05], which can be combined with the $E - J$ equations established in [PCL+00]. This provides a good compromise on accuracy, complexity, and execution speed, and is therefore used as the basis for resistive SFCL modelling in Chapters 6 and 7 of this thesis.

The model proposed in [PCL+00] and [LSW+05] does not consider vaporisation of the coolant, or phenomena such as the "film boiling" effect (also known as the Leidenfrost effect, which normally follows a period of "nucleate boiling") where sudden changes in temperature reduce the efficiency of the thermal transfer due to a vapour film, as demonstrated by [KJKK+05, DYF+08, NKL+06, ZTE+03, DGA+07, RDGS08, WCC+99]. In particular, [DGA+07] offers an equation for calculating the heat transfer coefficient; however, the authors state that this value has negligible effect on the electrical sub-system, i.e., that the adiabatic model matches their non-adiabatic model. This result may be valid during the quench, but the thermal sub-system should be non-adiabatic in order to model superconductor recovery.

This model assumes a uniform temperature across the length of the superconducting material, and therefore assumes a uniform J_c value, i.e., that quenching will always occur at a particular temperature. In reality, the superconductor temperature is not uniform, and J_c will depend on the presence of defects in the superconductor (which can cause "hot spots") and the relative position of the cooling head of the cryogenic system [KLR06, CKY+09].

Furthermore, in [LSW+05] and [SB08] the coolant is assumed to be a perfect heat sink; the coolant is assumed to absorb energy without a change in its ambient temperature. To be more realistic, the "ambient" temperature of the coolant should increase after the onset of the fault (which will lessen the film boiling effect), and the cryogenic control system should then act to correct this change, albeit very slowly relative to the time taken for the superconductor to quench. During a quench, the temperature at the surface of the superconductor will be hotter than the temperature elsewhere in the coolant, until the temperature equalises (assuming the SFCL is removed from the circuit, and hence there is no current flow).

A model using a similar, but simplified, thermal approach to [LSW+05] is presented in [HS08]. However, the model calculates the heat dissipated into the coolant differently: it is based on predetermined values for the time of the fault and the total simulation time, rather than dynamically calculating the heat dissipation at run-time. Hence, the model in [HS08] is not as generic as that in [LSW+05], because it is scripted rather than intrinsically reacting to faults. The model does, however, offer an analytical equation for calculating the SFCL resistance (as derived in [SYG+03]), which differs from the typical power-law approach.

The superconductor in a resistive SFCL is often bonded to another non-superconducting shunt conductor, and therefore the shunt resistance and thermal interaction should also be modelled. This is described in references [vWvdEW+05] and [LSW+05]. As noted in [LSW+05], it may be necessary to model the effect of an external resistive shunt heating up during a fault, because temperature will affect its resistance.

Reference [DYF+08] approximates the variation of superconductor resistivity with temperature, by a quadratic equation. This was obtained by applying a constant DC current of known magnitude through a superconducting wire, and measuring the temperature and resistance of the wire. The authors explain that the heat initially leaves the superconductor wire by conduction, and then (after approximately 0.35 s) by convection; however, the authors only investigated the conductive period. Hence, a model that accurately represents the recovery of the superconductor should consider both conductive and convective heat transfer; this approach is considered in [BAD10]. An important result from [DYF+08] is that the proportion of energy that is dissipated into the coolant during a quench lies between 30-60% of the total energy. Although this value varies with time and current, it can be used as a guide for verification of other models.

The authors of [BAD10] argue that the superconductor heats up slowly, relative to electrical transients, and therefore the temperature does not need to be updated as often as in other models; however this is not fully justified because the comparison between this model and the experimental results is obscured during the first cycle. Hence, it is difficult to verify whether or not the assumption of an adiabatic system is valid during the initial stages of the fault. Reference [DGA+06] compares the rise of temperature with current during a quench, and shows that the temperature rise may lag the changes in current by approximately 1-2 ms. In addition, although the authors of [BAD10] mention film boiling, the model does not appear to account for this, and a constant value for the convection coefficient has been used.

The model presented in [Mal08] attempts to model the thermal characteristics of an SFCL, using a pseudo-FEA approach. The superconductor is "sandwiched" between two stainless steel plates. The superconductor and steel sections are divided into layers (a similar layered approach for modelling the heat flow into the substrate is described in [WCC+99]). Each layer has a particular temperature, which is assumed to be the same value across the entire area of the layer; the outer-most layers of steel (which are in contact with the coolant) have a constant temperature of 77 K. The overall temperature of the superconductor is the

mean of the layer temperatures. The flow of heat between layers is modelled, taking into account the thermal conductivity of the two different materials. The $E - J$ behaviour is based on the power law equations, except that the variation of temperature is ignored. In addition, the resistivity look-up table is simplified to depend only on temperature (but not current density). The model also ignores the parallel resistance of the steel shunts, and assumes that the current only passes through the superconductor. Two sides of the superconductor are presumably also in contact with the coolant and the resulting thermal transfer should be considered. Nevertheless, the model, although simplified, can represent the recovery of the superconductor, and avoids the problem of the difficulty of specifying the thermal convection coefficient, because the heat sink is a solid, in this case steel, rather than a liquid or a gas.

Reference [VS05] describes an analytical approach for modelling the critical current which is dependant on temperature, and hence the SFCL's resistivity can be calculated as a function of current and temperature. The model is used in the context of an inductive SFCL, but the equations could be modified for a resistive device. The thermal system is modelled using the conservation of energy equation; a similar approach is used in [MBLR05].

Reference [OBF$^+$08] provides a thermal model for an SFCL using a thermo-acoustic refrigerator.

An MgB_2 SFCL model is described in [BHH$^+$11], but the model does not implement a full thermal system, and is therefore only suitable for simulating relatively high fault currents, where quenching is guaranteed.

Appendix B

Analysis of Transient Recovery Voltage with Resistive SFCLs

B.1 Introduction

Switching events cause transients in any electrical circuit with reactive impedance. In power systems, circuit breakers experience a transient recovery voltage (TRV) across their terminals when opened, i.e., when current is interrupted at a current zero-crossing [HKLS83]. TRV is developed immediately after the arc between the circuit breaker terminals is extinguished [Col72], and is typically in the form of high frequency (relative to the fundamental system frequency of 50 Hz or 60 Hz) oscillations superimposed on the system voltage. These oscillations decay over time due to resistive damping in the system. TRV is clearly undesirable because the increased voltage may cause a restrike, resulting in re-ignition of the arc and failure to interrupt the fault current [SSHL95]. Furthermore, circuit breakers are usually opened in order to clear a fault, so there is already a significant disturbance to the system. This appendix analyses the effect of resistive SFCLs on TRV.

B.2 Background

Although the benefits of an SFCL on circuit breaker transient recovery voltage (TRV) have been shown in the literature [STB+10, LMCC07, ASPC06, ZJ09], the phenomenon has not been analysed fully for resistive SFCLs. References [CYS+02, DCP07, QHJL08, LLZS09] analyse how inductive SFCLs can reduce TRV. Reference [CYM05] considers resistive SFCLs, and evaluates the required limiting impedance for successful current interruption, assuming the SFCL is downstream of the circuit breaker. The following sections analyse the effect of an SFCL on TRV, when the SFCL is both upstream and downstream of the circuit breaker.

B.3 Analysis

The procedure in [Cho96] can be followed to determine an equation for circuit breaker TRV, with and without a resistive SFCL. A simplified circuit diagram is shown in Figure B.1. The circuit breaker is opened at a current zero-crossing shortly after the fault occurs. The SFCL is assumed to be located upstream of the circuit breaker. The system is described by Equations B.1, B.2, and B.3, where $v(t)$ is the source voltage and Z_f is the system impedance during the fault (while the system capacitance is shorted).

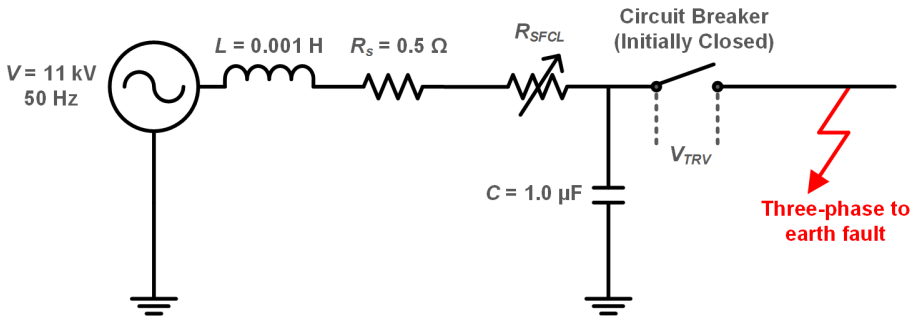


Figure B.1: Circuit used to examine effect of SFCL on TRV

$$v(t) = \hat{V} \sin(\omega t) \tag{B.1}$$

$$Z_f = R + j\omega L = R + sL \tag{B.2}$$

$$R = R_s + R_{SFCL} \tag{B.3}$$

The steady-state fault current, $i_f(t)$, is defined in Equation B.4, where ωt_0 represents the current phase offset, t_c is the time the fault is cleared, $\phi = \tan^{-1}\left(\frac{X}{R}\right)$, $X = \omega L$, and $|Z_f| = \sqrt{R^2 + \omega^2 L^2}$.

$$i_f(t) = \frac{\hat{V}}{|Z_f|}\sin\left(\omega t + \omega t_0\right) \tag{B.4}$$

$$t_0(t) = t_c - \frac{\phi}{\omega} \tag{B.5}$$

A value of $t_c = \frac{\phi}{\omega}$ in Equation B.5 ensures that the current is interrupted at a zero-crossing.

The Laplace transform of Equation B.4 is given in Equation B.6.

$$i_f(s) = \frac{\hat{V}}{|Z_f|}\left[\frac{s\sin\left(\omega t_0\right)}{s^2+\omega^2} + \frac{w\cos\left(\omega t_0\right)}{s^2+\omega^2}\right] \tag{B.6}$$

When the circuit breaker is opened, the reflected current, $i_r(s)$, is equal to the negative of the fault current; that is $i_r(s) = -i_f(s)$. The TRV of the circuit breaker is calculated from the product of reflected current and the impedance looking into the (open) circuit breaker terminals, as given in Equation B.7.

$$\begin{aligned} V_{TRV}(s) &= i_r(s)\, Z_{open}(s) && \text{(B.7)} \\ &= -\frac{\hat{V}}{|Z_f|}\left[\frac{s\sin\left(\omega t_0\right)}{s^2+\omega^2} + \frac{w\cos\left(\omega t_0\right)}{s^2+\omega^2}\right]\frac{1}{\frac{1}{R+sL} + sC} && \text{(B.8)} \end{aligned}$$

where

$$Z_{open}(s) = \frac{1}{\frac{1}{R+sL} + sC} \tag{B.9}$$

Equation B.8 can be converted to the time domain using a package such as MATLAB.

B.4 Results

Figure B.2 compares the TRV for an SFCL with 1.0 Ω of resistance to the TRV without an SFCL. The plots begin at the instant when the phase A circuit breaker opens. The analytical results have been confirmed by simulating the circuit given in Figure B.1, using PSCAD. The results are also shown in Figure B.2. A very small time-step, in the order of 10 ns, is needed to ensure that the relatively high-frequency TRV is captured correctly. Similar to the analytical method, the circuit breaker model in the simulation requires a current zero-crossing before opening its contactors.

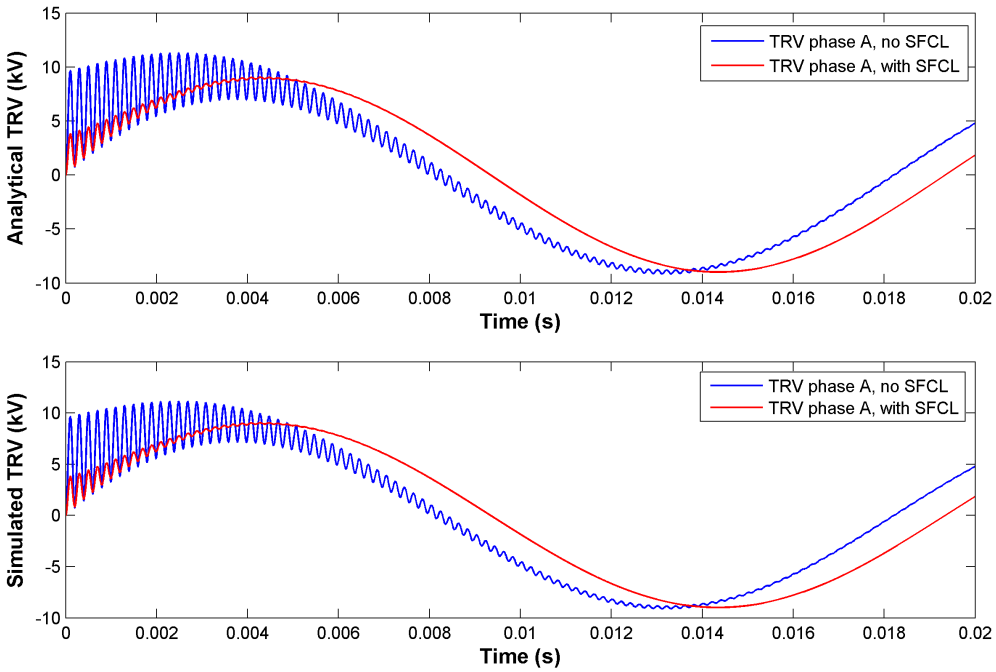


Figure B.2: Effect of SFCL on TRV (analytical and simulated)

Note that the current zero-crossings occur at different times, relative to the source voltage waveform, because the current phase angle (i.e., ϕ) is affected by the SFCL's resistance. Therefore, with the SFCL, the current-zero crossing occurs earlier, due to the additional resistance in the circuit. This is illustrated

in Figure B.3. Similar TRV waveforms are experienced for phases B and C. The resonant frequency of the TRV is $f_0 = \frac{1}{2\pi\sqrt{LC}} = 5.03$ kHz.

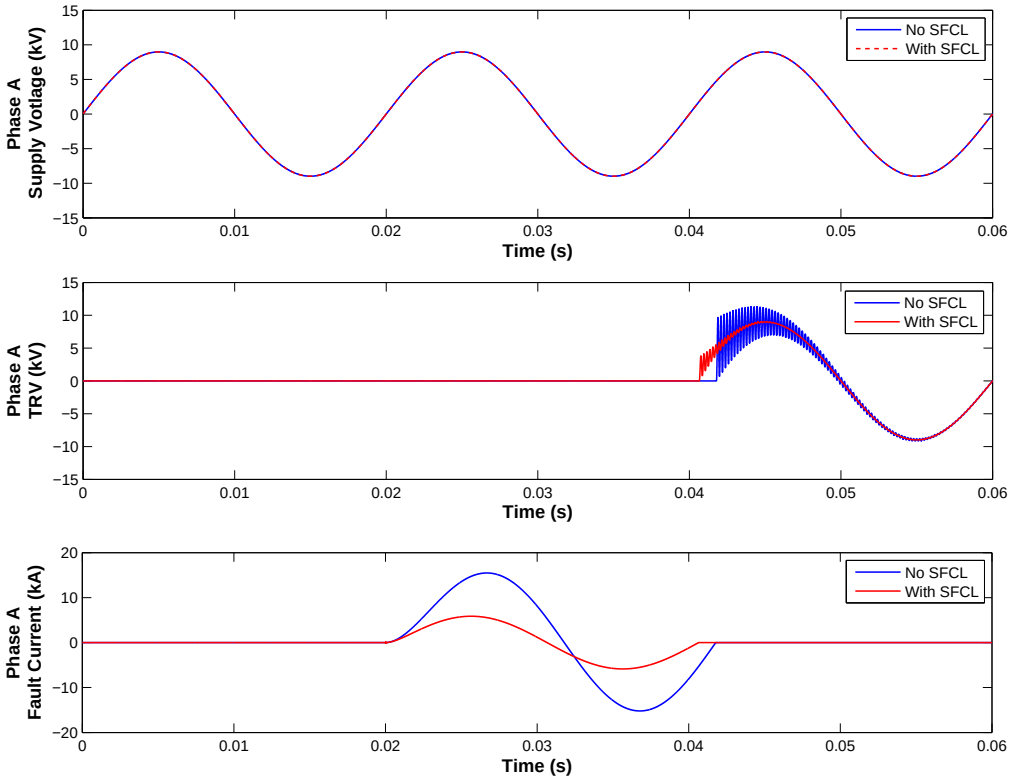


Figure B.3: System voltage, TRV, and fault current (with and without SFCL)

The SFCL may also be located downstream of the circuit breaker, as shown in B.4. Figure B.5 illustrates the difference in TRV for each SFCL location, relative to the circuit breaker. These results illustrate that a resistive SFCL upstream of the circuit breaker will increase damping which causes the TRV to decay earlier than without the SFCL. The initial TRV magnitude is not affected. Therefore, there is some benefit to having a resistive SFCL upstream of the circuit breaker, which is contrary to the advice in [ASPC06]. The significance of this benefit will depend on the specific impedance values for a given system.

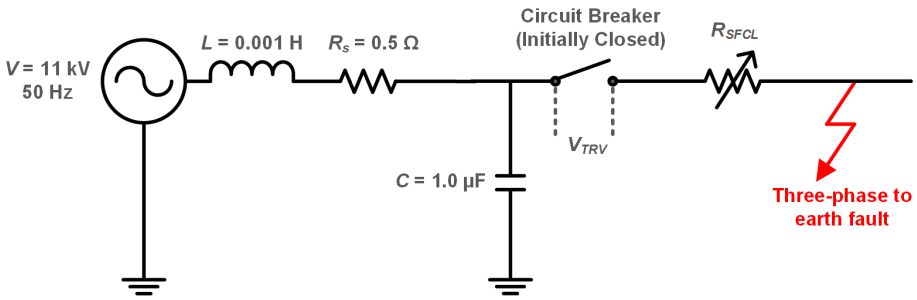


Figure B.4: SFCL located downstream of circuit breaker

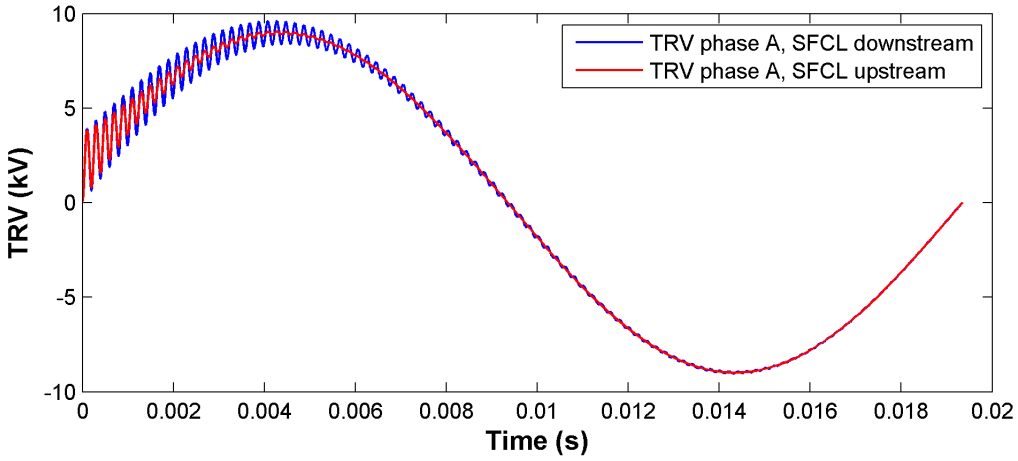


Figure B.5: TRV for SFCL location relative to circuit breaker

B.5 Assumptions

The following assumptions have been made in this analysis:

- The SFCL fully quenches rapidly and can be modelled as a constant resistance. This is a reasonable assumption because the SFCL should be rated to quench well before the typical operation time of a circuit breaker [ASPC06].
- No load is connected to the system.
- The system impedances are lumped as R, L, and C values.
- The circuit breaker waits until a current zero-crossing before opening. The analytical model is also valid for other values of t_c, such that the circuit

breaker does not operate on the current zero-crossing; this has been verified in simulation. The TRV will be significantly higher in these cases.

- For simplicity, the steady-state fault current is used in the analysis; i.e., the fault current is assumed to reach its steady-state value before the circuit breaker is opened. For the values used in this example, this simplification has no effect on the TRV waveform because the time constant (X/R), which dictates the maximum magnitude and decay of the DC component of the fault current, is small.

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