DIGITAL RF MULTIPLEXING FOR A TVWS TRANSCEIVER IMPLEMENTATION

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Abstract. Future devices operating in the TV white space (TVWS) spectrum will require to access different bands at different locations and times in order to avoid interference to incumbent users, requiring agility and sufficient spectral masks to satisfy regulators. In order to realise radio devices capable of this, we briefly review design efforts on a radio transceiver capable up- and downconverting the 40 8MHz TVWS channels residing between 470MHz and 790MHz. While we briefly address the overall proposed structure, the aim of this contribution is to address the practical issues of interfacing data conversion devices sampling at RF to state-of-the-art FPGAs which can then perform the digital operations required for up- and downconversion.

Introduction. Many filter bank schemes currently evolving in the context of frequency agility and cognitive radio [1] are located in the baseband. With substantial progress in the area of analogue-to-digital (ADCs) and digital-to-analogue converters (DACs), see e.g. [2], the idea of operating a filter bank receiver up to radio frequency is appealing and could yield frequency agility and flexibility required of future TVWS devices. Efforts to create such a filter bank based transceiver experience a bottleneck at the RF end, where data at high sampling rates needs to be exchanged between conversion devices and the computational devices executing the digital up- and downconversion, such as field programmable gate arrays. Below, we highlight an approach that permits data exchange between the RF domain sampled at 1.92Gsps and an FPGA device. The lower limit on K is imposed by the permissible input rate of an FPGA, while an upper limit is presented by the number of input channels within in FPGA.

Overall System. The proposed transceiver uses a two-stage design as shown in Fig. 1, with 40 8MHz channels on the left converted to a 1.92Gsps signal that is fed into the DAC/ADC on the right. The important components are the multiplexing devices next to the DAC/ADC which will create the polyphase signals for the polyphase filter (PPF). For implementational flexibility, we here consider a parameterised filter bank with different decimation ratios in stage one (PPF) and stage two (the filter bank multicarrier system, FBMC).

Multiplexer. A standard hardware multiplexer permits 8 polyphase components, while the system considered needs to enable $K = \{3, 4, 5\}$ polyphase components. The proposed architecture is outlined in Fig. 2, and enables the conversion in the receiver by means of a TDL line that is filled at a rate of 1.92/8 Gsps, buffered at $1.92/L$ MHz and emptied at a rate $1.92/K$, with L the least common multiple of 8 and K. A dual structure operates in the transmitter.

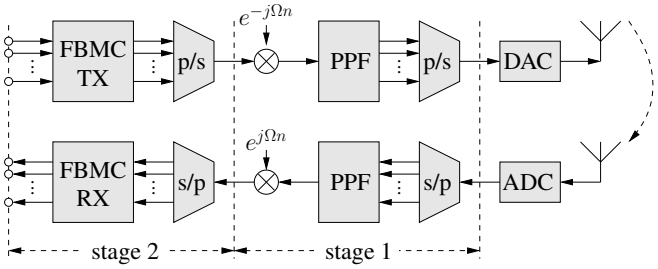

Fig. 1. Proposed multi-stage TVWS filter bank transmitter (above) and receiver (below) with a polyphase filter (PPF) in stage 1 and an FBMC modulator in stage 2.

Conclusion. This abstract has described a hardware multiplexer as part of a flexible TVWS transceiver. It bridges the gap between digital RF and FPGA, interfacing the latter with acceptable rates and numbers of polyphase components.

References

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[3] S.J. Shellhammer, A.K. Sadek, and W. Zhang, "Technical challenges for cognitive radio in the TV white space spectrum," in *Inf. Theory Appl. Workshop*, pp. 323–323, Feb. 2009.

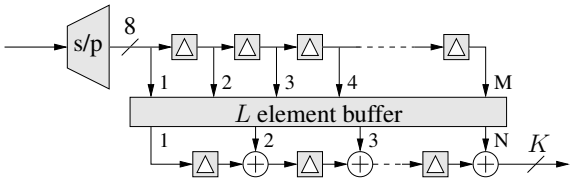

Fig. 2. Flexible hardware multiplexer for receiver, allowing $K = \{3, 4, 5\}$ polyphase components to be created from an 8 channel multiplexer, with $\{M, N\}$ s.t. $L = 8M = KN$.