Fusion Engineering and Design xxx (2012) xxx–xxx

Contents lists available at SciVerse ScienceDirect

Fusion Engineering and Design

journal homepage: www.elsevier.com/locate/fusengdes

# A user configurable data acquisition and signal processing system for high-rate, high channel count applications

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ARTICLE INFO

*Article history:*
Available online xxx

*Keywords:*
Data acquisition
DSP
FPGAs
Reconfigurable

ABSTRACT

Real-time signal processing in plasma fusion experiments is required for control and for data reduction as plasma pulse times grow longer. The development time and cost for these high-rate, multichannel signal processing systems can be significant. This paper proposes a new digital signal processing (DSP) platform for the data acquisition system that will allow users to easily customize real-time signal processing systems to meet their individual requirements.

The D-TACQ reconfigurable user in-line DSP (DRUID) system carries out the signal processing tasks in hardware co-processors (CPs) implemented in an FPGA, with an embedded microprocessor (μP) for control. In the fully developed platform, users will be able to choose co-processors from a library and configure programmable parameters through the μP to meet their requirements.

The DRUID system is implemented on a Spartan 6 FPGA, on the new rear transition module (RTM-T), a field upgrade to existing D-TACQ digitizers.

As proof of concept, a multiply-accumulate (MAC) co-processor has been developed, which can be configured as a digital chopper-integrator for long pulse magnetic fusion devices. The DRUID platform allows users to set options for the integrator, such as the number of masking samples. Results from the digital integrator are presented for a data acquisition system with 96 channels simultaneously acquiring data at 500 kSamples/s per channel.



## 1. Introduction

Plasma fusion experiments contain a large number of diagnostics, requiring high channel count data acquisition systems. As the experiments are run for longer, the amount of data acquired increases beyond practical real-time storage limits. Processing this data while it is being acquired allows real time control, and can lead to significant reductions in data storage requirements, allowing larger parts of the experiment to be diagnosed.

This real-time signal processing is usually carried out in host control central processing units (CPUs) or in field programmable gate arrays (FPGAs) on the digitizers. Carrying out the real-time processing in FPGAs, which are integrated into the data acquisition hardware, has the advantage of eliminating the additional latency involved in transferring data over host bus adaptors to a CPU. The parallel architecture of FPGAs is well suited to implementing digital signal processing (DSP) algorithms, which are inherently computationally parallel, resulting in efficient and high speed implementations. These characteristics have led to many DSP systems being developed in FPGAs, e.g. the coupler protection system on Alcator C-Mod [1].

Although FPGAs are "field programmable" in the sense that their functionality can be defined (and redefined) after manufacture, their flexibility at run-time, or dynamic reconfigurability is limited compared to microprocessors. From an end user's perspective, this could be a disadvantage: the signal processing performed on the acquired data cannot readily be altered. The time and cost of re-designing FPGAs as application requirements evolve can be significant.

This paper describes the development of a new platform that will allow end users of data acquisition DSP systems the ability to dynamically reconfigure the systems, without requiring the specialist engineering knowledge or time needed to re-design an FPGA. The DRUID system will allow users to 'build' customized signal processing systems, optimized for high channel counts, through simple software routines.

The architecture of the DRUID system is described in the next section. Section 3 describes the digital integrator that has been

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http://dx.doi.org/10.1016/j.fusengdes.2012.03.047

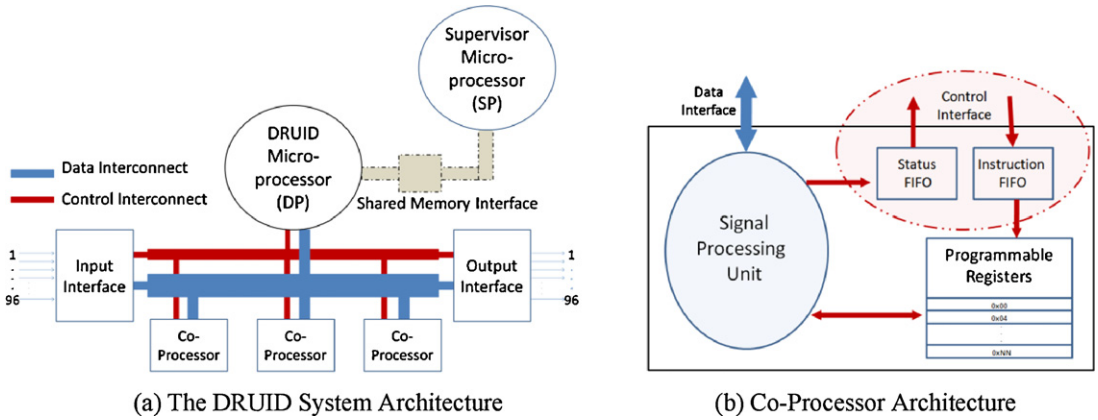


**Fig. 1.** (a) The DRUID system architecture and (b) co-processor architecture.

developed as a proof of concept of the architecture and Section 4 concludes and looks forward to future developments.

## 2. The DRUID architecture

The DRUID system consists of an embedded microprocessor used for configuration and control, and hardware co-processors to perform the signal processing tasks. Fig. 1(a) illustrates the architecture with its separate control and data interconnects. Such "coarse-grain" reconfigurable architectures have been proposed before [2]. However, with modern FPGAs providing embedded arithmetic slices optimized for DSP operations, the DRUID system can be implemented in an FPGA. This allows the system to exploit all of the advantages of FPGAs (cost, speed, HW reconfigurability and parallel processing) while providing microprocessor-like flexibility, for the subset of signal processing functions commonly used in plasma fusion diagnostics.

The DRUID microprocessor (DP) is an embedded Xilinx MicroBlaze inside the FPGA. The DP is responsible for configuring the co-processors and sending instructions over the control interconnect. The data interconnect allows data transfers in any direction between the co-processors.

Fig. 1(b) illustrates the structure of the co-processors. Each co-processor has been optimized to perform a single processing function 'simultaneously' on a single sample data vector. Data in the DRUID system is processed on a sample by sample basis, where each sample consists of data from 96 channels. The co-processors can receive instructions and update their status after processing each sample. This approach allows great flexibility in implementing a DSP algorithm.

The DRUID microprocessor is not involved in the actual data transfer between co-processors. It simply manages the flow of data. This allows continuous execution of the DSP algorithms, with the DP sending instructions to the co-processors as required. The inline processing architecture avoids traditional real-time operating system difficulties, resulting in deterministic data flow.

To reconfigure the system, users simply need to modify the software running on the DRUID microprocessor. This will be done through a second, supervisor microprocessor (SP) via a shared memory interface. The SP will implement an operating system to provide a user interface, and will be capable of generating a DRUID system reset. On reset the DP will execute the new code from the shared memory. Options for implementing the SP (embedded or external) and the shared memory interface are still being investigated. Through this architecture, operating parameters can be modified, or a completely different system can be implemented by activating different co-processors—without the time, effort and complexity of re-designing an FPGA.

## 3. Digital integrator

### 3.1. Principle

The first application that has been developed for the DRUID system is a digital integrator for long pulse magnetic fusion experiments. It is based on the chopper integrator principle proposed in [3]. The magnetic diagnostics used in fusion experiments require continual, real-time integration of the measured signal to give magnetic flux readings, which may then be used for real-time control. Offsets induced in the measured signal by the first amplifying stage, when integrated, can have a significant effect on the readings. A 'chopper-integrator' [3,4], as illustrated in Fig. 2, is used to alleviate the offset problem.

The analogue modulation of the data is carried out by switching the polarity of the coils [3]. A problem with this method is that overshoots may appear in the signal at the switching points. Parts of the signal around these transitions may have to be discarded before integration.

### 3.2. Implementation

The new DRUID platform has been implemented on a Xilinx Spartan 6 FPGA [6] on D-TACQ's RTM-T module. As illustrated in Fig. 3, the data is digitized after amplification. The demodulation and integration of the data are carried out after digitization. Ref. [5] describes progress that has been made with a fixed implementation of such a digital integrator on D-TACQ's ACQ196CPCI digitizers. A

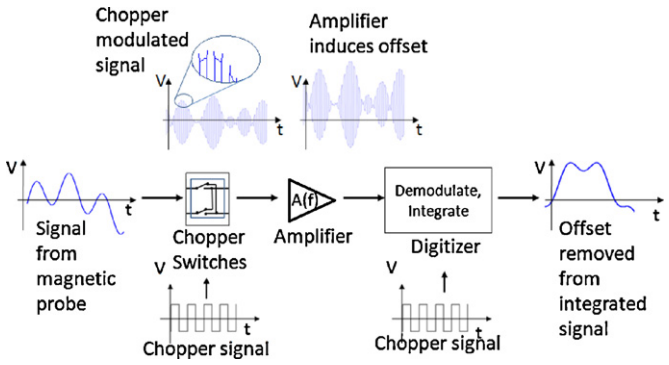


**Fig. 2.** The chopper-integrator principle [3–5].

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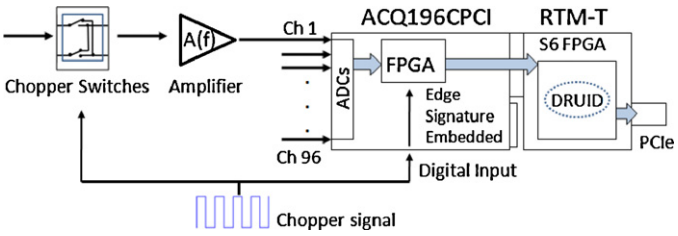


**Fig. 3.** DRUID platform implementation hardware.

```
while(1)
  read sample_type;
  instruct MAC to read in sample;
  if (sample_type = rising_edge or falling_edge) then
    instruct MAC to multiply sample by zero; (discard)
    instruct MAC to output the accumulated value;
    instruct MAC to reset the accumulation;
    if sample_type = rising_edge then
      set polarity = 1;
    else
      set polarity = -1;
    end if;
  else
    instruct MAC to multiply sample by polarity;
    instruct MAC to update accumulation;
  end if;
end while;
```

**Fig. 4.** Simplified algorithm for digital integrator operation.

partial summation is carried out on the data between chopper transitions, discarding samples around the edges that may have become corrupted.

This processing has now been moved to a multiply-accumulate (MAC) co-processor on the DRUID platform which is implemented on the RTM-T. The MAC unit can be configured through software to carry out the demodulation and the integration (accumulation) between chopper edges. The demodulation is carried out by feeding the same chopper signal into one of the digitizer's digital inputs and embedding signatures into the data stream. The DP can decide how to deal with the data on a sample by sample basis—whether samples need to be discarded if they surround an edge, whether they need to be rectified before accumulation, etc. This allows users to control the number of samples that are thrown away and removes the difficulties with synchronizing a demodulation signal. The output frequency of the system can also be controlled—in the digital integrator implementation, piecewise integration is carried out between chopper edges and the accumulated result is output every time a new edge occurs.

A simplified algorithm in Fig. 4 illustrates how the integrator is implemented using sample-by-sample processing in the MAC co-processor.

### 3.3. Resource utilization/statistics

Table 1 records the percentage of the total available resources utilized by the entire module (including the RTM-T communications and control interfaces), the DRUID platform and just the MAC co-processor. Block RAM utilization is high because they are used for the embedded microprocessor memory and because the architecture of the platform requires storage internal to the co-processors. Given the results obtained, there is clear scope in the FPGA to implement more co-processors.

**Table 1**
Resource utilization on the Spartan 6 (XC6SLX45T).

| | Slice registers | Slice LUTs | RAM | DSP |
|---|---|---|---|---|
| Total | 15% | 37% | 54% | 1% |
| DRUID | 6.4% | 3.7% | 34.5% | 1% |
| MAC CP | 1.9% | 0.6% | 3.5% | 1% |

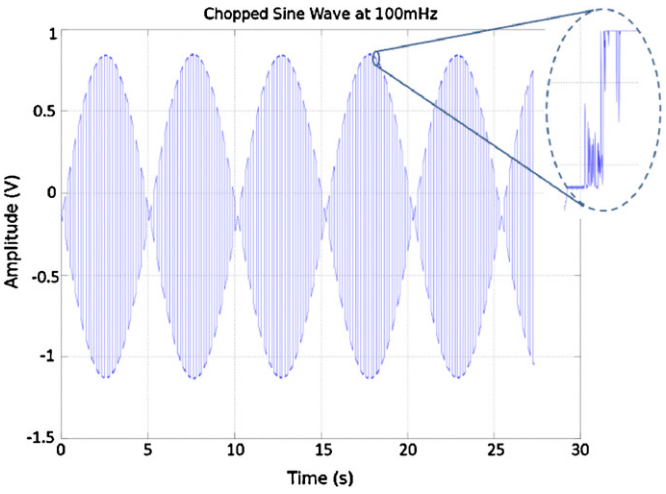


**Fig. 5.** Chopped sine wave input to the digitizer.

The latency through the data acquisition system measured from the analogue to digital conversion all the way through to transfer over PCIe (peripheral component interconnect express) on cable to a host computer is less than 10 μs. Additional latency due to the DRUID platform will vary and depend upon the type of signal processing carried out. For the digital integrator operating in streaming mode, this additional latency was measured to be 1.2 μs.

### 3.4. Results

The DRUID-MAC system has been tested on the D-TACQ ACQ196-RTM-T hardware [7] with simultaneous data acquisition on 96 channels sampled at 500 kSamples/s per channel. For clarity, the results in the next section only show a single channel.

Fig. 5 shows the chopped sine wave input to the digitizers, along with the kind of signal corruption that may be caused by the switching at the chopper transitions. A DC offset can also be seen in the signal.

Fig. 6 demonstrates how the software routine can be modified to zero out the corrupted samples.

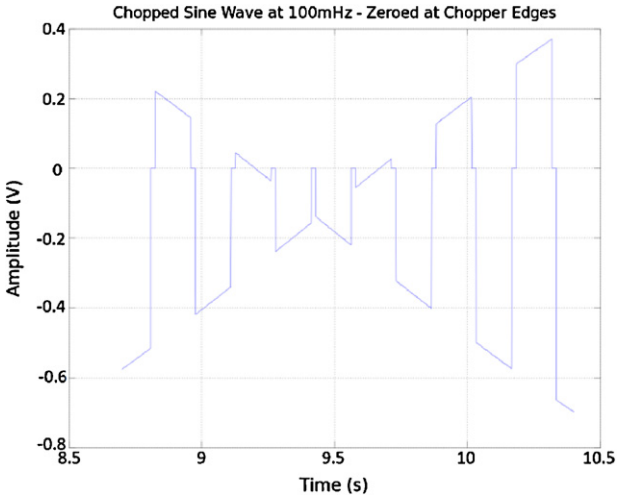


**Fig. 6.** Corrupted samples zeroed out.

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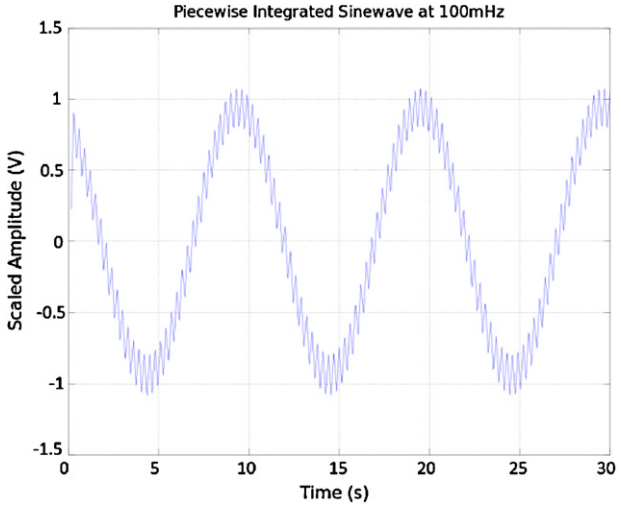


**Fig. 7.** Piecewise integration.

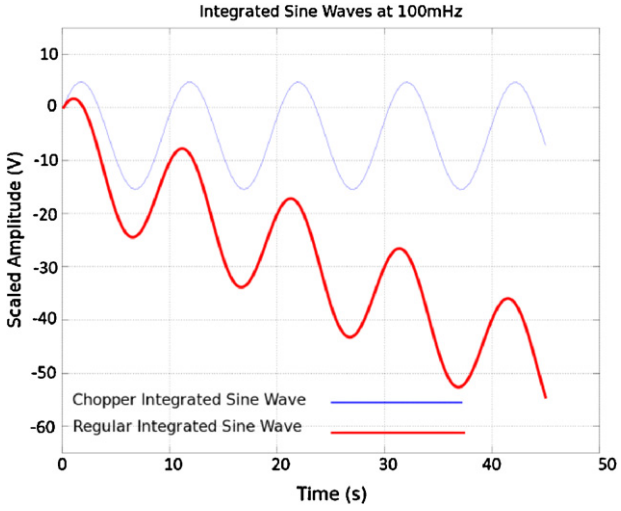


**Fig. 8.** Final summation carried out in software.

Fig. 7 shows the piecewise integrated output. Compare this with Fig. 5. The DC offset has been removed—it shows up as high frequency 'noise' on the required signal, which can be filtered out. This signal has been output at twice the chopper frequency. Integration over many samples significantly reduces the output data rate. Piecewise integration is carried out to avoid overflow problems—the final summation can be carried out in software on a host computer.

Fig. 8 shows result after the final summation has been carried out. For comparison, integration of the input signal without using a chopper has also been plotted on the same graph. The result illustrates the significant effect that offsets can have on an integrated signal, and the effectiveness of the chopper integrator in alleviating the problem. Because additional information can be sent out by the DRUID system, such as the measured chopper duty cycle ratio, with each output sample, the software can compensate for any analogue signal distortions.

## 4. Conclusion

The DRUID system is being developed to provide a powerful digital signal processing platform for plasma fusion and other high energy physics experiments. This paper has described the architecture of the system and demonstrated a working prototype for the digital integrator application. Users can change the functionality of the system in a microprocessor-like way, while fast, simultaneous processing is carried out on a very large number of input signals, utilizing the parallel processing capabilities of the FPGA. With the addition of more CPs, users will be able to combine multiple processing units to implement more complex algorithms, which can be updated or modified through software as experiment requirements evolve.

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