Power conversion for a modular lightweight direct-drive wind turbine generator

Max Alexander Parker

A Thesis presented for the degree of
Engineering Doctorate

School of Electrical, Electronic and Computer Engineering
University of Newcastle upon Tyne
England

July 2009

Power conversion for a modular lightweight direct-drive wind turbine generator

Max Parker

Submitted for the degree of Engineering Doctorate
July 2009

Abstract

A power conversion system for a modular lightweight direct-drive wind turbine generator has been proposed, based on a modular cascaded multilevel voltage-source inverter. Each module of the inverter is connected to two generator coils, which eliminates the problem of DC-link voltage balancing found in multilevel inverters with a large number of levels.

The slotless design of the generator, and modular inverter, means that a high output voltage can be achieved from the inverter, while using standard components in the modules. Analysis of the high voltage issues shows that isolating the modules to a high voltage is easily possible, but insulating the generator coils could result in a significant increase in the airgap size, reducing the generator efficiency.

A boost rectifier input to the modules was calculated to have the highest electrical efficiency of all the rectifier systems tested, as well as the highest annual power extraction, while having a competitive cost. A rectifier control system, based on estimating the generator EMF from the coil current and drawing a sinusoidal current in phase with the EMF, was developed. The control system can mitigate the problem of airgap eccentricity, likely to be present in a lightweight generator.

A laboratory test rig was developed, based on two 2.5kW generators, with 12 coils each. A single phase of the inverter, with 12 power modules, was implemented, with each module featuring it's own microcontroller. The system is able to produce a good quality AC voltage waveform, and is able to tolerate the fault of a single module during operation.

A decentralised inverter control system was developed, based on all modules estimating the grid voltage position and synchronising their estimates. Distributed output current limiting was also implemented, and the system is capable of riding through grid faults.

Declaration

The work in this thesis is based on research carried out in the New and Renewable Energy Group, the School of Engineering, Durham University, England, in conjunction with the New and Renewable Energy Centre (NAREC), Blyth, Northumberland and the University of Newcastle Upon Tyne. No part of this thesis has been submitted elsewhere for any other degree or qualification and it all my own work unless referenced to the contrary in the text.

"I love deadlines. I like the whooshing sound they make as they go by."

Dilbert, by Scott Adams

Acknowledgements

I would like to thank my supervisor, Dr. Li Ran, for his endless patience in supervising me, and his knowledge and enthusiasm. I would also like to thank Professor Peter Tavner for his role in my supervision, for introducing me to the joy of Microsoft Project, and inspiring me with many stories of his time in the Royal Navy and the electrical engineering industry. At Newcastle University Professor Alan Jack has provided much constructive criticism of the high voltage aspects of the project, and without his input chapter 5 would never have been written, and this thesis would have been much the poorer.

The test rig would never have been built without the amazing work of the electrical and mechanical workshop technicians, with special thanks to David Jones for wiring everything up, Neil Clarey for manufacturing the control boards, Tony Collinson for building the mechanical systems and Ian Hutchinson for ordering components and running everything smoothly. I am also greatful to Cleveland Circuits, who manufactured the power boards.

From NaREC, I would like to thank Kevin Hanley for his kind assistance in explaining the company structure and finances for my Eng Doc business case study. I would also like to thank Steve McDonald, Adrian Wilson and Stephen Wilson for their support during the project.

Acknowledgements must go out to my fellow postgraduate students in the New and Renewable energy group at Durham, including, but not limited to, Richard Martin, Michael Wilkinson, Nick Stannard, Fabio Spinato and Padraig Lyons. Much merriment was had over the years, as well as much discussion about engineering.

Finally I would like to thank the past and present members of the Durham University Karate-do Shotokai club, including Grant Ingram, Aidan Rhodes, Thomas Butts, Andrew Egan, James Holloway, Will Black, Philippa Wilcox and Angharad Kenway. Practicing karate with these people has provided an outlet for the anger and frustration which frequently arises throughout the course of academic research, and has helped keep me sane.

Contents

List of Figures

List of Tables

Chapter 1

Introduction

The birth of the modern wind turbine is considered by many to have occurred in 1957 with the 200kW Gedser turbine [1], shown in Figure 1.1, which featured a 3-bladed upwind turbine, driving a cage rotor induction machine through a step up gearbox, and featuring electromechanical yaw control. Until the mid 1990's, most turbines were based on this "Danish Concept".

Figure 1.1: The Gedser wind turbine [2]

The generator was connected directly to the electricity grid, usually with a capacitor bank for reactive power compensation and often through a soft starter. This resulted in an almost fixed speed operation, meaning that any gusts in the wind

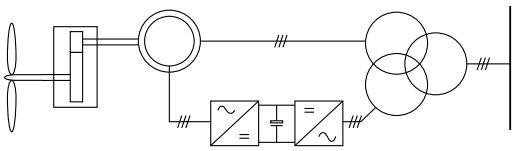
would result in a sudden spike in the electrical power output. This required a stiff grid in order to maintain stability and also resulted in high mechanical stresses to the turbine drive train [3]. Blade pitch control was added to turbines in order to reduce the generator torque at high wind speeds but the time constant of the pitch control mechanism was usually too slow to compensate for gusts. Such limitations increased the interest in variable speed wind turbines. Variable speed operation offers the following advantages:

- The turbine inertia can be used to smooth the mechanical forces in the drive train, so the energy of the gust will cause the turbine rotation speed to increase temporarily instead of being transferred onto the grid.
- In a similar fashion, the turbine power output is smoothed, which is of benefit to the operators of the electricity network.
- Power capture is increased at lower wind speeds as the turbine speed can be matched to the wind speed and so track the maximum power point of the system.
- Acoustic noise is reduced at lower wind speeds by the lower rotation speed of the turbine.

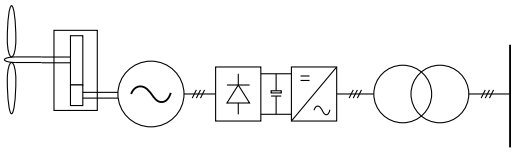
1.1 Variable Speed Concepts

1.1.1 Geared Doubly Fed Induction Generator

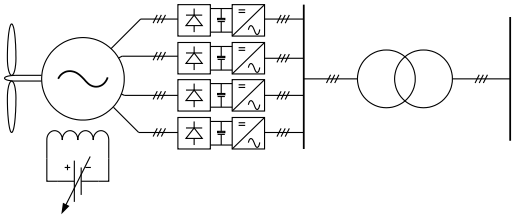
The most widely used method of achieving variable speed is to use a Doubly-Fed Induction Generator (DFIG), shown in Figure 1.2a, and Figure 1.3, in which the stator of a wound rotor induction machine is connected directly to the grid, while the rotor is connected via a 4-quadrant ac-ac converter. The converter is typically rated at around 25% of the turbine output, and allows a speed variation of around ±33% from the synchronous speed [3]. The generator is typically a 6-pole unit, with a synchronous speed of 960rpm, and is connected to the turbine hub through a step up gearbox. The generator and converter are standard industrial parts, which has contributed to an increase in reliability and reduction in cost of wind turbine systems.



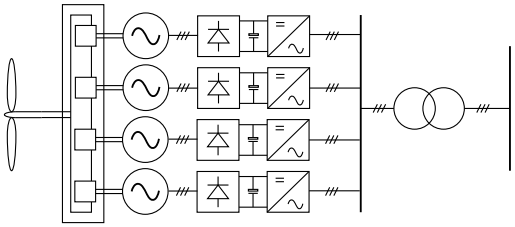
(a) Geared drivetrain with doubly-fed induction generator and transformer interface.



(b) Geared drivetrain with permanent magnet generator, fully rated converter and transformer interface.



(c) Direct drive generator with four fully-rated converters and transformer interface.



(d) Clipper concept – geared drivetrain with multiple generators and fully rated converters.

Figure 1.2: Turbine Drive Systems

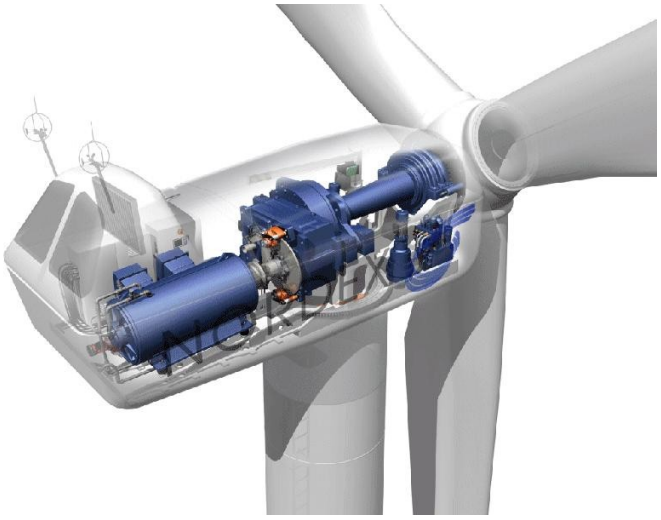


Figure 1.3: A Nordex wind turbine, using a geared generator [4]

Reliability of the geared turbine system is generally high, due to the use of a standard industrial generator and converter, although the generator brushes need to be maintained. The gearbox is one of the less reliable parts, generally as wind turbine gearboxes tend to be specialised parts [5]. Scaling turbines to larger sizes results in a lower rotation speed, which increases the gear ratio required to achieve the rated speed of the generator. This has resulted in an increase in the number of stages in the gearbox, usually 3 for large turbines, as well as the gearbox size, which reduces the turbine efficiency and gearbox reliability.

The increase in the size of the turbines has meant that the current in the generator connection cables has increased as the voltage has remained static at 690V. This is a problem in a DFIG-based system where the transformer and converter are usually housed in the base of the tower in order to reduce the weight of the nacelle. This means that several high current cables must be passed down the entire height of the tower.

A further issue with the DFIG-based system is in it's ability to ride through grid faults. A generator without power electronics is able to ride through faults because the generator is designed to withstand the high currents that occur for a short period of time when the grid voltage collapses. A power electronic interface must limit the current by reducing the modulation depth of the output as the power device thermal inertia is too low to allow it to withstand high over-currents, which is desired to operate protection relays.

1.1.2 Direct Drive Synchronous Machine

The use of a slow speed direct drive generator, as in Figure 1.2c, eliminates the need for a gearbox in the turbine, increasing efficiency and eliminating a source of unreliability. Enercon is the main producer of direct drive turbines and produce models up to 2.3MW in size along with a prototype capable of producing up to 6MW. Some examples of direct drive machines are shown in Figure 1.4.

The generator most used in direct drive turbines is the wound field synchronous machine, similar to what is used in conventional power generation. Variable speed is achieved by using a fully-rated direct in line ac-ac converter, which is more expensive than the partially rated converter of the DFIG system. Fault tolerance can be achieved by using several small converters instead of one large one – the loss of one

(a) Enercon E70 [6] (b) Zephyros Z72 [7]

Figure 1.4: Some Direct Drive Turbines

small converter will result in a reduction in maximum power output but the turbine will still produce power. The fully-rated converter typically allows a greater range in turbine speeds than the DFIG system, increasing power capture at low wind speeds. The Enercon E70, shown in Figure 1.4a, uses this type of generator.

Machines using permanent magnets instead of electrical excitation have also been designed [8], which offer an improvement in efficiency and a reduction in complexity compared with electrical excitation. However the magnets used are expensive and the generator is more difficult to manufacture due to the permanent force of attraction between the rotor and stator. The Zephyros Z72, shown in Figure 1.4b, uses this type of generator. An induction generator of this size would be impractical for direct drive, as the larger air gap of a large diameter machine would result in a high leakage flux, and thus a high magnetising current [1].

Low speed slotted synchronous machines are often used in marine propulsion and hydroelectric generation, and these typically have a rated speed of around 100-200rpm with 30-60 poles and power ratings up to hundreds of MW. By contrast, the Enercon E82 is rated at 2MW and rotates at up to 19.5rpm, and would require a 300-pole generator to achieve 50Hz output. This leads to a very small pole pitch as well as a large generator diameter, while retaining the small airgap used in high speed machines, leading to high air gap closing forces. Because of the high air gap forces, a very strong and stiff structure is required in order to maintain the air gap

size. A geared system typically has a specific weight of around 10kg/kW for the generator and gearbox, while present direct drive systems have a specific weight of 20-30kg/kW [1].

The multipole generator system is complicated and expensive to manufacture, and has been shown to be less reliable than the DFIG-based system which uses standard parts [5]. The converter has also been shown to be less reliable, but the absence of a gearbox means that overall reliability is similar to that of the DFIG system. Cost is also increased due to the fully-rated converter, although the systems using permanent magnets instead of electrical excitation offer even greater efficiency but at higher cost. Fault ride-through capability is improved, due to the fully-rated converter that interfaces directly to the grid, as is operation in weak grids. Efficiency is higher due to the removal of the gearbox, while power capture is improved by the increased speed range.

1.1.3 Alternative Systems

Wind turbine systems have been developed which use a fully-rated converter and a high speed induction or permanent magnet synchronous generator connected through a gearbox, shown in Figure 1.2b. Such systems are not widespread due to the increased cost of the converter compared with the DFIG system, while still including a gearbox. One system has been introduced by the manufacturer Clipper, which uses a step-up gearbox driving four permanent magnet generators at 1133rpm rated speed, with each generator having it's own power converter, shown in Figure 1.2d. Advantages are claimed in fault tolerance and grid fault ride through capability, although the turbine is primarily marketed for remote areas with weak grid connections and long fault clearance times.

It is anticipated that as power electronic converters become more compact and economical, concepts including fully-rated converters will become more attractive while the DFIG, suffering from problems with fault ride through and reliability of the brushes and slip rings, would gradually fade away in newly built wind turbines.

A potential solution for the scalability issues of current designs is to use a medium speed generator, operating at around 100-200rpm, and a single stage gearbox [9]. The generator would be smaller than a typical direct drive generator, and much more similar to conventional designs, while the single stage gearbox would be more

reliable and lighter. Further weight improvements could be achieved by integrating the gearbox, generator and low-speed bearing.

All the concepts detailed above are connected to the grid using a step up transformer, located either in the base of the turbine or the nacelle. The grid voltage is typically 11-33 kV and the generators typically output power at 690V. Systems using industrial medium voltage converters have been designed [10], although these are more expensive due to the higher cost of high voltage power semiconductor devices.

1.2 Turbine Scalability

Perhaps the biggest trend in the wind industry is the move towards greater numbers of offshore turbines. Onshore turbines are limited in size by site access and transportation, and few turbines larger than 3MW are in operation onshore. There is less of a transportation issue offshore, while the cost of installation, foundations and electrical connection is much greater per turbine. For this reason the offshore industry is driving the building of larger turbines.

While reliability is important onshore, it is even more important offshore where access to the turbine for maintenance is significantly more difficult and expensive. It is clear that both of the current mainstream turbine designs suffer from reliability issues, which need to be solved in order to make offshore wind power competitive with other forms of generation, and these problems will become more significant as the turbine size increases.

From a reliability standpoint it is desirable to eliminate the gearbox, so a direct drive solution is required. Unfortunately the direct drive turbines currently in operation suffer from the problems with the complexity and weight of the generator, and the unreliability of the power electronic interface, which must be addressed.

1.3 Lightweight Direct Drive Generators

All iron-cored electrical machines, as in Figure 1.5, experience a force of attraction between rotor and stator, which may be 100 times greater than the torque producing shear force. In a radial flux machine this force is balanced between the different sides of the rotor. However if the rotor or stator become distorted this will decrease the

air gap size in parts of the machine, increasing the stress in that area, which will further distort the machine. For this reason radial electrical machines need to have a stiff structure to maintain a constant air gap and prevent this deformation. A stiff structure is simple to achieve in a high speed machine, but much more difficult in a low speed machine with a large rotor diameter but relatively small air gap size. The generators are also expensive to manufacture due to the large number of rotor poles, which leads to a large number of stator slots compared with a high speed machine, making winding the generator a long process.

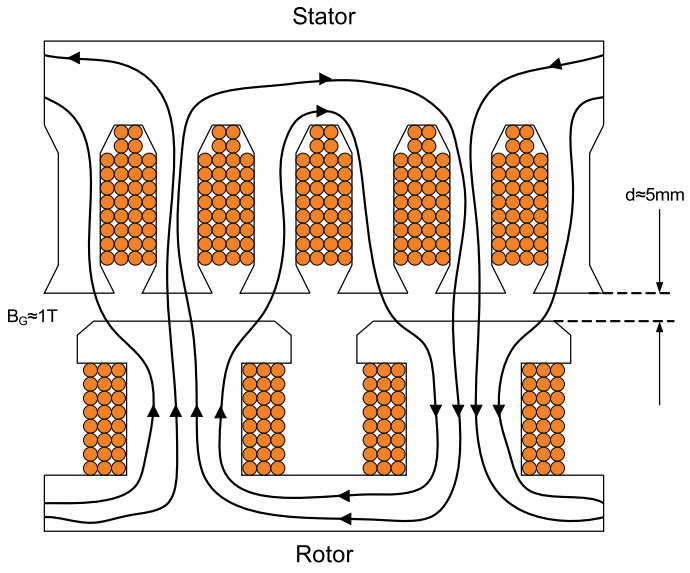


Figure 1.5: Cross section of a slotted generator, with electrical excitation

An alternative generator construction is to situate the stator coils in the air gap of the generator, with an iron core behind them, and permanent magnet excitation on the rotor, which is shown in Figure 1.6. This would reduce the airgap flux density from around 1T to 0.5T, which would significantly reduce the attraction forces between rotor and stator. The lower flux density means that a greater number of turns would be required in the stator coils in order to achieve the same EMF. This is possible because the elimination of the stator slots allows more space for copper, and enhanced cooling potential, which allows a higher current density to be used at the expense of lower efficiency. The reduced airgap closing forces allow a lighter structure to be used to support the generator.

A generator has been designed in association with Durham University which uses a completely ironless stator, and a prototype has been constructed [11]. The

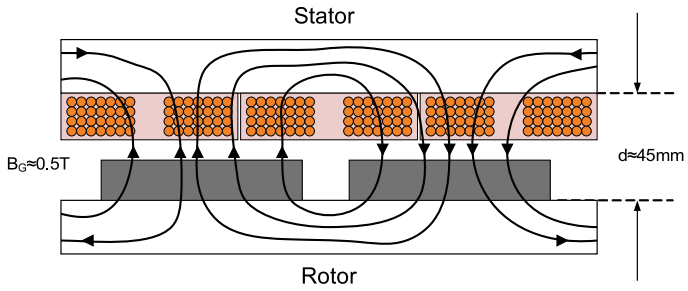


Figure 1.6: Cross section of a slotless generator, with permanent magnet excitation

ironless stator reduces the flux density to around 0.25T, and the highly uneven flux distribution around the permanent magnets mean that a larger pole pitch must be used than in an iron cored generator in order to avoid excessive leakage flux. This results in a very large generator diameter – up to a third of the turbine diameter. To support the generator a spoked structure has been proposed. The generator with an iron core but airgap windings mentioned in the previous paragraph has been proposed as an alternative solution as it offers a greatly reduced diameter.

It is proposed modular system of coils be used, with racetrack coils being random wound and encapsulated as single units before being attached to the stator. This approach should allow greater reliability, and reduced cost of the mass produced coils, compared with a slotted machine.

1.4 Power Electronic Interface

One of the distinguishing features of the lightweight concept under consideration is that the separate coils and modular design mean that it is fairly easy to vary the number of electrical phases of the generator. Most electrical machines use three phases, as this is what the electricity grid uses. Although connecting a machine through a power electronic inverter allows a different number of phases to be used, the convention of using three phases is kept in order to allow machines and inverters from different manufacturers to interoperate. In spite of this, multi-phase machine designs offer several advantages over three-phase [12]:

- Multi-phase machines have a higher fault tolerance than 3 phase. If one phase of a three phase machine is lost then the machine will behave as a single phase machine, and will be unable to self start as well as being significantly derated.

If one phase of a 15 phase machine is lost then the machine will still start and derating will be minimal.

- Multi-phase machines produce a magnetic field with lower space-harmonic content, leading to higher efficiencies.
- The reduced space-harmonics in the magnetic field leads to lower-time harmonic components in the excitation waveform. These components would produce a pulsating torque and excess noise.

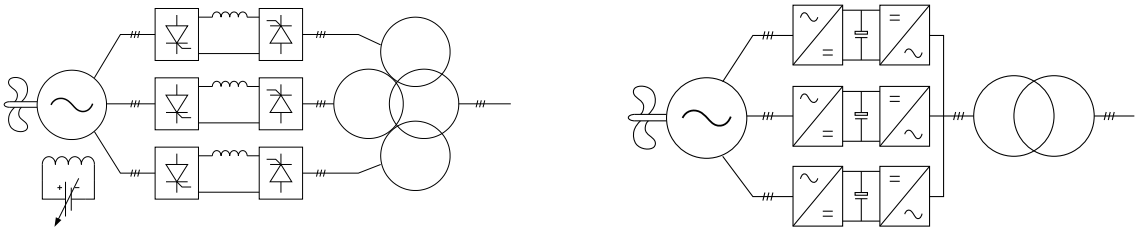
The issue of fault tolerance is of greatest interest in wind applications, but this can still be achieved using a three phase generator with multiple coils connected separately rather than in series. One method for connecting the coils devised by the designers of the proposed generator is to connect each coil to a common DC bus, via a single phase rectifier. This is possible because of the minimal mutual coupling between coils, and offers a high level of fault tolerance. However, the use of passive rectifiers and the low reactance of the coils leads to a short conduction period, which would lead to a pulsating torque. To minimise this pulsating torque several phases are used, the generator design used in this project features 8 phases.

At present, low-speed direct-drive and multi-phase machines are being used in the area of marine propulsion. Although there are many differences, some of the technology may be appropriate to large scale wind.

1.4.1 Marine Drive and Other Multiphase Applications

Electric ship propulsion is attracting considerable interest, due to the increases in efficiency and the ability to distribute the engines around the ship without the need for long drive shafts. A distribution voltage of 4.16kV and 60Hz is usually used, with 13.8kV used in larger ships. Direct drive machines are used, with multi-phase machines in particular attracting considerable interest due to their fault tolerance and smooth torque characteristics. In the past synchronous machines have been used, driven by thyristor-based converters, with several 3-phase converters being used to supply the phases in groups of three. The converters are often supplied by a phase shifting transformer to step the voltage down and reduce the rectifier input current harmonics. This arrangement is shown in Figure 1.7a. A more recent connection method involves using voltage source inverters, shown in Figure 1.7b,

where a phase shifting transformer is not needed if an actively controlled PWM rectifier is used. At present converters are available which can operate up to 4.16kV, so a step-down transformer is not always required.



(a) Multi-phase synchronous machine with current-source inverter

(b) Multi-phase induction machine with voltage-source inverters

Figure 1.7: Marine Drive Systems

Most of these machines are similar to conventional machines, unlike the proposed concept, so most of the power conversion technology would not be appropriate. For instance, the Alstom Advanced Induction Motor shown in Figure 1.8, designed for ship propulsion, is a 20MW machine rotating at 180rpm, using around 20 poles. As a comparison, a 1.8MW lightweight direct drive generator design would rotate at 15rpm and have around 200 poles.

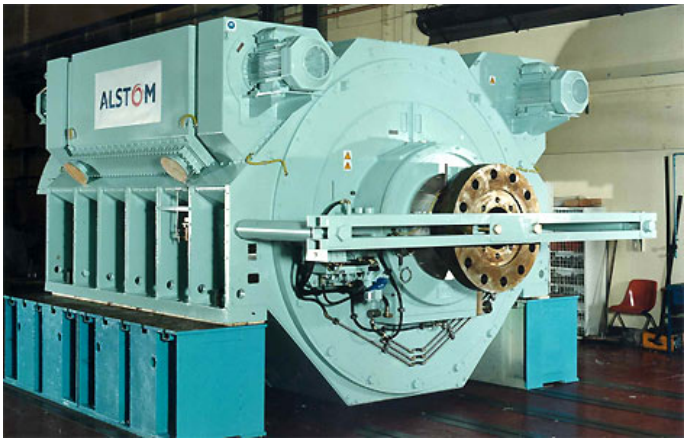


Figure 1.8: Alstom/Converteam advanced induction motor [13]

The conventional machine design used in most multi-phase machines uses overlapping coils, leading to a high level of coupling between phases. This combined with the need to provide excitation for the induction machine means that coils cannot be considered separately, and an often complex centralised switching scheme must be used [12]. The centralised switching and higher airgap tolerance of the

more compact machine means that distributed power electronics is not necessary, and the converters are usually housed in several cubicles allowing easy access for repairs. However the multiple converters provide for a high level of fault tolerance, as described in [12], and this would be beneficial for large scale wind turbines.

Another application of multiphase machines is in aircraft applications, where a high level of fault tolerance is required. A design of brushless DC machine for aircraft fuel pumps uses a 4 phase machine with single tooth windings, specifically designed to minimise coupling between coils. The coils are each driven by an individual single phase inverter and DC link, although control is central. In this case the inverter is separate from the machine, which at 15kW and 60,000rpm and oil cooled is very compact, while the inverter is air cooled and fairly large [14].

The main similarity between multi-phase machines and the lightweight direct drive generator technology is that in both cases the machine and power conversion must be designed together as a system, rather than the conventional practice of buying generic machines and drives from different suppliers. Most multi-phase machines rely for fault tolerance on the larger number of phases and sophisticated control while the proposed concept relies on having a large number of identical coils with an arbitrary number of phases.

1.4.2 Power Conversion Issues with Lightweight Generators

The modular nature of the proposed concept invites a modular power conversion scheme, in order to reduce cost and improve fault tolerance, and the nature of the machine provides opportunities and challenges in the design of such a scheme. These issues, to be found in any generator using separate coils along with a lightweight ironless or slotless structure, are detailed below:

- The use of separate modular coils results in low mutual inductance between adjacent coils, meaning that a modular power conversion scheme can be controlled locally, without having to worry about coils connected to other modules. This is different from the multi-phase induction machine arrangement in which central control is required and therefore fault tolerance is lower.

- The lightweight generator structure results in a lower air gap stability, meaning that the air gap size and hence the coil EMF could vary around the machine

and with time as the machine rotates. It is desirable to keep the power drawn from each coil constant in order to keep the torque distribution around the generator even, and to prevent torque pulsations.

- The slotless design allows the coils to be more easily insulated to a higher voltage than possible in a slotted generator. This could allow a system to be used in which the grid interface transformer can be eliminated, improving efficiency and reducing cost.

1.4.3 Proposed Power Electronic Interface

It has been proposed that a cascaded multilevel voltage source inverter (CMVSI) be used to connect the generator to the grid. This type of inverter consists of several H-bridge inverters whose outputs are cascaded to form one phase of the inverter, with the outputs switched so as to synthesize a sinusoidal voltage output. Such a system allows for a high output voltage while using lower voltage switching devices, and a modular approach can be used with each level being a separate identical module to reduce costs.

One of the main problems limiting the use of multilevel converters has been the difficulty of controlling the DC-link voltages of the different levels. In the proposed design the DC links of the modules will be fed by individual coils in the generator, and if a boost rectifier is used the DC-link voltages will be individually controllable. Such a system, with boost rectifiers, is shown in Figure 1.9.

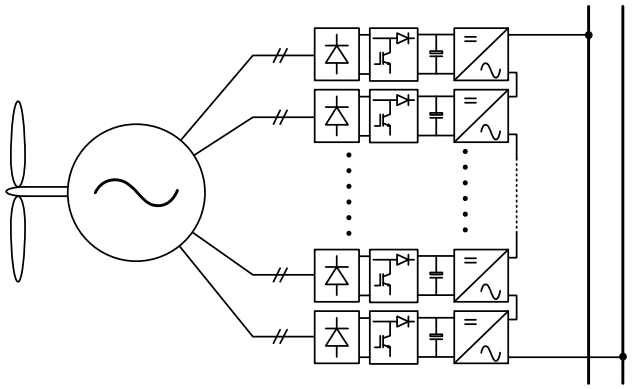


Figure 1.9: Direct-drive generator with one phase of the cascaded multilevel inverter-based grid interface

1.5 Scope of this Project

A switching strategy for the proposed inverter has been developed within Durham University, which aims to equalise the power sharing between converter modules as much as possible. A rectifier topology and control system have not been determined, and must be designed, with the following features being desirable:

- Shaping the coil current so that it is sinusoidal and in phase with the coil EMF, in order to maximise the power extraction from the coils and minimise torque ripple.
- Allowing a wide variation in turbine speed, allowing maximum power capture at a wide range of wind speeds.
- Regulating the module DC link voltage to maintain a constant voltage with changing inverter output, and a difference in power sharing between modules.
- Preventing ripple in the DC link voltage, at twice the grid frequency due to the inverter switching, from causing an associated ripple in the rectifier current demand.
- Mitigating any undesirable effects of the airgap eccentricity on the generator EMF.

The design of the rectifier will have a significant impact on the system efficiency and cost, as well as the power output and control strategy. A 1.8MW lightweight generator has been designed, and components will be sized for this design. The choice of components will give allow a breakdown of the electrical losses in the system, as well as the costs of the converter components. A test system will be designed and built around a smaller direct drive generator in order to validate the proposed power electronic design.

While the inverter switching strategy has been developed, it has not been implemented in hardware, method of implementation must be developed. As the power electronic modules could feature a significant processing power due to the rectifier, much of the inverter switching could be implemented on the modules themselves, rather than determining each switching instance in a central controller. This would

have the advantage of reducing the number of control cables that would need to connect to the modules.

As the proposed system will have a high voltage output of 11kV, the issues with using such a high voltage will be investigated. In particular the insulation requirements in the generator and power electronics will be determined, as well as the arrangements for lightning strike protection.

The main goal of this project is to show that the proposed system is workable, which will be demonstrated on a laboratory prototype. A significant advantage of the proposed inverter system is that of fault tolerance, where the inverter is able to continue operating after faults in some of the modules, and this must be demonstrated. The ability of the inverter to ride through grid faults should also be investigated.

The choice of a cascaded multilevel inverter, with a high voltage output, for grid interfacing, is highly dependent on the design of the proposed generator. While the generator design makes the proposed power electronic system possible, the design and control of the power electronic system could also mitigate many of the disadvantages of the generator design, increasing the viability of the complete system.

Chapter 2

The Savonius Project

Initial work was concerned with developing a power electronic interface for a small scale wind turbine, with a newly developed direct drive axial flux generator. The interface is designed to connect the generator to a battery bank, to charge the batteries, and the aim was to increase the power extraction compared with connecting the generator through a passive rectifier alone. This is achieved by increasing the speed range of the turbine, so that the turbine's maximum power operating point can be tracked over a wider range of wind speeds.

While this system different from the large scale applications mentioned in the introduction, the principle of increasing the speed range of the turbine to improve the power capture is equally valid for large scale systems, as is the method for estimating the improvement in the annual power capture of the turbine.

The wind turbine used is a savonius-type vertical-axis turbine, which will extract 166W in a 9m/s wind, and rotating at the optimum speed of 216RPM. It is a drag-based turbine, so it will generate torque from rest and can self-start. The turbine is shown in Figure 2.1, and further details are given in Table 2.1. The generator is an air-cored axial-flux generator, with coils wound on nylon bobbins and mounted in a plastic frame in the air gap, and is designed to be cheap to produce and rugged [15]. The individual bobbin-wound coils mean that characteristics will be similar to the lightweight direct-drive generator, which was mentioned in the introduction. In particular the mutual inductance between coils will be low. The generator has 12 coils in 3 phases, and for this application the 4 coils in each phase will be connected in parallel. A summary of the generator characteristics is given in Table 2.2.

Typically small scale wind turbines use permanent magnet synchronous genera-

Figure 2.1: The savonius wind turbine

Turbine diameter	0.78m
Turbine height	2.4m
Turbine moment of inertia	7.9Nms^2

Table 2.1: Turbine characteristics

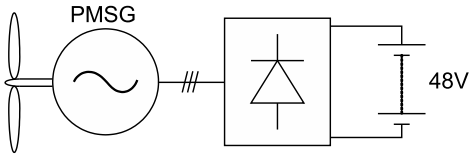
Number of coils	12
Number of pole pairs	8
Coil Inductance	4mH
Coil Resistance	1Ω
Maximum current per coil	3A

Table 2.2: Generator characteristics

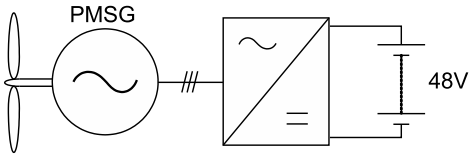
tors (PMSG), as in this case, which are connected to the batteries through a passive diode rectifier. This is shown in Figure 2.2a. A charge controller is usually also used, which will prevent the batteries being over charged by dumping power into a load. The fixed battery voltage limits the speed range of the turbine, meaning that the number of turns in the generator coils will determine the operating speed of the turbine, and hence the power capture in different average wind speeds.

An alternative approach would be to replace the passive rectifier with a fully active four-quadrant converter, shown in Figure 2.2b. This would provide a voltage boosting capability allowing the turbine speed to vary, as well as drawing a sinusoidal current, maximising the generator utilisation and minimising torque ripple. Unfortunately the converter would use 6 or more switching devices, making it costly in terms of components and gate driving circuitry. The converter would also require the generator EMF position to be tracked, requiring a powerful controller.

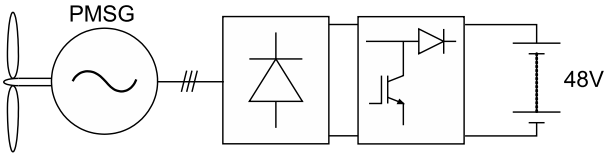
A cheaper alternative is to use a boost converter in between the passive rectifier and battery, to allow the turbine to operate at different speeds, shown in Figure 2.2c. Although the passive rectifier would still cause a torque ripple in the generator, the converter would be significantly cheaper, requiring only one transistor. It is this design which shall be considered.



(a) Battery connection through passive rectifier



(b) Connection through full 4-quadrant converter



(c) Connection through passive rectifier and boost converter

Figure 2.2: Small scale wind turbine battery connection

2.1 Modeling of the System

Initial modeling was carried out in order to find the most efficient operating point for different wind speeds, and to calculate the power curve – the curve of power output against wind speed. For all modeling the generator was represented as sinusoidal EMFs in series with inductance and resistance for each phase, with the EMF being proportional to the rotation speed. The DC side of the rectifier was modeled as a Thevenin-type voltage source to represent the battery and boost converter. The mechanical power extracted by the turbine is given by the following equation:

$$P_{\text{mech}} = 0.5 C_p \rho {v_w}^3 A \tag{2.1}$$

Where P_{mech} is the mechanical power extracted, C_p the turbine coefficient of performance, which determines how much of the energy in the wind the turbine can extract, v_w the wind speed, A the turbine swept area and ρ the air density. C_p is a function of, λ, the ratio of the speed of the blade tips to the wind speed, and is shown for this turbine in Figure 2.3.

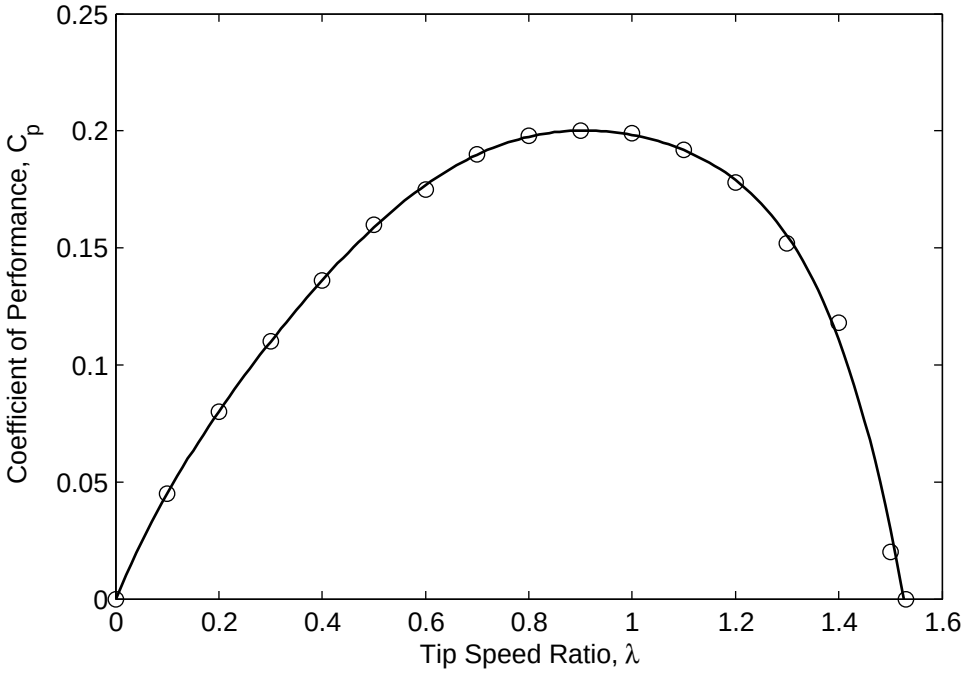


Figure 2.3: Turbine C_p-λ curve

A simulation was created using Simplorer, shown in Figure 2.4. For a given wind speed and turbine speed, the mechanical power can be calculated using Equation 2.1,

and the torque calculated by dividing by the speed. The electrical torque can be calculated from the electrical circuit simulation, from the coil real power. When the electrical torque is subtracted from the mechanical, the resultant torque will cause the turbine to change speed, and the speed will move toward a steady state value where the mechanical and electrical torques balance, at a rate determined by the turbine moment of inertia.

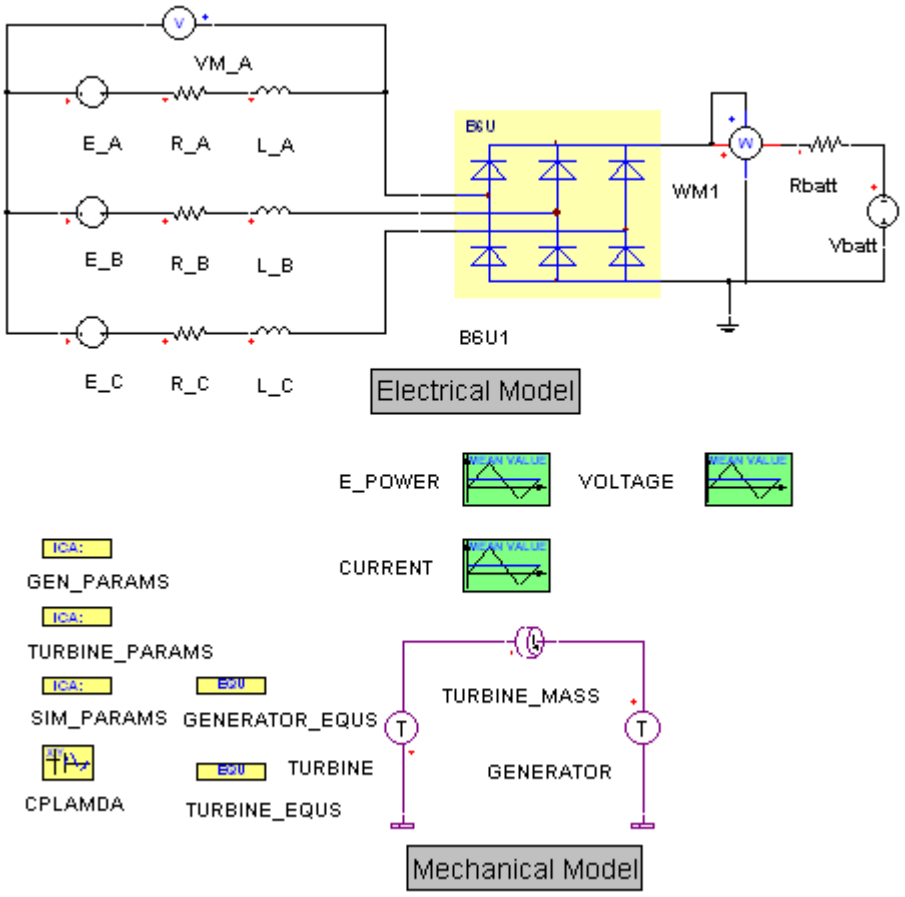


Figure 2.4: Simplorer model for the system

The simulation was run for a simulation time of 10s, to allow the turbine speed to settle at the steady state value, and at the end of the time the power output and other variables were recorded. This was carried out at DC voltages between 10V and 100V and wind speeds between 1 and 20m/s, with a step of 1V and 1m/s respectively. 1820 simulations were required, which were set up and performed automatically.

The results of the simulations were processed using Matlab, to smooth out and interpolate the curves. For each wind speed, the maximum electrical power was

found along with the other parameters at this power. The electrical power was also calculated for DC voltages of 24V and 48V, to simulate the effects of connecting the output of the rectifier directly to a battery.

2.2 Simulation Results

Some of the simulated power-speed curves for various wind speeds are shown in Figure 2.5, along with the operating lines for maximum power and direct battery connection. It can be seen that the direct battery connections limit the speed to a narrow range, with the speed being higher at higher powers due to the voltage drop from the generator resistance increasing. The battery terminal voltage will also increase due to the internal resistance of the batteries. The line of maximum electrical power is slightly to the right of the maximum mechanical power, as the faster generator speed reduces the current for a given power, increasing the efficiency. This offsets the drop in wind power capture from operating at a faster speed.

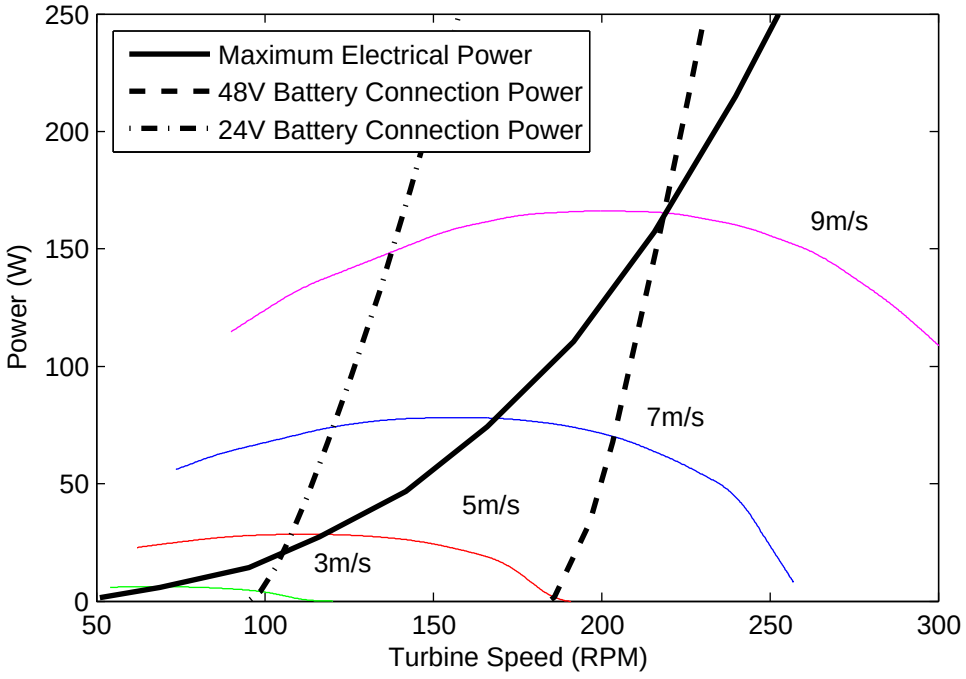


Figure 2.5: Electrical power vs. turbine speed at different wind speeds.

The simulated power vs. wind speed curve is shown in Figure 2.6 for maximum power and battery connections. It can be seen that the limited speed range of the direct battery connection at 48V battery voltage limits the power capture at low

wind speeds. Above around 8m/s wind speed, the power capture is very similar. At 24V battery voltage, the speed range of the turbine is limited around a lower value than at 48V, and the power capture is good at low wind speeds, but deteriorates above 7m/s wind speed.

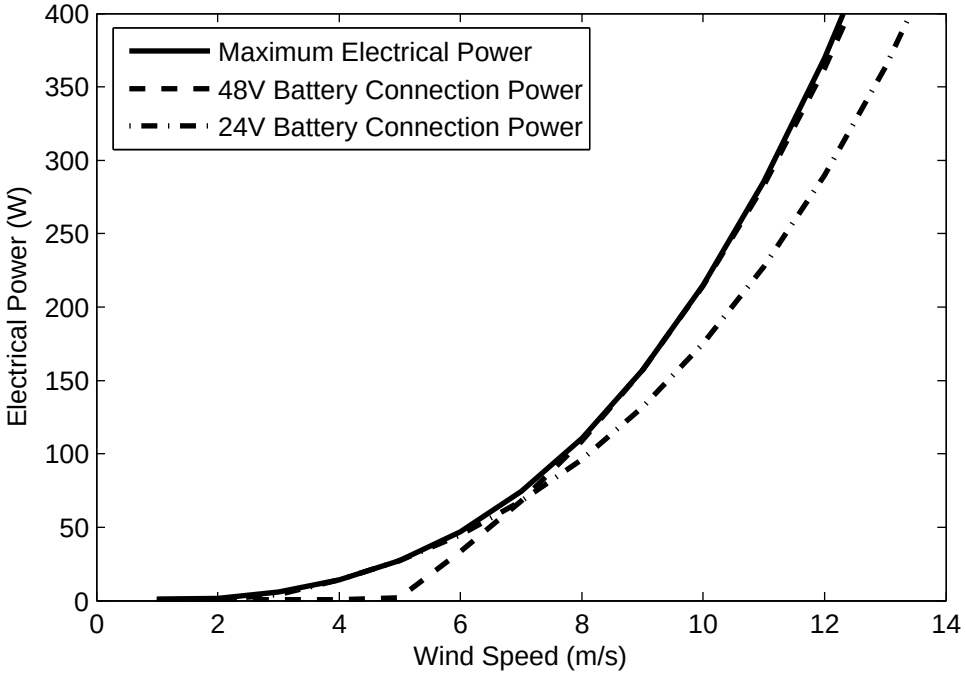


Figure 2.6: Electrical power vs. wind speed

2.3 Proposed Power Tracking Solution

2.3.1 Converter Topology

It can be seen in Figure 2.6 that a direct battery connection at 48V, as currently used, results in a good tracking of the maximum power curve at wind speeds above 8m/s. It is only below 8m/s where energy capture efficiency is low. It is therefore proposed to use a boost-type DC-DC converter to boost the DC output of the rectifier at low wind speeds so that the generator will operate at the optimum speed. At above 8-9m/s the DC output of the rectifier will reach the battery voltage, the converter will stop switching and the current will be carried by the boost diode, which will have to be rated appropriately. This represents a cost saving over a converter rated across the entire range as the switching transistor and smoothing capacitor will have a much

smaller rating and can be significantly cheaper. A further cost saving is achieved by using the generator inductance as the inductance in the boost converter.

As the converter cuts out when the DC output of the rectifier reaches the battery voltage, the converter cut-out wind speed will depend on the EMF produced by the generator and the battery voltage. A low generator EMF and high battery voltage will result in a high converter cut-out wind speed, leading to a large speed range and good power capture, but would require a large converter. A high generator EMF and low battery voltage will result in a low converter cut-out wind speed and a small converter, which will limit the maximum generator speed, leading to reduced power capture at higher wind speeds. Because of this, it is vital to match the generator EMF and the battery voltage to achieve the optimum converter cut-out wind speed, which is a compromise between power capture and converter size and cost.

2.3.2 Tracking Algorithm

If the generator resistance is ignored, the generated power output of a wind turbine is related to the wind speed cubed, when the turbine is operating at the optimum speed. At the optimum speed, the tip speed ratio will be constant, so the rotation speed will be proportional to the wind speed, i.e.

$$\begin{aligned} P_{\text{gen}} &\propto {v_{\text{wind}}}^3 \\ P_{\text{gen}} &\propto {\omega_{\text{gen}}}^3 \end{aligned} \tag{2.2}$$

Ignoring resistance, the generator voltage will be proportional to the rotation speed. Combined with Equation 2.2 this gives:

$$\begin{aligned} P_{\text{gen}} &\propto {V_{\text{gen}}}^3 \\ I_{\text{gen}} &\propto {V_{\text{gen}}}^2 \end{aligned} \tag{2.3}$$

Equation 2.3 can be used as the basis of a tracking algorithm [16]. The generator voltage is measured, and the corresponding current demand for the DC-DC converter calculated, based on the assumption that the generator is operating at the optimum speed for the current wind speed. If the speed is below the optimum then the DC-DC converter will be drawing less power than the turbine is producing and the turbine

will speed up toward the optimum speed. If the speed is above the optimum then the converter will be drawing too much power and the turbine will slow down. This way the maximum power operating point of the turbine is tracked without requiring the measurement of the wind speed or the turbine rotation speed.

The actual I_{dc} vs. V_{dc} curve of the system, taken from the simulation described in Section 2.1, is shown in Figure 2.7. The DC values of voltage and current should be proportional to the AC values. A quadratic relationship was found to fit the measured values best, with a simple squared relationship being less accurate. This can be attributed to the resistance of the generator, which is not insignificant in an air-cored machine due to the large number of turns needed to produce the voltage. The effect of the resistance is to make the ideal rotation speed slightly higher than the speed where the turbine would give maximum power output. This increases the generator voltage, lowering the current, and reducing the effect of the resistance.

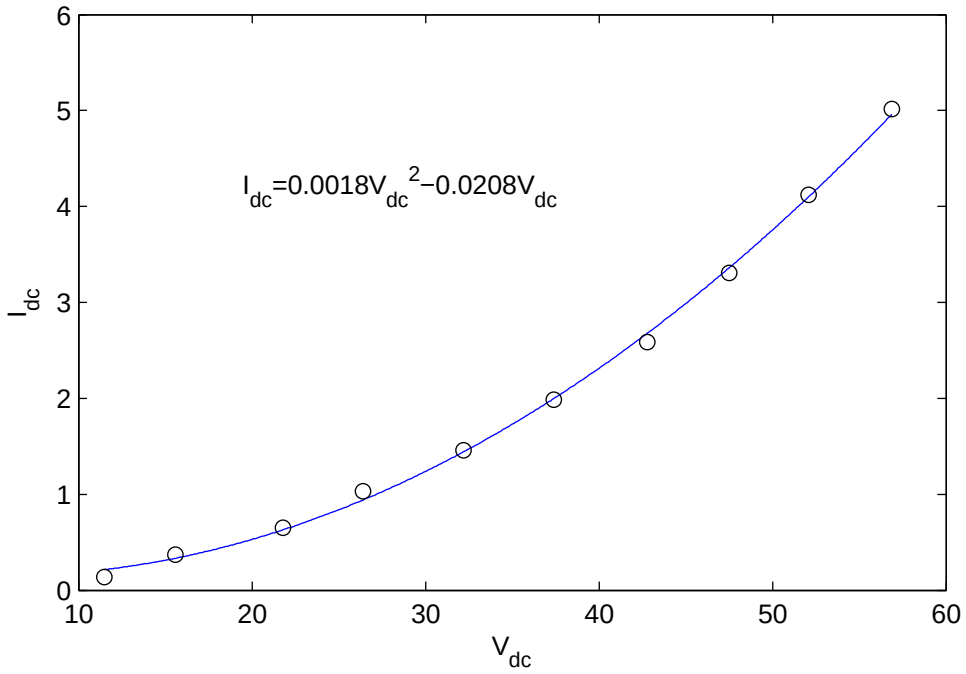


Figure 2.7: V_{dc} vs. I_{dc} relationship at maximum power.

2.3.3 Operating Range

The operating range of the turbine and power electronic interface is summarised in Table 2.3. The boost converter will cut in at 3m/s wind speed, with the current and voltage after the rectifier at 0.36A and 16V respectively. The boost converter will

operate to track the maximum power operating point until the wind reaches around 9m/s, at which point the current and voltage after the rectifier will be 3A and 52V respectively. A circuit breaker will be used to disconnect the generator when the coil current reaches 14A, in order to prevent the coils overheating. This corresponds to a DC current of 17A, which would occur at a wind speed of 18.5m/s.

	Wind speed	Generated power	Generator speed	DC voltage	DC current
Power electronics cut in	3m/s	5.8W	69RPM	16V	0.36A
Power electronics cut out	9m/s	165W	216RPM	52V	3.5A
Generator cut out	18.5m/s	1200W	440RPM	78V	17A

Table 2.3: Turbine operating range

2.4 Implementation of the Power Interface

2.4.1 Boost Converter Implementation

The circuit for the boost converter is shown in Figure 2.8, which does not include the rectifier to convert the 3-phase AC from the generator to DC, or the circuit breaker on the input side. The machine inductance is used for the boost inductance, in order to reduce costs. A shunt resistor is used to measure the current and potential dividers to measure voltage, again to reduce costs, and because galvanic isolation is not required. The circuit was designed for a power electronics cut-out wind speed of 15m/s, with the actual cut-out of 9m/s the transistor Q1 and capacitor C1 can be much smaller. The completed converter is shown in Figure 2.9.

2.4.2 Controller Hardware Implementation

For the controller a PIC16F876 microcontroller was chosen. This has many peripheral functions on board, such as ADC, PWM and serial communications, and uses very little power, but has the disadvantage of limited signal processing power. It was felt that a more powerful microcontroller or DSP would have unreasonable power supply requirements and a high cost. The controller is shown in Figure 2.10.

The current measurement from the shunt resistor is amplified using a differential amplifier and the voltage measurements buffered. As the input voltage is PWM

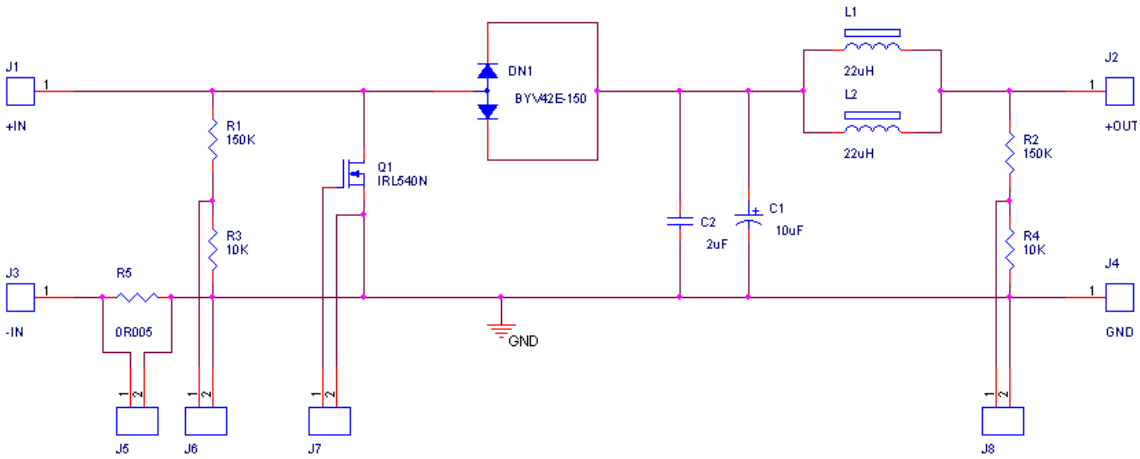


Figure 2.8: Boost Converter Circuit

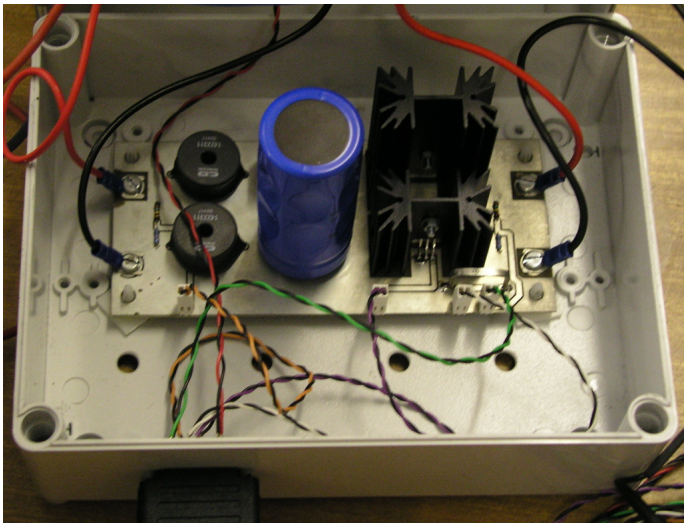


Figure 2.9: Completed Converter

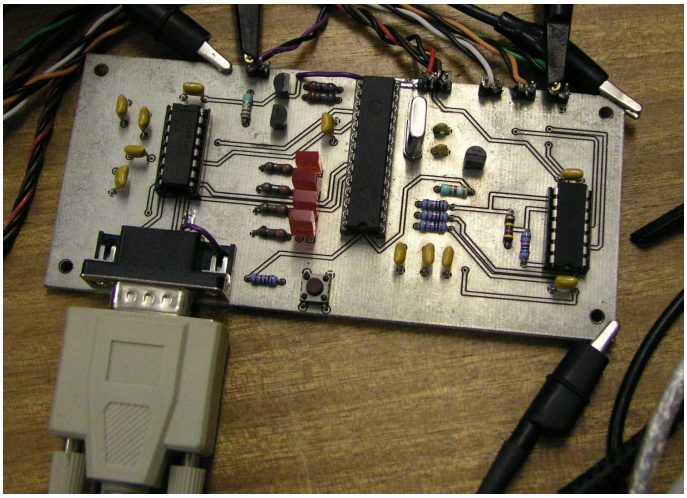


Figure 2.10: Completed Control Board

switched, an average voltage is derived using a first order R-C filter at 1KHz, with the other measurements also being filtered. The measurements are converted to digital using the ADC on the PIC microcontroller.

The PWM signal for the MOSFET is provided by the digital PWM on the microcontroller. This removes the need to use a separate PWM chip, which would also require a DAC to supply the analogue input. Using a 4MHz clock on the microcontroller will give a 16KHz PWM signal with 8 bits of accuracy (256 steps).

Communications are carried out using the serial port on the microcontroller, connected to an RS232 transceiver to provide the correct RS232 voltages.

2.4.3 Controller Software Implementation

The software run by the microcontroller consists of two control loops. The first one controls the input current to the converter, and the second implements the tracking algorithm by setting the current demand for the first loop based on the input voltage.

Voltage and current are sampled at 1KHz. The input voltage and current are filtered with a 2-pole butterworth digital filter with a cut-off frequency of 20Hz in order to eliminate the effects of the 6^{th} harmonic ripple from the rectifier, and obtain an average value. This is necessary as the microcontroller is not fast enough to control this ripple out using the converter.

Current is controlled by incrementing or decrementing the duty cycle depending on whether the current is less than or greater than the demand current, in effect a slow integral controller. This was found to be more stable than a fast P-I controller, as the sampling speed of the microcontroller is slow compared with the response time of the converter. The second loop runs much more slowly, at around 10 times per second. The demand current is calculated from a quadratic function of the input voltage, shown in Figure 2.7.

2.5 Testing

The testing is concerned with the operation of the hardware, and uses a laboratory prototype of the generator, shown in Figure 2.11. An actual turbine was not available, so it was not possible to test the tracking algorithm in real world conditions, so the operation of the complete system was simulated.

Figure 2.11: Generator Prototype

2.5.1 Converter Operation

The main question in testing the converter was how it would react to having the inductance on the other side of a rectifier, particularly because the rectifier was situated approximately 1m away from the converter, and connected with cables. There was also a question of parasitic capacitance in the wiring, and how this would affect the voltage waveform.

Testing was carried out with the generator driven at a fixed speed and the converter operating with a fixed duty ratio. The phase current was measured using a hall-effect current probe, and the phase-to-neutral voltage with a high voltage differential probe.

The results for one phase are shown in Figure 2.12. The current is what is expected for a passive rectifier feeding a constant voltage, but also including current ripple from the PWM switching, which is low. The voltage shows considerable over voltage spikes, up to twice the normal voltage. This is more easily seen in Figure 2.13, which shows the switching waveform, where considerable ringing can be seen on the switching transitions. This is likely to be due to the interactions between the inductance and parasitic capacitance of the connecting leads, and has

been observed in PWM-inverter-fed motors [17].

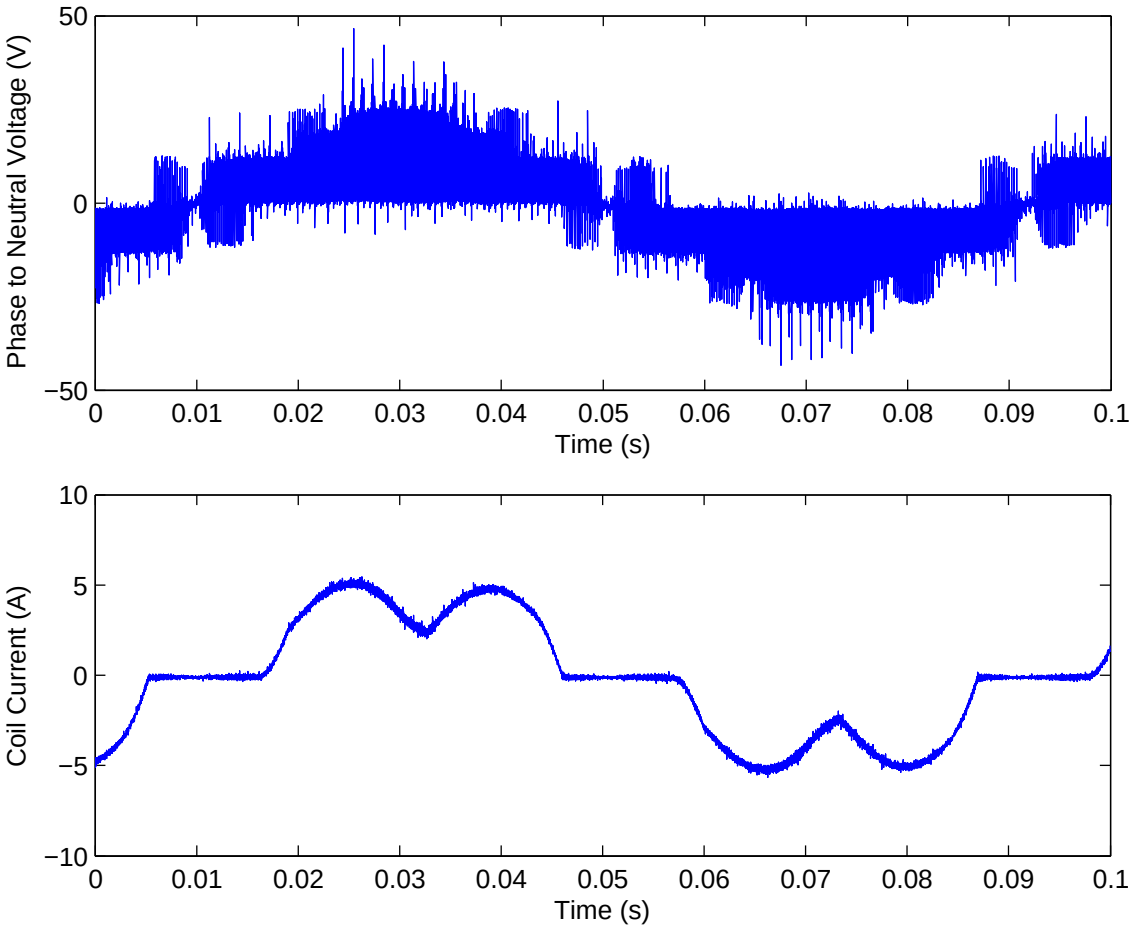


Figure 2.12: Coil voltage and current for one machine EMF cycle.

The voltage spikes are significantly lower on the DC side of the rectifier, meaning that the switching MOSFET does not need to be rated for a higher voltage. The voltage spikes increase the insulation requirements in the machine, but the prototype machine was insulated to 415V, so this is within the acceptable range.

2.5.2 Tracking Algorithm Operation

The motor driving the generator in the laboratory is an induction motor controlled by a simple V-F controlled inverter, so the system can only be run at fixed speeds, and does not have the capacity to simulate connection to a wind turbine. Because of this limitation, testing of the tracking algorithm consisted of varying the motor speed to give a different voltage at the generator terminals and measuring how the controller sets the DC current. Measurements were crude due to a speed oscillation

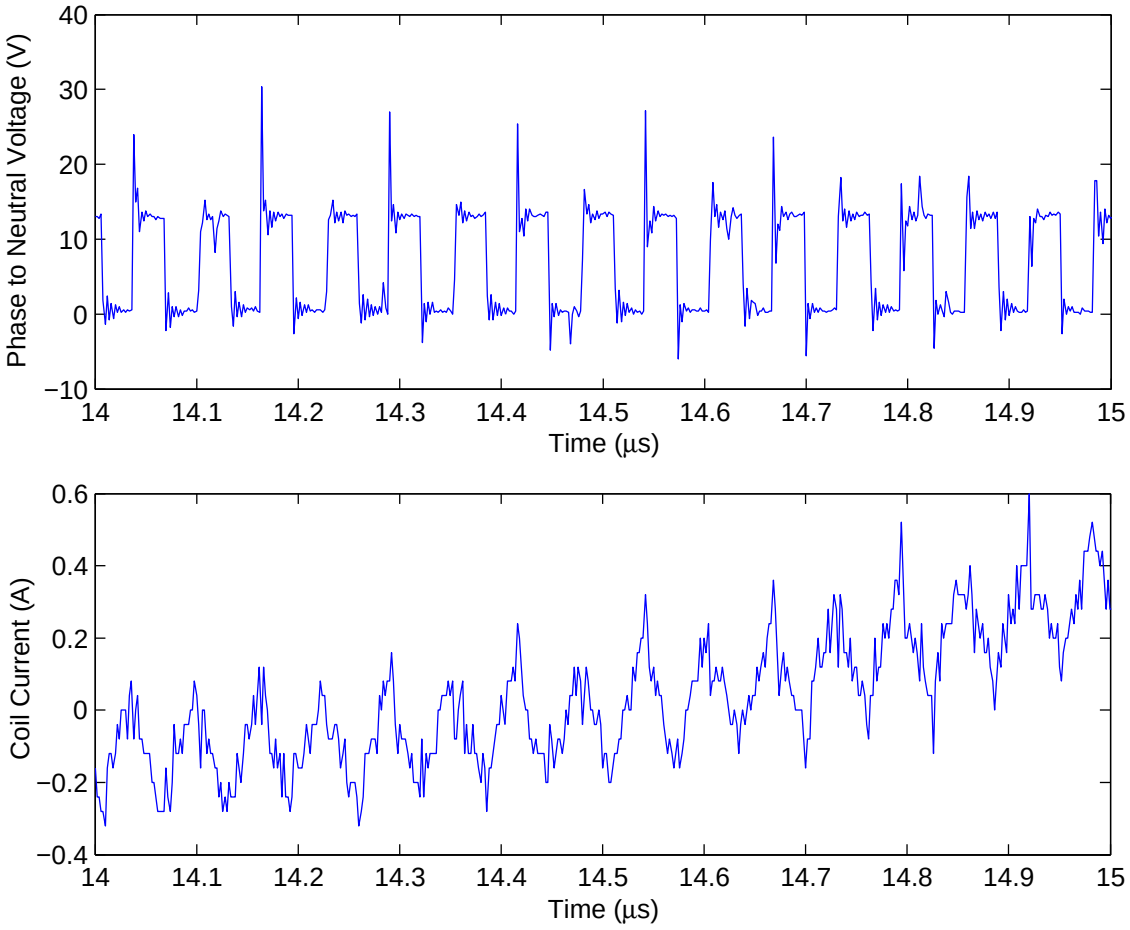


Figure 2.13: Coil voltage and current at PWM switching scale.

of around 1Hz caused by problems with the belt drive, and could not be re-taken as the equipment needed to be used for other projects. The results are shown in Figure 2.14 below, and show an accurate tracking of the desired current.

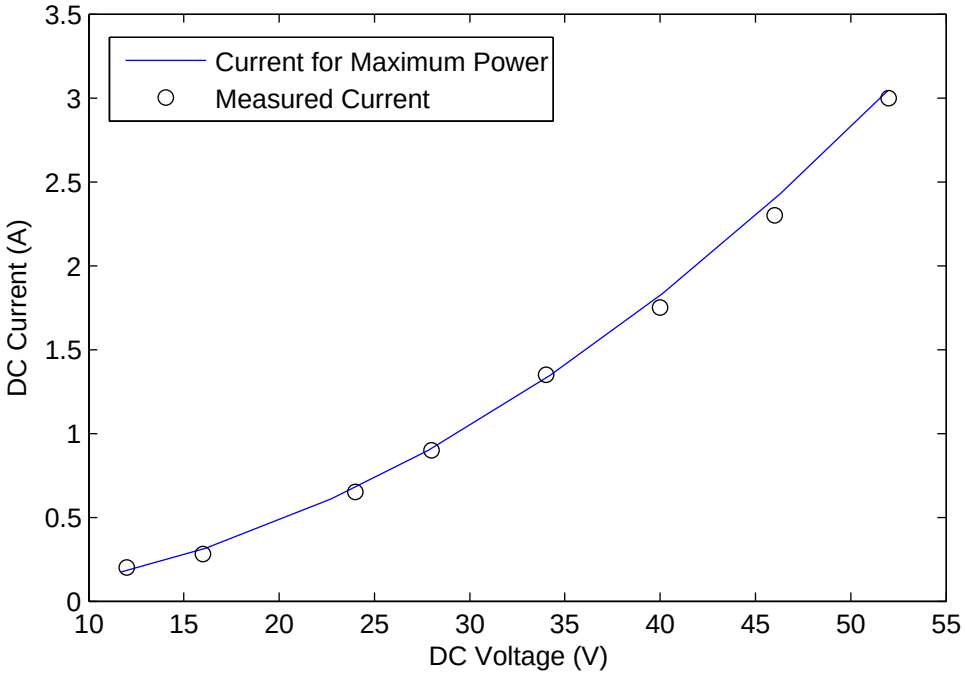


Figure 2.14: Measured and desired current vs. voltage.

2.6 Simulation and Analysis of System Operation

Simulation and analysis must perform two tasks:

- Determine the ability of the tracking algorithm to track the maximum power operating point of the turbine, in realistic simulated wind conditions at different average wind speeds.
- Determine the energy gain over the course of a year of using the power tracking system, compared with a direct battery connection.

2.6.1 Simulation of the Tracking Algorithm

Simulation was carried out using Simulink, and the SimPowerSystems blockset, and the model is shown in Figure 2.15. To keep the simulation time down, the switching of the DC-DC converter was not simulated, and was represented as a thevenin source

as in the simulation of Section 2.1. The voltage of the source was varied in the same way as the duty cycle of the converter in the actual implementation.

Wind speed data was generated randomly in Matlab, using a recognised technique, and read from a table in the Simulink model. The model was simulated for a simulation time of 5 minutes, for average wind speeds of 5, 7 and 9m/s, and for connection with and without the converter. The theoretical maximum power was also calculated.

Results for the 5m/s average wind speed are shown in Figure 2.16. Average powers for all three wind speeds are summarised in Table 2.4. It can be seen that the inertia of the turbine prevents it tracking the ideal rotation speed as this varies too quickly. However it can be seen in Table 2.4 that the extracted power is only slightly less than the maximum power, and it is also much more constant.

	Average Power (W)		
	5m/s wind	7m/s wind	9m/s wind
Maximum	27.9	74.7	162.4
Connection through converter	25.6	71.5	157.3
Direct connection	8.2	64.2	157.2

Table 2.4: Average power extracted

2.6.2 Estimate of Annual Energy Capture

The probability distribution of wind speeds can be calculated in most common cases using the Rayleigh distribution. The probability that the wind speed is greater than a value v is given by Equation 2.4 [18].

$$F(U) = \exp\left(\frac{-\pi}{4}\left(\frac{v}{\overline{v}}\right)^2\right) \tag{2.4}$$

Where $\overline{v}$ is the average wind speed. From this the probability distribution can be calculated, and this is multiplied by the power curves calculated in Section 2.1 in order to obtain the power density. The speed distribution for an average wind speed of 5m/s (typical of the Durham area) is shown in Figure 2.17, and the power density curves for the different connection systems are shown in Figure 2.18. The power curves assume the the power extracted is similar to what would be the case if the turbine could react instantly to changes in wind speed.

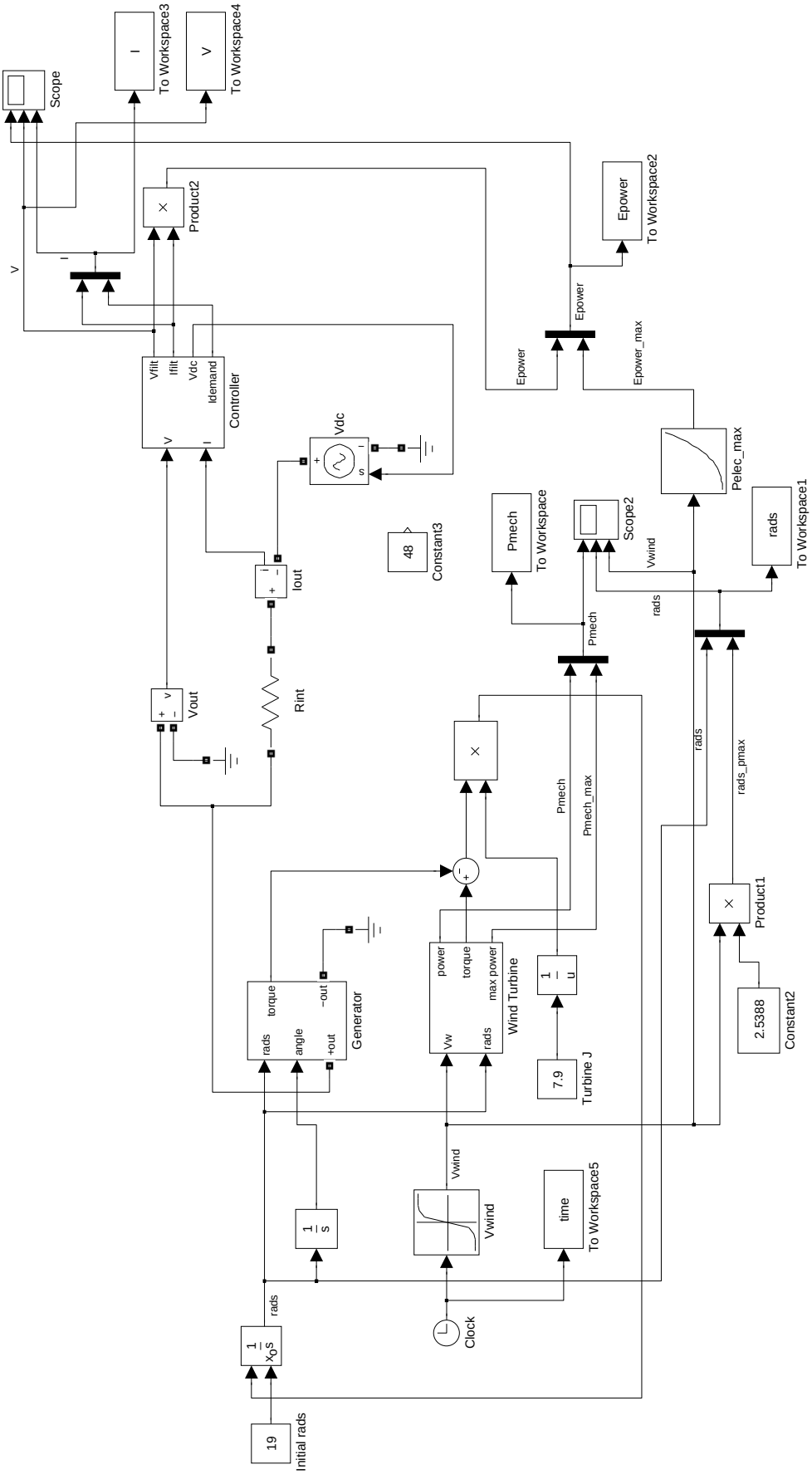


Figure 2.15: Simulink model used for testing the tracking algorithm.

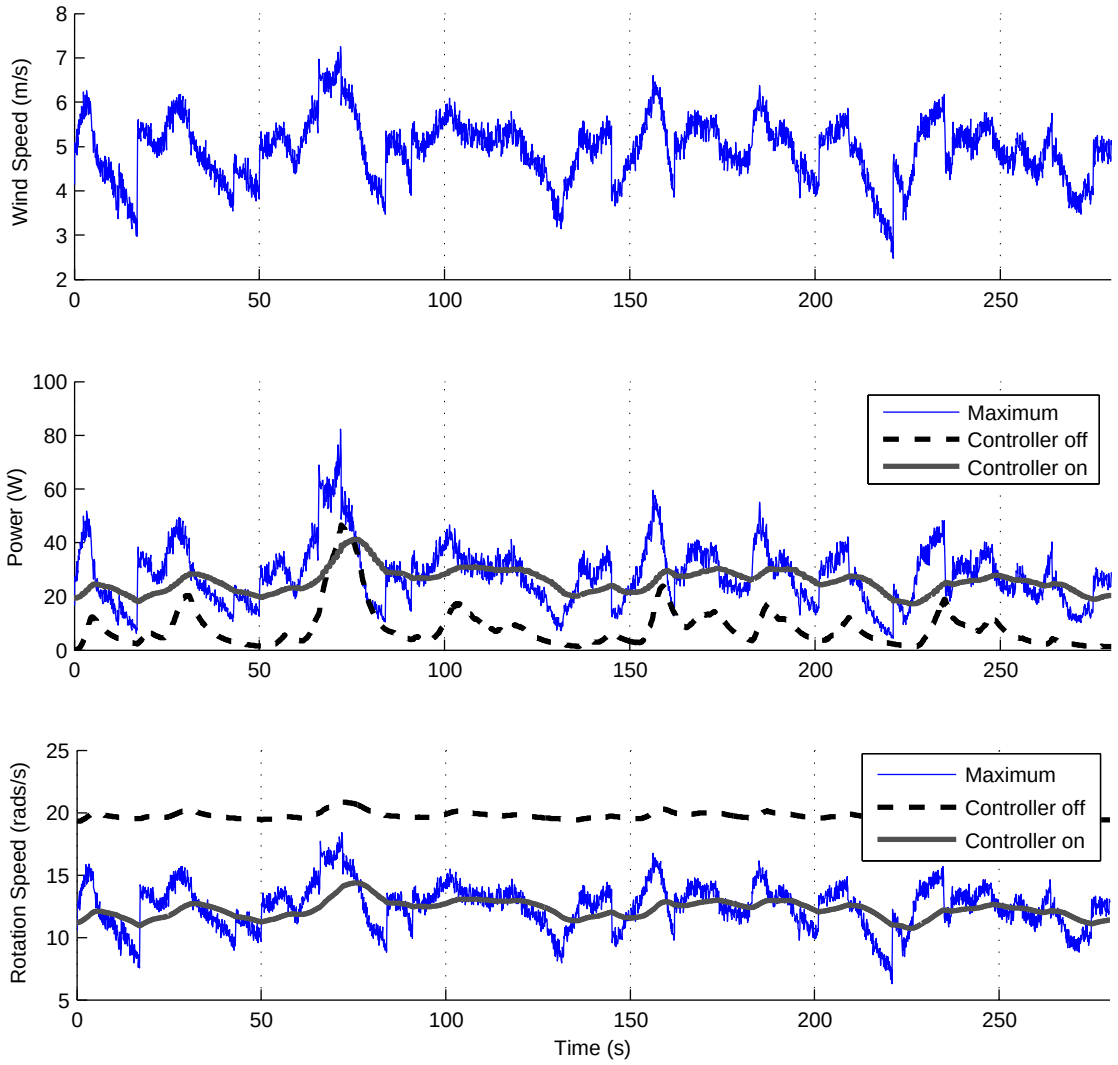


Figure 2.16: Tracking results for 5m/s average wind speed

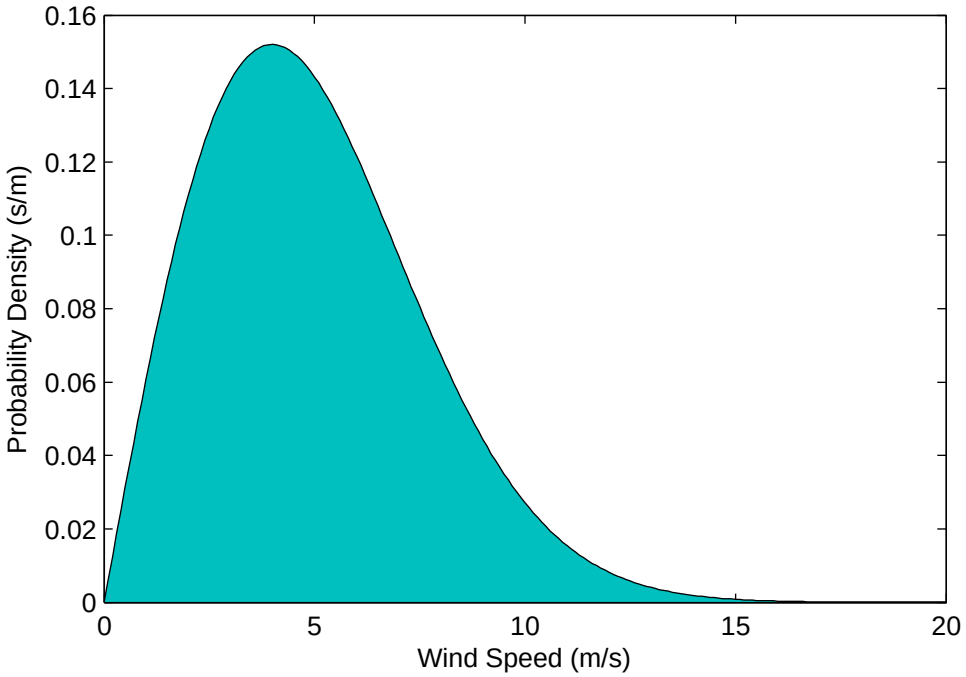


Figure 2.17: Wind speed distribution for 5m/s average wind speed

The areas in Figure 2.18 show the average power extracted over one year. The power gain at low wind speeds from having the proposed partially-rated boost converter over the direct battery connection is clear. At higher wind speeds power lost by limiting the DC voltage to 48V is small. At 7m/s average wind speed, shown in Figure 2.19, the power gain at low wind speeds is less significant while the power loss at high speeds is more so. There is also a power loss compared with the maximum due to the cut-off speed of the generator due to the generator current limit.

The average power is obtained by integrating the probability density function, and this is then multiplied by the time for one year to obtain the annual energy extraction. The total annual extraction for several wind speeds is shown in Table 2.5 and a comparison of the partially rated converter and maximum power are in Table 2.6. These also include extraction for a fully-rated converter, which can track the maximum power operating point of the turbine until the coil current reaches the maximum value.

It can be seen that the energy capture is improved at low average wind speeds, although the result is less significant at higher speeds. At higher wind speeds there is a significant difference between the extracted energy with a converter and the theoretical maximum. This is mostly due to the generator being cut out above

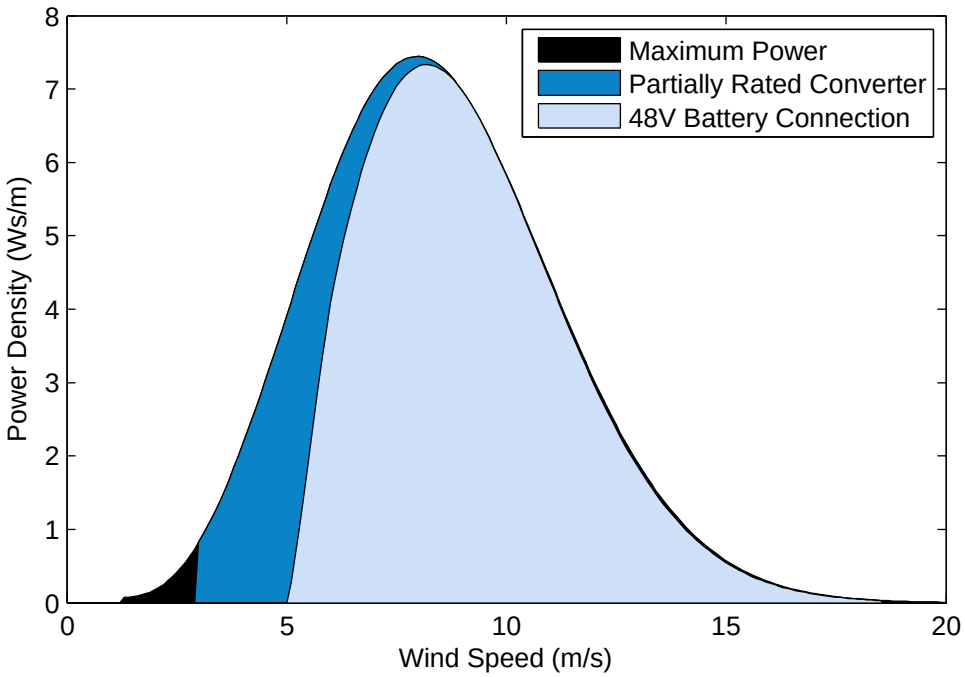


Figure 2.18: Power density for 5m/s average wind speed

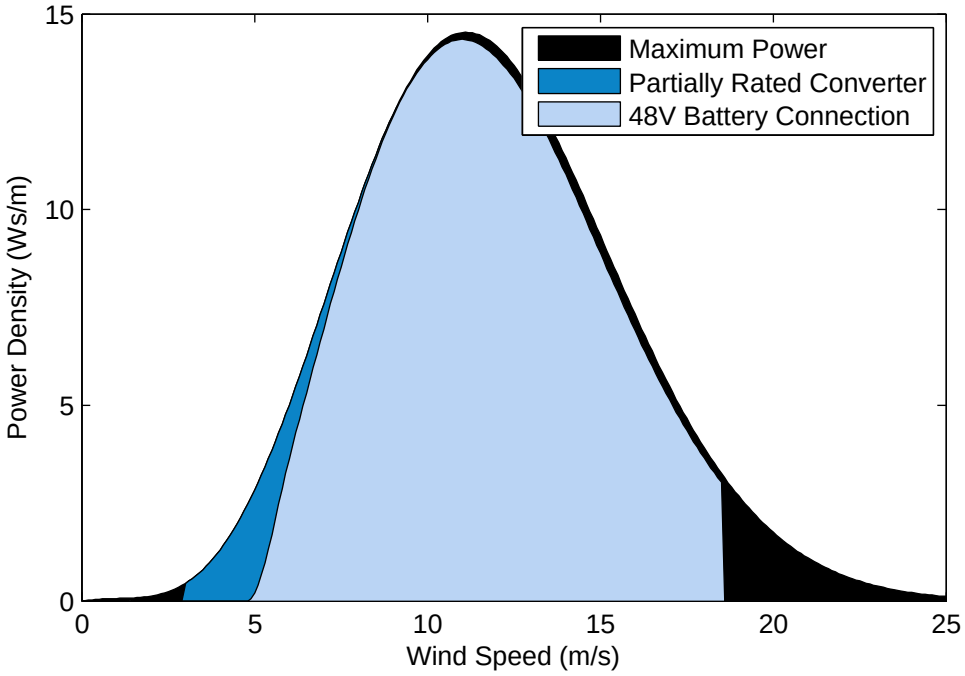


Figure 2.19: Power density for 7m/s average wind speed

Average wind speed (m/s)	Annual energy capture (kWh)			
	Battery	Part Converter	Full Converter	Maximum
5	371	451	453	454
6	690	762	771	779
7	1083	1144	1168	1229
9	1848	1891	1954	2520

Table 2.5: Annual energy capture

Average wind speed (m/s)	Partially rated converter		Fully rated converter	
	Increase over battery (kWh)	Percentage increase	Increase over battery (kWh)	Percentage increase
5	80	21.6%	82	22.1%
6	72	10.4%	81	11.7%
7	61	5.6%	85	7.9%
9	43	2.3%	106	5.7%

Table 2.6: Comparison of partially and fully rated converters

18m/s wind speed. The fully rated converter improves on the energy capture further, especially at higher average wind speeds, but would increase the cost. The fully rated converter considered here would track the maximum power operating point until the maximum current is reached, at which point it would disconnect. It would also be possible to keep the current at the maximum while increasing the speed above the maximum power operating point, reducing the turbine efficiency but allowing power extraction to continue. The maximum power would be limited by various factors including the maximum voltage of the converter, the maximum speed of the turbine and the maximum power into the batteries.

2.7 Conclusion

This work has shown the following:

- A low cost power tracking converter has been designed to operate with an axial flux permanent magnet generator driven by a savonius wind turbine.
- The converter allows more energy to be extracted from the wind than a simple passive rectifier.
- The energy saving depends on the wind resource and therefore the turbine site but is greater at lower wind speeds, as typically found in an urban location.

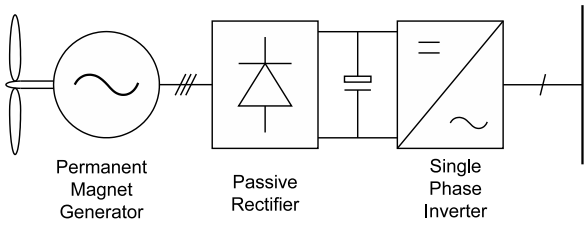
- A power tracking controller does not necessarily increase the cost of a wind turbine converter.

- A partially rated converter can extract a similar level of energy to a fully-rated converter at low average wind speeds, and is cheaper. A fully rated converter must either use a generator with a lower voltage, requiring high current components, or be able to reduce the voltage as well as boost, requiring an extra inductor.

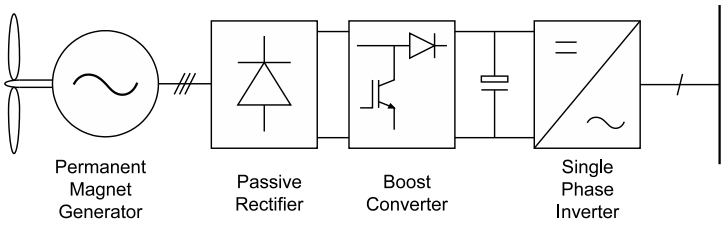
- The generator design is significant as it affects the wind speed at which the converter cuts out. A higher cut out speed will result in better performance at high wind speeds but also a more expensive converter.

Despite being designed around a battery charging application, this work also has applications in the grid connection of small-scale wind power. Small scale wind turbines are typically connected to the grid through a passive rectifier and a single-phase inverter, shown in Figure 2.20a. The inverter can only reduce the voltage, meaning that there is a minimum DC-link voltage and hence a minimum turbine speed. A boost converter between the rectifier and inverter, shown in Figure 2.20b, will allow a lower turbine speed, improving power capture at low wind speeds.

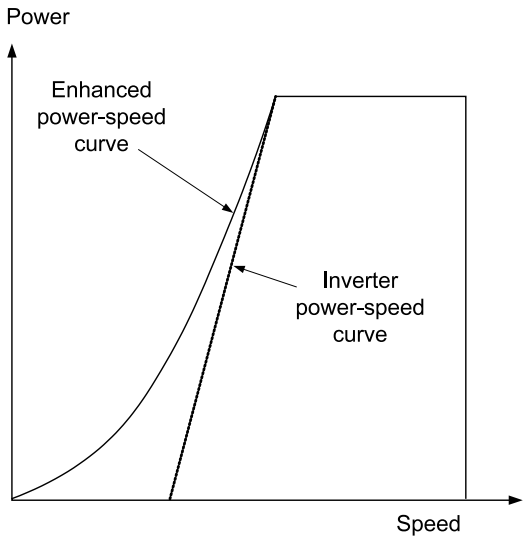
The currently available wind turbine inverters can also have fairly crude power tracking curves, and a separate boost converter could improve the power capture by following a more accurate characteristic, as shown in Figure 2.20c. Alternatively a learning algorithm could be implemented to learn the turbine maximum power characteristic, reducing the installation costs. Such an algorithm is described in [19].



(a) Grid connection using a single-phase inverter.



(b) Grid connection using a single-phase inverter and boost converter.



(c) Improved power capture using a boost converter interface.

Figure 2.20: Small scale wind turbine grid connection.

Chapter 3

Power Electronic Architecture, Turbine Steady State Control and Power Extraction

A modular power conversion scheme for the direct-drive wind turbine system, using a cascaded multilevel voltage source inverter for grid connection, has been proposed, and the implementation of such a system is the aim of this project. The power electronic architecture of the individual modules is not specified, and can have a significant impact on the control characteristics and power extraction capability of the wind turbine system. This chapter aims to evaluate a number of different module topologies, based on the control characteristics and power output.

The control and power output characteristics of the wind turbine system are derived partly from the characteristics of the turbine and partly from those of the generator and power electronics. The system under consideration in this project is based on a pitch-regulated horizontal-axis wind turbine, similar to the majority of large variable speed wind turbines in production. Pitch regulation has replaced stall regulation in multi-MW wind turbines, although stall regulation is still used in smaller turbines, including most domestic scale turbines such as the savonius turbine described in the previous chapter.

The turbine characteristics will be considered first, followed by the generator and power conversion characteristics. The generator and power conversion characteristics are strongly influenced by type of power conversion used, and this will affect the power capture of the turbine. Only the steady state characteristics will

be considered in this chapter, dynamic control requirements will be left to a later chapter.

3.1 Wind Turbine Characteristics

The characteristics of a wind turbine were covered in chapter 2 for the turbine used in the project, but will be covered again in this chapter in greater detail. In a wind turbine, as in any type of turbine, the power coefficient of the turbine is a function of the tip speed ratio [20]. The tip speed ratio, λ, is defined as the ratio of the tangential velocity of the rotor tip to the wind speed.

Using the tip speed ratio, the turbine coefficient of performance can be found using Equation 3.1, where P_R is the rotor power, C_p the power coefficent, or coefficient of performance, ρ the air density, v_w the wind velocity and A the swept area of the turbine rotor.

$$P_R = 0.5 C_p \rho {v_w}^3 A \tag{3.1}$$

The turbine coefficient of performance, C_p, is related to the tip speed ratio λ by the $C_p - \lambda$ curve. A typical $C_p - \lambda$ curve for a wind turbine is shown in Figure 3.1. It is clear that to achieve the maximum power output the tip speed ratio must be kept constant, at the value for maximum coefficient of performance. This means that the turbine speed must be varied proportionally to the wind speed, and this is carried out until the rated power of the turbine is reached.

Above the rated power of a turbine, the energy extraction must be limited so that the capacity of the grid interface equipment is not exceeded. Perhaps more importantly, the torque in the turbine drivetrain must be limited in order to protect the mechanical components, which would otherwise have to be massively over engineered for normal use. There are two ways of limiting the power: stall-regulation and pitch-regulation. In all the analysis in this chapter, $C_p - \lambda$ data are taken from [21].

3.1.1 Stall Regulation

If the turbine is operating at a tip speed ratio that is either higher or lower than the value for maximum performance, then the power output of the turbine will be

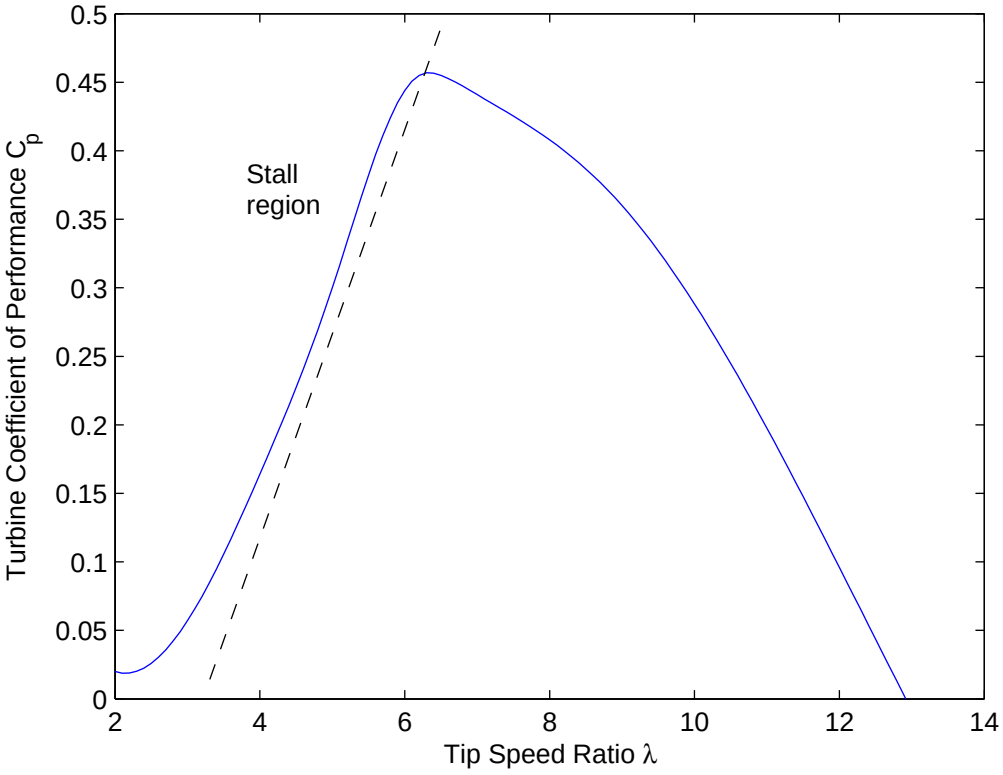


Figure 3.1: A $C_p - \lambda$ curve for a stall-regulated wind turbine

reduced. In a stall-regulated turbine the turbine power is limited by operating the turbine at a tip speed ratio lower than the ideal value, leading to aerodynamic stall, which reduces the extracted power.

This method of power regulation is mostly used in small scale and fixed speed turbines. In a fixed speed turbine, the limited maximum speed will cause the blades to stall, reducing the power. A variable speed turbine under stall regulation will be inherently unstable [22], as any gusts in the wind speed will cause the speed to increase, further increasing the power. This makes control difficult, and also applies large transient torques to the drivetrain, which is undesirable.

3.1.2 Pitch Regulation

The power output is limited in a pitch-regulated turbine by adjusting the blade pitch using mechanical actuators, in order to reduce the angle of attack, which decreases the aerodynamic lift on the blades and reduces the power. This method leads to a family of $C_p - \lambda$ curves for the different blade pitches, shown in Figure 3.2.

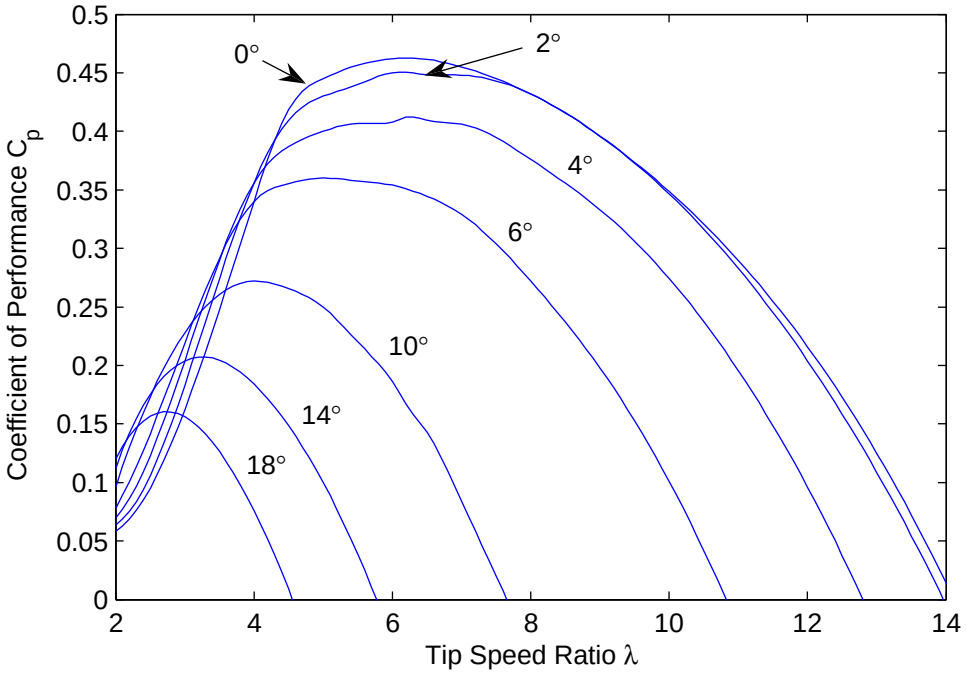


Figure 3.2: A $C_p - \lambda$ curve for a pitch-regulated turbine at various pitch angles

Pitch regulation reduces the transient torque in the turbine drivetrain and blades, meaning that these components do not need to be over-engineered, and will be more reliable and cheaper. This offsets the increase in cost and complexity of the

pitch control mechanism, which must be located in the blade hub. Pitch regulated turbines can also be quieter as the stalling process can be noisy. For these reasons, a pitch-regulated turbine will be used in this analysis.

3.2 Variable Speed Turbine Operating Regions

The operating region is usually defined in terms of power vs. turbine speed or torque vs. turbine speed, and represents a control characteristic which the turbine controller tracks. The turbine does not track wind speed directly as the wind speed varies over the swept area of the turbine, due to various factors including the wind shear closer to the ground and the back pressure from the hub, as well as the level of turbulence. For this reason it is almost impossible to calculate the average wind speed from a wind measurement at a single point [22]. Wind turbine operating regions are defined by various limits imposed by the different components. Some of these are listed below, and shown in Figure 3.3.

- Output power limit, usually dictated by the limits of the grid interface transformer, or the grid side converter in a fully-rated converter system.
- Torque limit, dictated by the limits of the strength of mechanical components, as well as the maximum current in the generator. A mechanical system which must withstand a high torque will be heavy and costly, so it is beneficial to be able to operate the system at a lower torque. The torque in an electrical machine is generally limited by the current in the coils and the coil area.
- Maximum speed, dictated usually by the maximum rotor power in a DFIG-based system, the maximum DC-link voltage in a permanent-magnet synchronous generator, as the EMF is proportional to rotor speed, or the maximum centrifugal force which the blades can withstand. Wound rotor synchronous machines can run at a higher speed if the field current is reduced, although torque is reduced as well, and the same results can be achieved with a cage-rotor induction machine using a vector-controlled drive.
- Cut-in speed, usually chosen because it is uneconomical to extract power below this wind speed. For instance, in a DFIG-based system at low speed power must be applied to the rotor, and this power must be supplied from the stator,

leading to a large amount of circulating power, leading to losses. A low rotation speed could also excite resonant modes in the turbine tower.

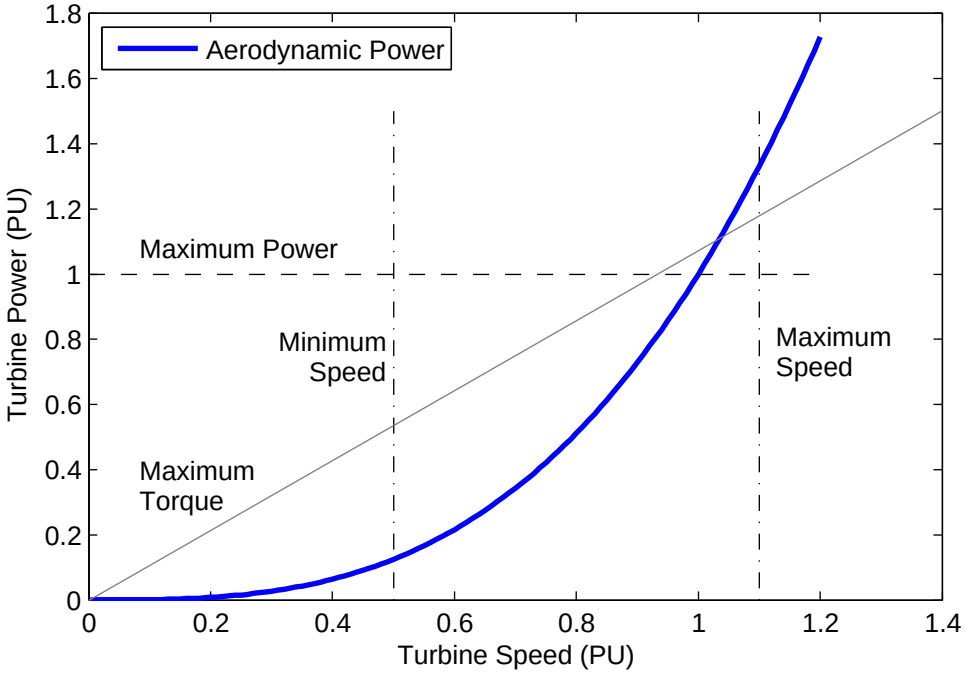


Figure 3.3: Operating limits for a wind turbine

3.2.1 Power Limited Operating Region

The simplest operating scheme, used in several studies of wind turbine operation [22] [5], is shown in Figure 3.4. In section A-B, the turbine speed remains constant at the minimum speed and the power increases as the wind speed increases. In section B-C the turbine speed tracks the maximum power operating point until rated power is reached. Once the rated power is reached, at the rated speed, the turbine remains at the rated power in section C-D, using pitch control to limit the rotation speed.

In section C-D the turbine is normally run above the rated speed, but below the maximum speed, this is done in order to smooth the power flow. The pitch control system has a time constant associated with it, so the pitch control mechanism cannot perfectly track the rated speed in rapidly changing wind conditions, and the generator torque cannot be increased to limit the speed. Instead the turbine speed is allowed to increase during gusts, before the pitch control mechanism is able to react to control it. During short dips in the wind speed the power extraction is held constant and the turbine allowed to slow down until the wind speed picks up again.

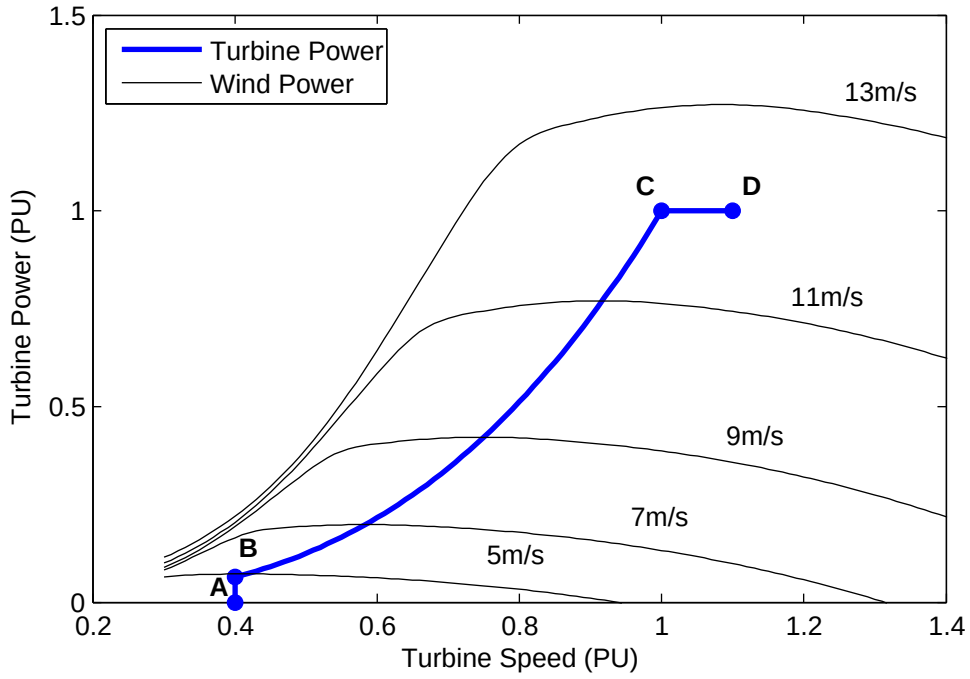


Figure 3.4: Wind turbine simple operating region

The power curve resulting from the simple operating region is shown in Figure 3.5, and can be seen to follow the turbine operating region closely.

3.2.2 Speed Limited Operating Region

A more complex operating region is shown in Figure 3.6, and features in several studies [23] [24] as being more representative of real wind turbine operation, particularly with DFIG-based systems. Operation in sections A-B and B-C is identical to the simple case above, the difference being that the maximum speed of the turbine is reached at point C, in this case at 70% of the speed of the simple case, before rated power has been achieved. In section C-D, the speed is held constant while the torque increases, with the turbine operating in the stall region. At point D the rated power of the turbine is reached and the turbine power is held constant at the maximum power, with pitch regulation used to regulate the speed in section D-E as in the simple case.

In section C-D the blade pitch is not changed, meaning that the turbine is operating in the stall region, which could result in significant noise. To reduce the noise the blade pitch could be increased to decrease the level of stall, which would reduce the power capture at that speed. The power curves for both the full power

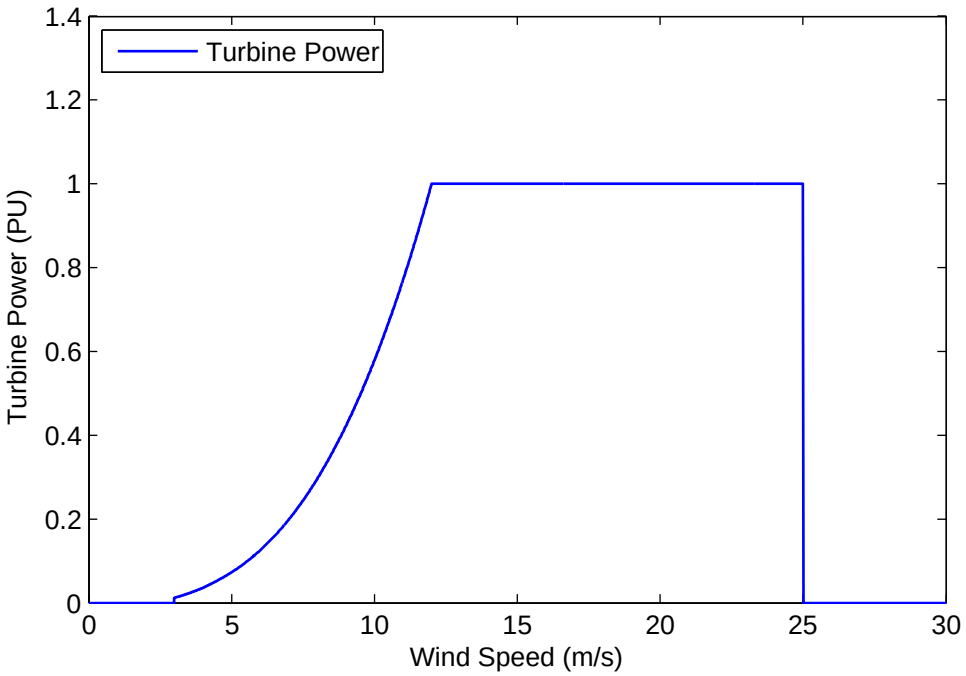


Figure 3.5: Power curve for simple operating region

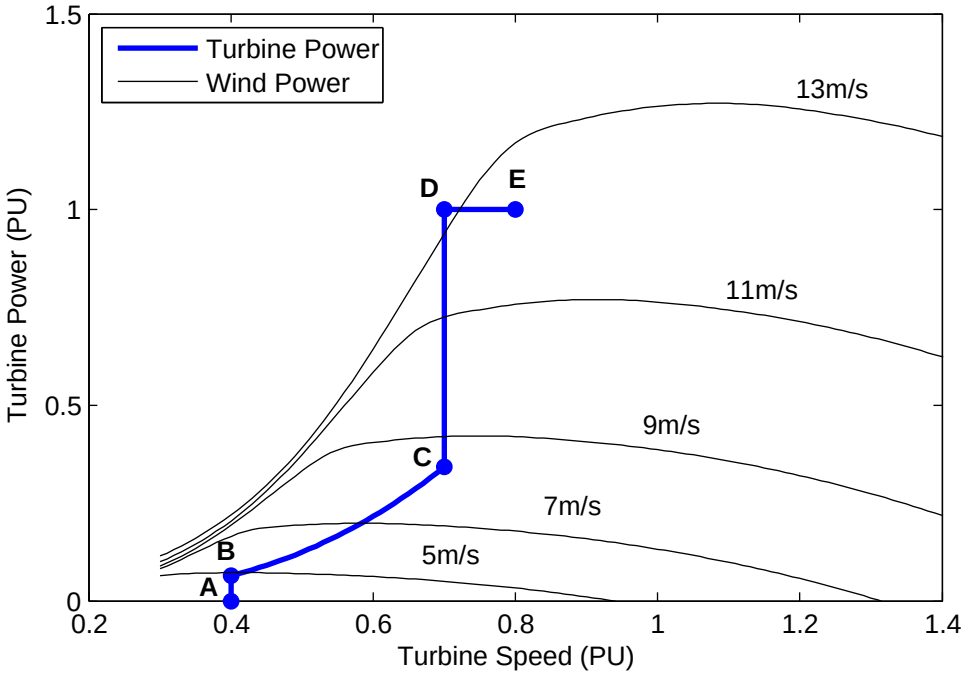


Figure 3.6: Speed-limited operating region

and the limited stall control methods are shown in Figure 3.7, in which the turbine speed remains constant above 8m/s wind. The results of such a control method can be seen in the power curve of the Vestas V80 turbine, shown in Figure 3.8, which offers different power curves with different noise levels in the stall region.

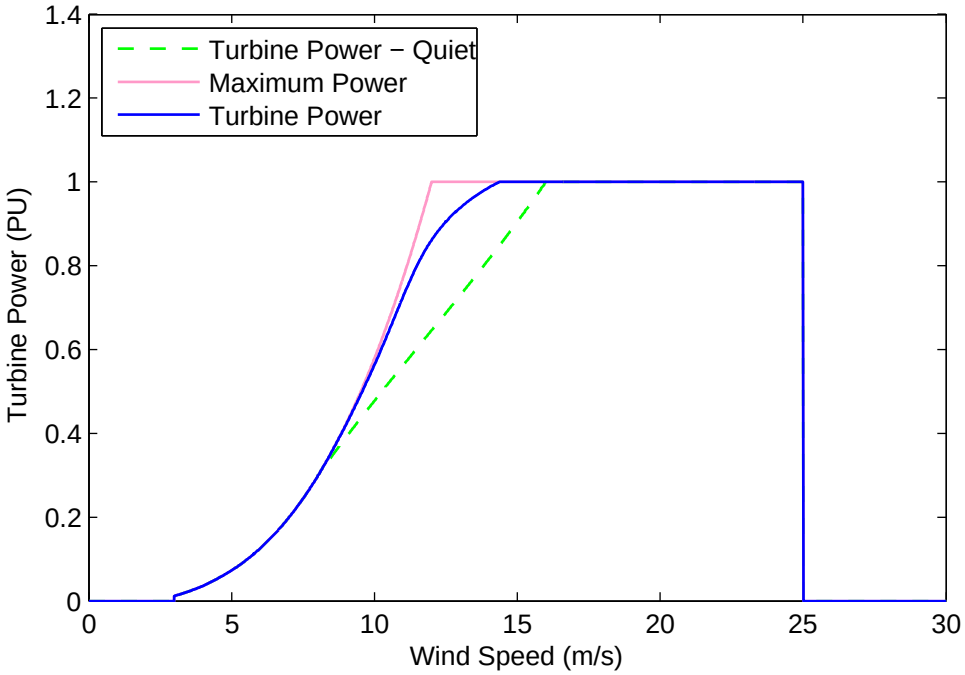


Figure 3.7: Power curve for speed-limited operating region

3.2.3 Torque Limited Operating Region

A third operating region can be used if the torque limit of the turbine drivetrain is reached before the rated power. This region is shown in Figure 3.9, for a turbine in which the torque limit is around 83% of the maximum torque in the simple case. In this case, maximum power tracking continues until the torque reaches the maximum at point C, at which point the torque is held constant and the speed increases in the region C-D. At point D the rated power of the turbine is reached and the turbine power is held constant at the maximum power, with pitch regulation used to regulate the speed in section D-E as in the simple case. The rated power is the same as that in the simple case as, while the rated torque is reduced by 83% the speed is increased by 20%.

The power curve for the torque-limited operating region is shown in Figure 3.10, and shows little difference from the maximum power region. Noise should be lower

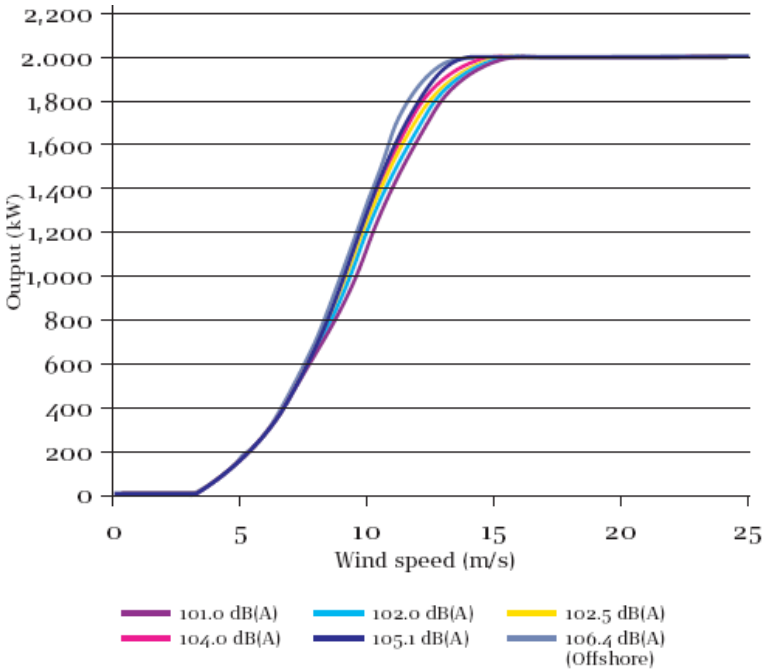


Figure 3.8: Power curve for Vestas V80 2MW turbine [25]

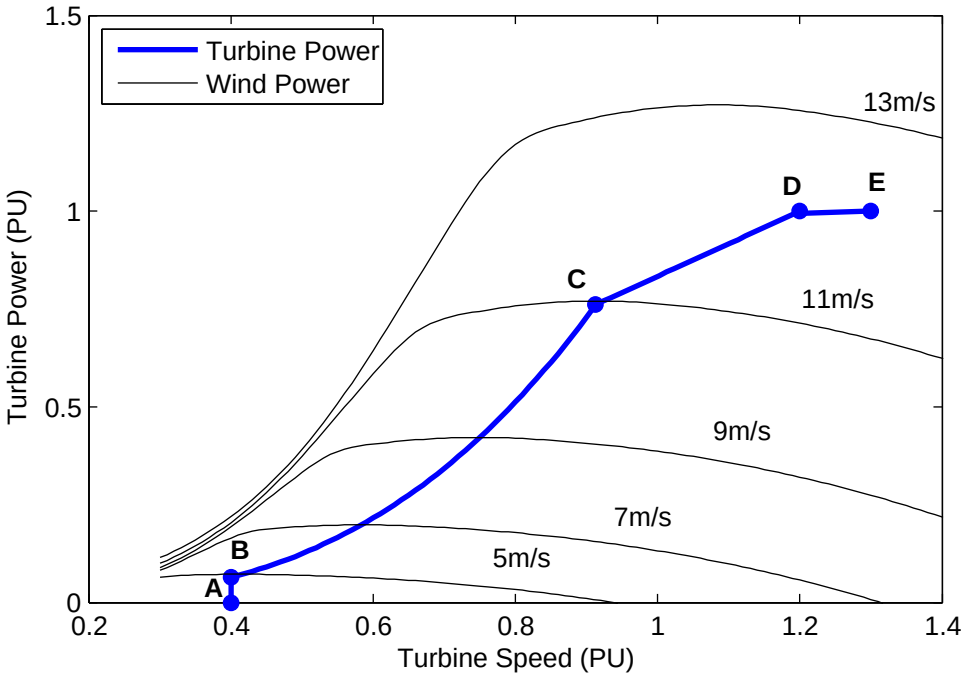


Figure 3.9: Torque-limited operating region

than the torque-limited case as the turbine is not operating in the stall region, but there could be an increase in noise over the simple operating region due to the increased turbine speed. Reducing the speed to reduce the noise will limit the total output power of the turbine.

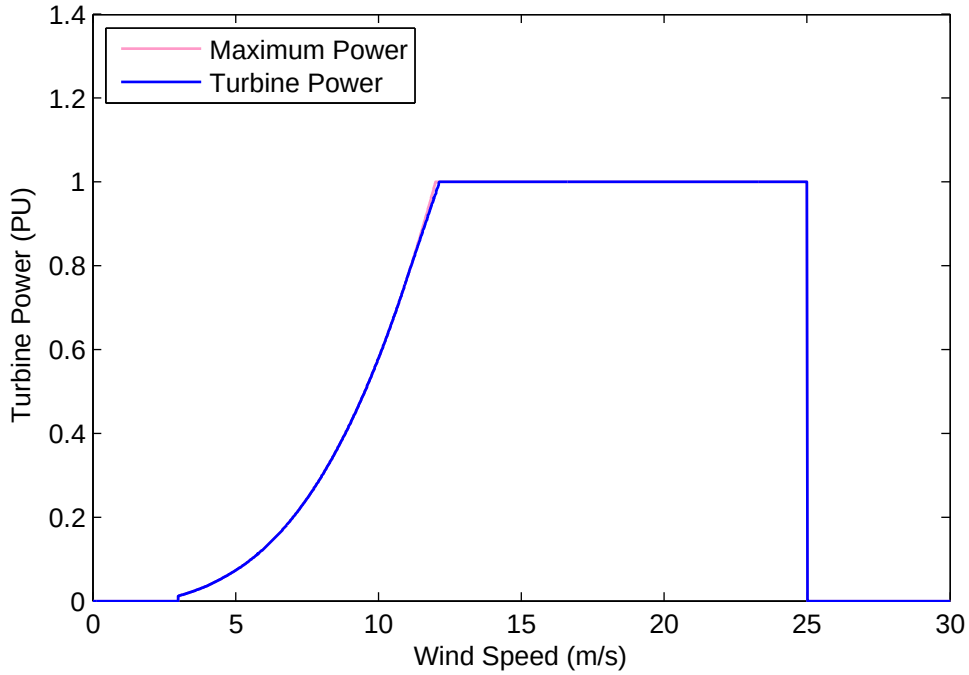


Figure 3.10: Power curve for torque-limited operating region

3.2.4 Choice of Operating Region

The speed-limited operating region is mostly associated with geared DFIG-based drive systems [23] [24], as the generator offers only a limited speed range, and the gear ratio can easily be selected to achieve the optimum maximum speed for the turbine blades. Power is slightly reduced compared with the ideal power tracking scenerio, especially if noise is to be controlled.

The torque-limited operating region is more interesting for permanent-magnet direct drive turbines, where the torque of the permanent magnet generator is limited by the allowable coil current. In this case a higher power output can be obtained from a given generator design than with the simple operating region, although the power electronic grid interface will need to be capable of handling the increased speed range of the generator, and the turbine blades the increased speed. This operating region is likely to be in use in the Zephyros Z72 wind turbine [8], in which

the power output in offshore applications is increased by increasing the maximum speed, although the noise level is increased.

3.3 Power Electronic Interface Architecture

In a turbine using a permanent-magnet direct-drive generator, the power electronic interface determines the speed range, and hence the power capture capability of the turbine. A grid interface has been proposed for a lightweight direct drive generator, and this is shown in Figure 3.11. A modular approach is used, with one or more coils connected to each module via a rectifier. The output of each module is a single-phase H-bridge inverter, with the outputs of the inverters being cascaded to form a cascaded multilevel voltage source inverter (CMVSI), allowing a high voltage output while using standard components in the modules. Modules will be mounted on the generator itself, and in order to minimise the voltage between adjacent modules while allowing a star connection the modules will be arranged into two parallel strings per phase.

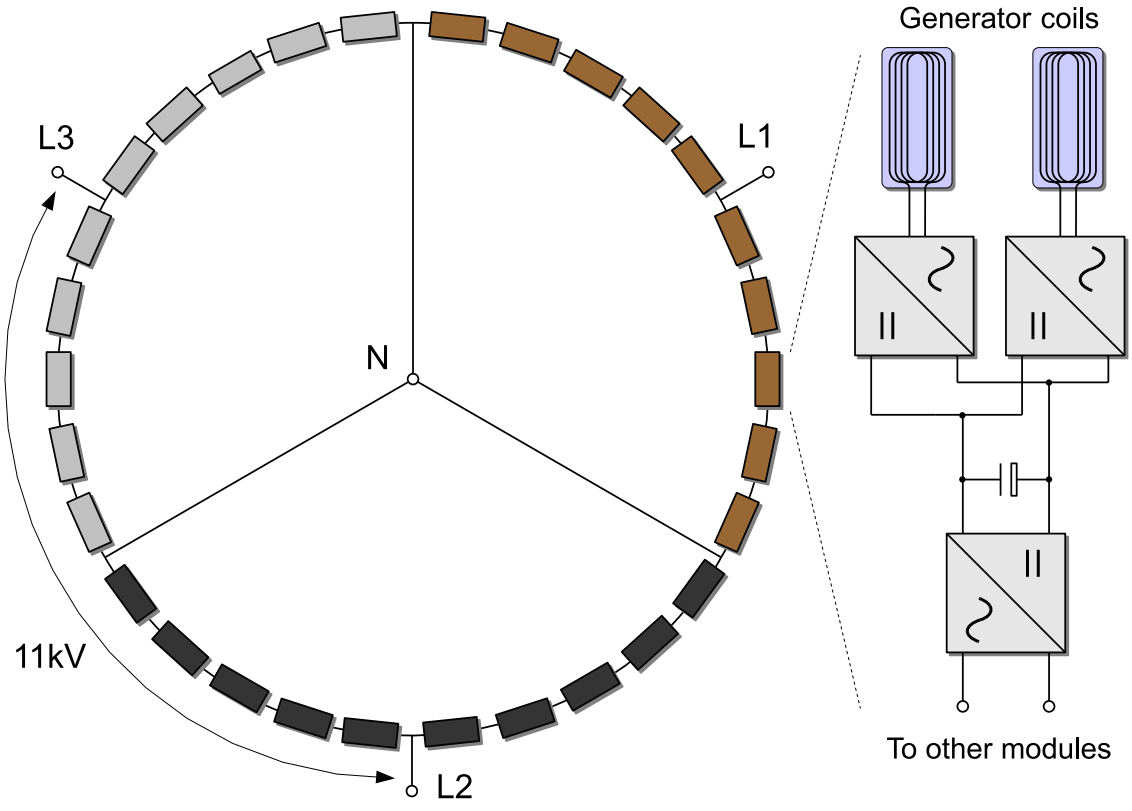


Figure 3.11: The proposed generator grid interface

The connection of the converter modules is shown in greater detail in Figure 3.12, which shows the connection of the series and parallel modules. The grid coupling inductance is not shown, and this must be included for each string of modules separately, either within the turbine nacelle or as many smaller inductors distributed between the modules. If two strings are connected in parallel without any inductance, then any difference in the switching instances of the modules in different strings will cause a massive current to flow between the strings if a module in one string has switched, and the corresponding module in the other string has not. Power sharing between the two strings will not be investigated.

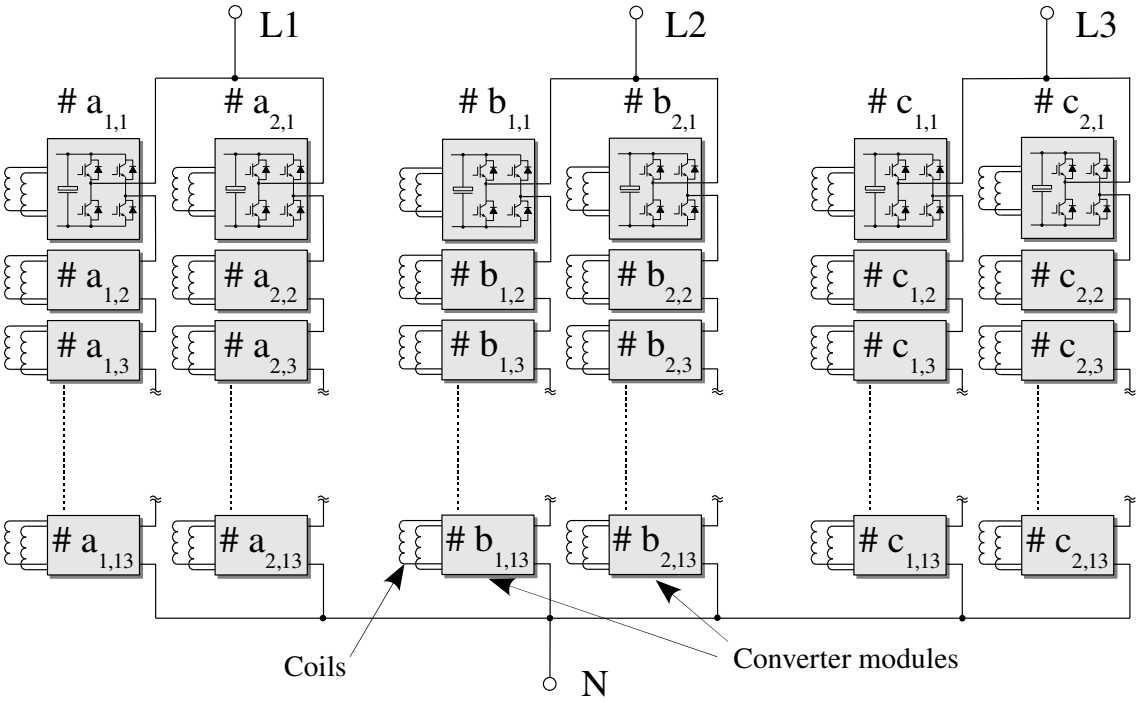


Figure 3.12: Converter module connection in greater detail

The operating region of the turbine depends on the type of rectifier used, as well as the modulation scheme for the multilevel inverter. Three possible solutions will be analysed, to calculate the difference in power extraction:

- Passive rectifier input with fundamental switching output. Control of the turbine is simple, but the grid voltage dictates the DC-link voltage of the modules, which effectively makes the turbine fixed speed.
- Passive rectifier input with PWM switching output. The PWM switching allows the DC-link voltage to vary, allowing variable speed operation. The

speed range is dictated by the allowed modulation depth of the PWM converter and the maximum DC-link voltage.

- Boost rectifier input with fundamental switching output. The fundamental switching of the output inverter fixes the DC-link voltage, but the boost rectifier allows the turbine speed to vary. The minimum speed is dictated by the maximum boost ratio of the boost rectifier.

It is also possible to use a boost rectifier and PWM output, but this will offer little increase in turbine speed variability, and hence the operating region will be the same as that of the turbine with boost rectifier and fundamental inverter switching. There are advantages associated with using PWM switching on the output but these will not be considered at this stage.

In calculating the power curves of the above solutions, the highly non-linear nature of the passive rectifier requires a numerical calculation of the speed variability of the turbine, similar to the analysis of the savonius turbine in the previous chapter. The boost rectifier is assumed to be able to draw a sinusoidal current from the coils, which allows standard electrical machine analysis techniques to be used.

3.4 Calculation of System Power Curve

3.4.1 Turbine and Generator for Analysis

Analysis of the operating regions and development work in subsequent chapters will be based on a 1.8MW turbine and generator design. The generator is a lightweight iron-cored design, using permanent magnets and an airgap winding, similar to the design described in [11]. Parameters for the generator are listed in Table 3.1, and the turbine parameters are listed in Table 3.2.

The electrical phase separation between adjacent coils is 135°, giving a machine with 8 phases, which was done in order to smooth the torque and power pulsations from using a passive rectifier. Two coils will be connected to each power electronic module, and these coils can be selected such that the phase separation is 90°, giving a constant power flow in total, if a sinusoidal current is drawn from each coil. With 162 coils this gives 81 modules, allowing a string length of 13 modules with two strings in parallel per phase on the grid side.

Diameter	7m
Rated speed	24.7rpm
Rated output power	1.87MW
Rated shaft power	1.94MW
Rated Torque	752kNm
Number of poles	216
Number of coils	162
Coil V (RMS)	410V
Coil I (RMS)	30.4A
AC frequency	45Hz
Coil inductance	7.6mH
Coil resistance	320mΩ
Number of modules	13 per inverter string

Table 3.1: Generator Parameters

Turbine diameter	66m
Maximum C_p	0.46
λ at maximum C_p	6.3

Table 3.2: Turbine Parameters

Turbine modeling is carried out using the same method as in Section 2.1. Based on the simple operating profile, the torque limit of the generator will be reached at a wind speed of 12.25m/s, when the turbine will be generating 1.736MW shaft power, and spinning at 22.1 rpm, and these will be selected as the rated wind speed, power and shaft speed of the system. In all cases a cut-in wind speed of 3m/s and cut out of 25m/s are used.

3.4.2 Fundamental Inverter Switching and Passive Rectifier

System Modelling

For this analysis one power electronic module is considered, and the results multiplied by the total number of modules to obtain the overall result. The DC link capacitance was assumed to be large enough that the voltage would remain constant and the effects of the inverter harmonics could be ignored. The required DC link voltage to give an output of real power P and reactive power Q from the inverter is given by Equation 3.2, where N is the number of inverter levels, V the peak grid phase voltage, L the line inductance and ω the line angular frequency.

$$V_{\mathrm{DC}} = \frac{1}{N}\sqrt{\left(V + \omega L\frac{2Q}{V}\right)^2 + \left(\omega L\frac{2P}{V}\right)^2} \tag{3.2}$$

The above is derived from the basic power relationship for a transmission branch ignoring the resistance [26]. It is assumed that each inverter module is operated in quasi square wave switching at fundamental frequency so that a good sine wave can be synthesized from the outputs of many inverter modules cascaded [27].

The system was simulated in Simulink, using the structure shown in Figure 3.13. The input to the model is the wind speed and demand of reactive power. In the majority of grid codes [28], a wind farm and indirectly a wind turbine may be required to operate with a specific reactive power demand which may be explicitly given or derived from a voltage or power factor control loop. The output of the model is the real power. The real power is determined together with the DC link voltage so that Equation 3.2 is satisfied and at the same time the turbine mechanical power matches the output real power and ohmic losses in the system. The rectifier power is used to calculate the mechanical torque, which is used to calculate the turbine speed using a mechanical model of the turbine.

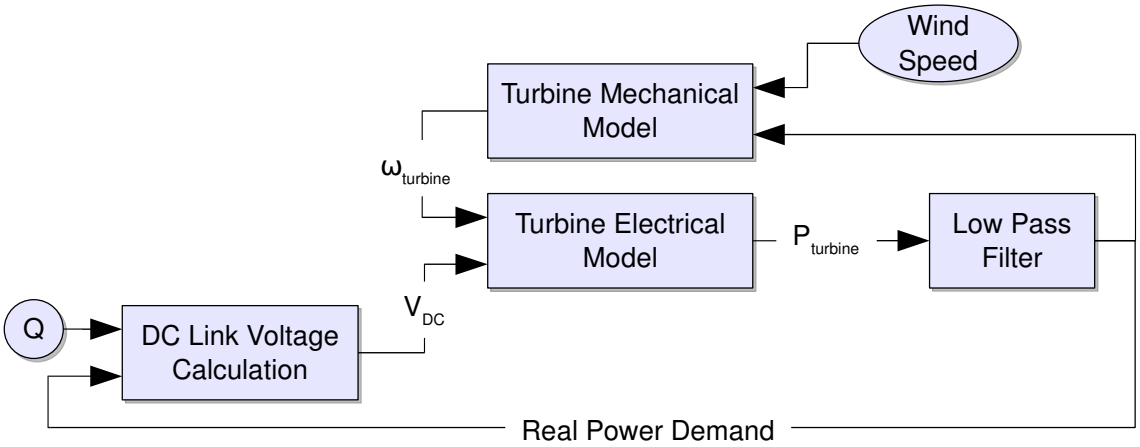


Figure 3.13: Simulation model structure

For a given DC link voltage and turbine speed the electrical model will give the electrical power output of the rectifiers. This is filtered to remove the second harmonic ripple from each of the diode rectifiers and used to calculate the required DC link voltage for the inverter according to Equation 3.2, which is fed back into the model. Thus the DC link voltage and turbine speed will move toward steady state values where the rectifier input power is equal to the inverter output power,

ignoring converter losses.

The simulation was run for wind speeds from 3m/s to 12.25m/s, with the latter being the rated speed. It is assumed that above the rated wind speed the turbine power output can be held at the rated power using pitch control. The simulation was run for unity power factor and reactive powers of 573kVAr lagging and 1081kVAr leading, corresponding to power factors of 0.95 and 0.85 at rated power, specified by the grid code [28]. A line inductance of 22mH was used.

The number of turns in the generator coils was selected such that the turbine would draw rated power at the rated wind speed and turbine speed, with the grid side voltage at 11kV line-to-line. While it was shown in Section 3.2.2 that limiting the speed to something below the ideal speed at rated power would only slightly reduce the power capture, doing so in this case would require a generator with a much higher torque rating.

Simulation Results

The results of the simulation can be used to calculate power curves for the system at unity power factor, 0.85 leading and 0.95 lagging power factors. It is assumed that above 12.25m/s wind speed the power output will remain constant until 25m/s when the turbine will cut off. The power curves corresponding to different power factors are shown in Figure 3.14. The maximum power is obtained purely from the turbine and generator characteristics without any constraints associated with the converter and reactive power requirement of the grid.

There is a reduction in the output of real power compared with the maximum, particularly below 10m/s wind speed. This reduction is affected by the reactive power output, with a leading power factor lessening the reduction while a lagging power factor increases it. At increased power levels, the commutation overlap in the uncontrolled rectifier could have an effect on the DC link voltage, although the low inductance of the coils means that the conduction interval is very low. Power is reduced at low wind speeds due to the almost fixed DC link voltage required by the inverter requiring a higher turbine speed than the optimum speed. This is shown in Figure 3.15.

Limited speed control is achievable by varying the reactive power output of the inverter, but the level of variation is small due to the low grid interface reactance

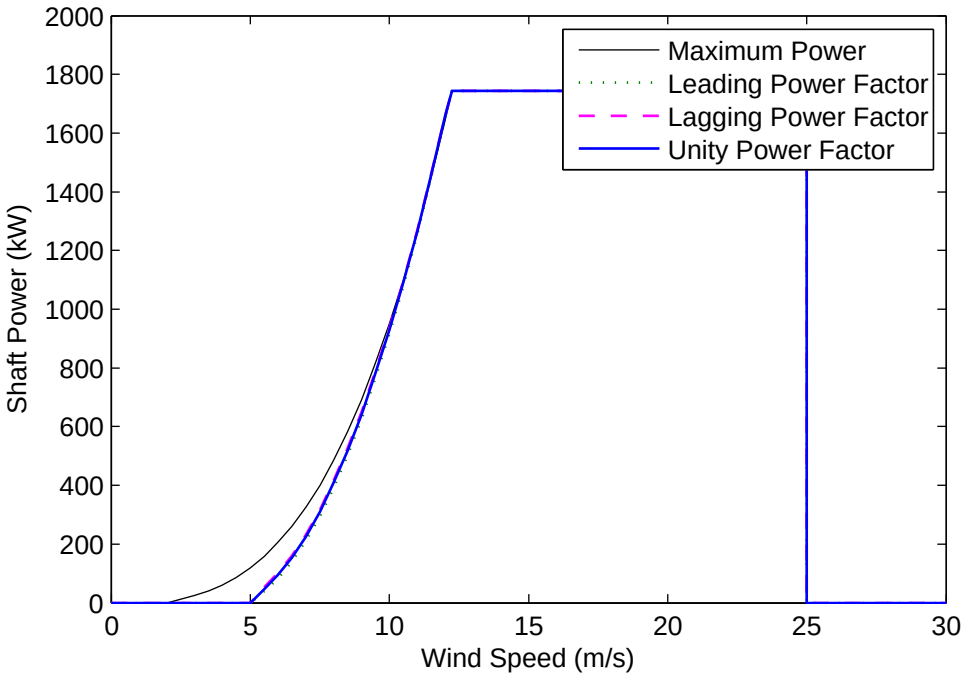


Figure 3.14: Simulated power curve for diode rectifier connection

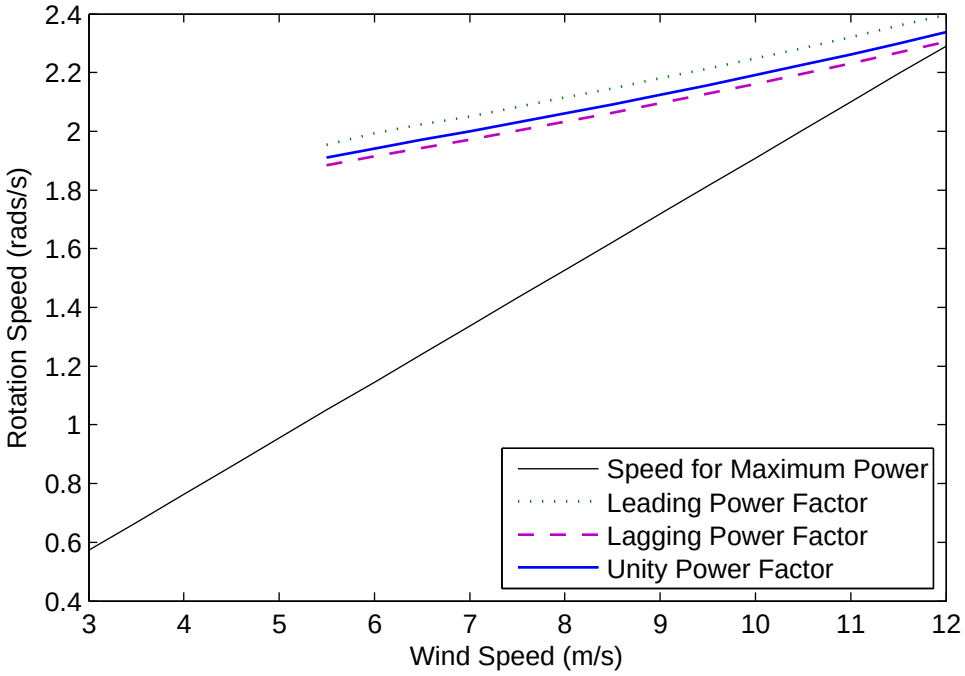


Figure 3.15: Simulated turbine speed for diode rectifier connection

of around 0.1p.u., so a large variation in reactive power would be required, which would need to be compensated. This has been documented in [29].

3.4.3 PWM Switching and Passive Rectifier

PWM switching of the inverter bridge allows the DC link voltage to vary independent of the grid voltage, allowing variable speed operation. At the rated wind speed of the turbine, the PWM switching of the inverter is used to reduce the apparent peak output voltage compared with the DC-link voltage. As the wind speed is reduced, the DC-link voltage will be reduced to allow the turbine speed to track the optimum speed for maximum power. At a particular wind speed, the maximum power conditions will be such that the DC-link voltage is equal to the peak output voltage, and cannot be reduced any further. At lower wind speeds the turbine will behave like the system with fundamental switching and a passive rectifier, with only a small change in turbine speed possible.

Increasing the DC-link voltage variability, and hence the speed range of the turbine, means that at the maximum speed of the turbine the voltage will increase and the inverter duty cycle will decrease. This will decrease the switch utilisation, requiring switching devices with a higher rating than for low variability. Switch utilisation is defined as P_O/P_T, where P_T is the product of the switch peak voltage and current ratings and P_O is the rated output power of the converter [30]. The inverter switch utilisation is shown against the DC link voltage variability in Figure 3.16.

Having a larger DC-link voltage variability means that the maximum power point of the turbine can be tracked over a wider wind speed range. However, a larger variability means that the DC-link voltage at the maximum speed of the turbine will be higher, requiring a higher voltage rating on the components, so for reasons of cost the variability must be limited.

The effects of using PWM switching on the inverter were simulated in a similar manner to the fundamental switching case. The difference is that the speed at which the DC-link voltage is equal to the peak output voltage is found by simulation, with the maximum power conditions used above this speed, and the method from Section 3.4.2 used at lower speeds. The number of turns in the generator coils was selected such that the turbine operates at the speed for maximum power capture at this cut-off wind speed.

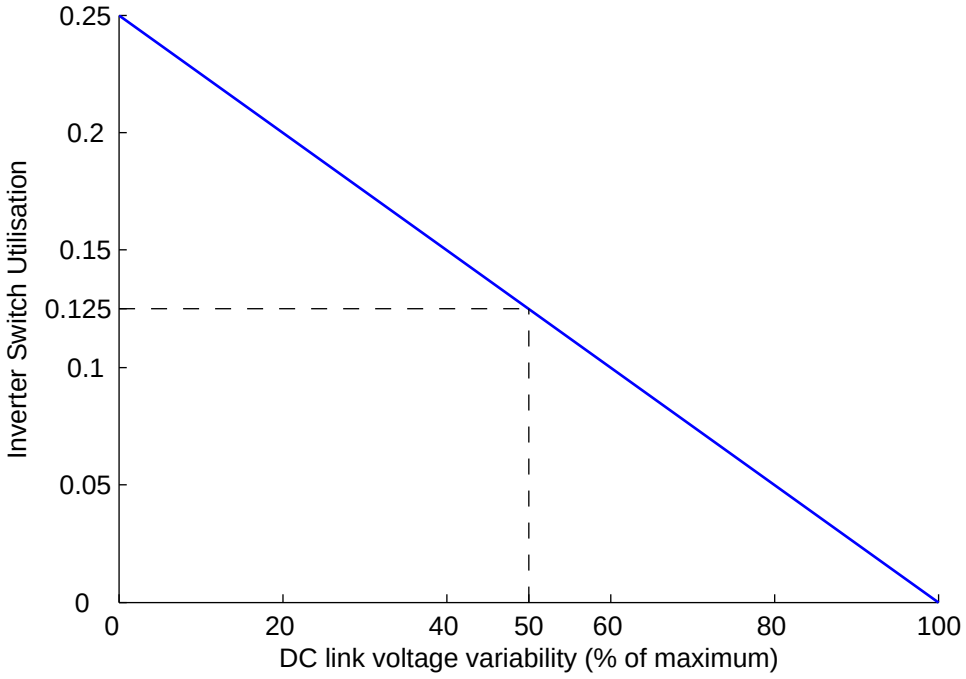


Figure 3.16: Switch utilisation for PWM switching of inverter

Two levels of DC-link voltage variability were simulated – 20% and 40%. In each case the maximum speed was selected as 110% of the rated speed, in order to allow smoothing of the turbine output power above rated wind speed. Simulations show that the DC-link voltage will equal the peak output voltage at 10.8m/s for the 20% variation case and 8.1m/s for the 40% variation case. The power curves from the simulation are shown in Figure 3.17, and the speed variation in Figure 3.18. An improvement in power capture can be seen, especially with the 40% variability case, although power capture is still reduced at low wind speeds.

3.4.4 Fundamental Switching and Boost Rectifier

A boost rectifier allows the generator speed to vary over a wide range while keeping the DC link voltage constant. This is achieved by including a boost converter after the rectifier, and also allows the rectifier to draw sinusoidal current at unity power factor. Efficiency can be reduced compared with the passive rectifier as there are more switching devices in the current path, leading to greater losses. Cost can also be increased due to the extra switching devices and the controller required to implement the power factor correction algorithms.

In the case of the simple operating region detailed in Section 3.2.1, the maximum

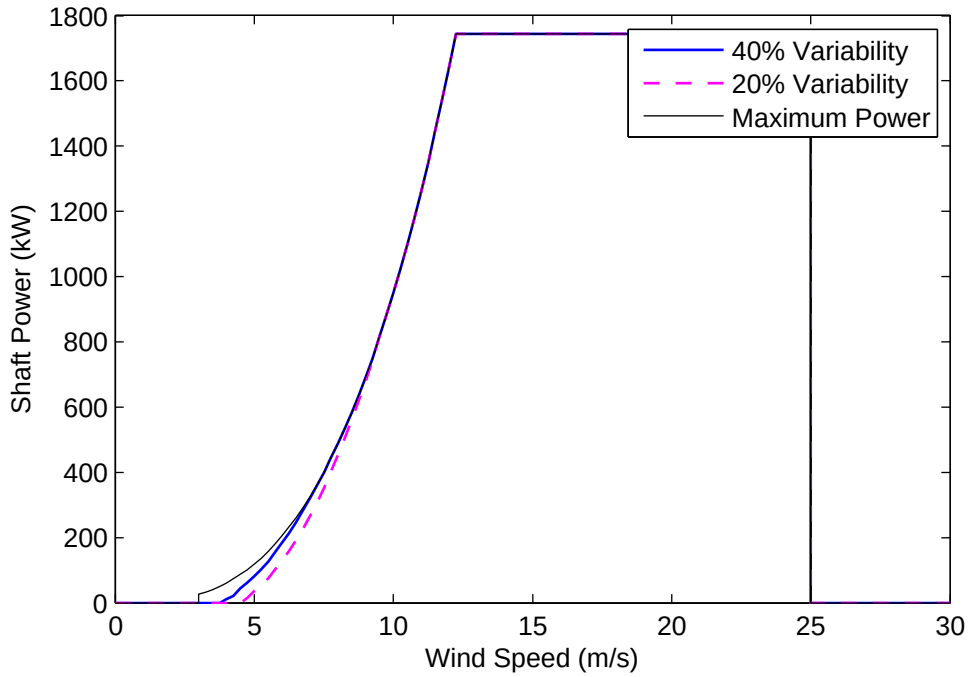


Figure 3.17: Simulated power curves for diode rectifier and PWM output

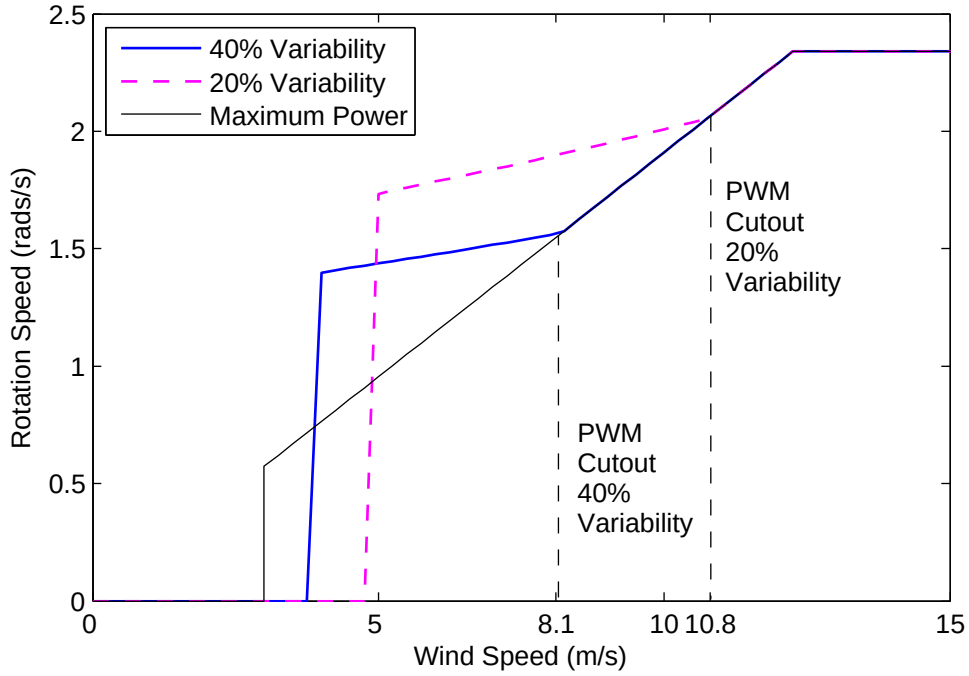


Figure 3.18: Simulated turbine speed for diode rectifier and PWM output

power output is dictated by the wind speed and turbine speed at which the maximum torque is reached, while tracking the turbine maximum power curve, and the turbine starts to operate at constant power. In the case of the 66m diameter turbine used here the peak torque, determined by the generator coil current limit, is reached at 12.25m/s wind, at a rotation speed of 22rpm, giving an output power of 1744kW.

If the torque limited profile described in Section 3.2.3 is used and the turbine speed allowed to increase past 22rpm up to 25rpm with the torque kept constant, an output power of 1.968kW can be achieved at 12.8m/s wind. Power curves can be calculated without needing to simulate the system, and are shown in Figure 3.19 for the simple and the torque-limited operating regions. In both cases a minimum speed of 7rpm was used.

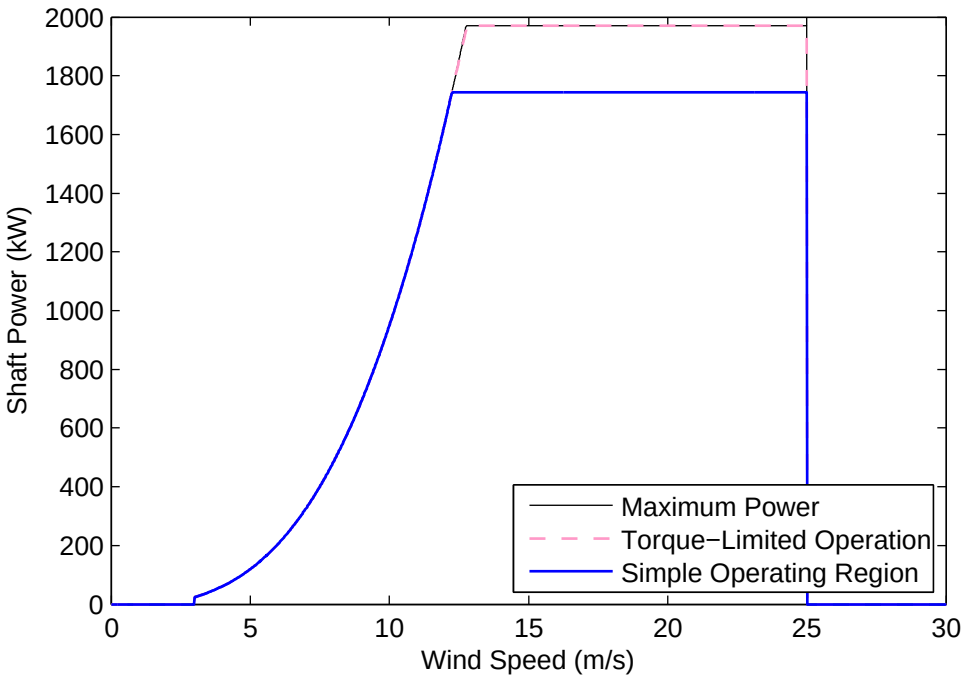


Figure 3.19: Calculated power curves for boost rectifier connection

The torque limited operation is more effective at increasing the power extraction if a larger turbine blade is used with the same generator and coil current, as the rated torque will be achieved at a much lower wind speed and rotation speed, limiting the output power. For instance, with a 70m diameter the peak torque is reached at 11.2m/s wind speed and 19rpm, giving a maximum power output of 1500kW. If the speed is allowed to increase to 25rpm at constant torque then a maximum power of 1.968kW can be achieved at 12.4m/s wind. The larger diameter turbine means that

below the rated wind speed the power capture will be increased for a given wind speed over the smaller diameter turbine.

3.5 Calculation of Annual Energy Extraction

The annual energy extractions for the different operating regions are calculated in the same way as in Section 2.6.2. The energy extraction was calculated for two average wind speeds of 7.5m/s and 9m/s, corresponding to typical onshore and offshore conditions. The annual power extracted is shown in Table 3.3 and Figure 3.20.

System	Annual Power Extraction (MWh) 7.5m/s wind	9m/s wind	Improvement Over Fundamental, Passive System 7.5m/s wind	9m/s wind
Fundamental, passive	4630	6470	0%	0%
PWM – 20% variability	4780	6600	3.2%	2.0%
PWM – 40% variability	4950	6750	6.7%	4.3%
Boost – simple	5070	6840	9.5%	5.7%
Boost – improved	5290	7260	14.3%	12.2%

Table 3.3: Annual power extracted

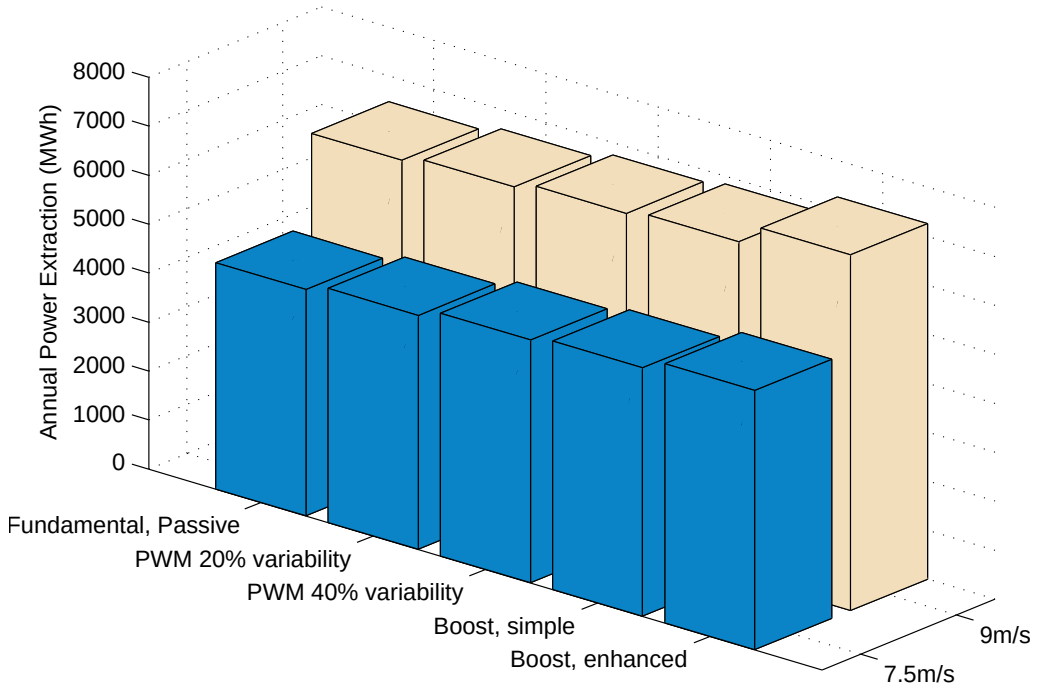


Figure 3.20: Annual power extracted

It is clear that the system with the boost rectifier and the enhanced speed range

offers the greatest power capture of any of the systems, with the boost rectifier with standard speed range in second. This is not surprising as the speed range with the boost rectified systems is the widest. The PWM switched inverter with 40% variability offers power capture close to that of the boost rectified system, with even the 20% variability system providing a significant advantage over the system with passive rectifier and fundamental switching.

Comparing the power extracted from the boost rectifier systems, the increase in power from the enhanced speed range profile is much greater at the higher average wind speed, which is due to the increased power capture at high wind speeds. Comparing the boost rectifier and other systems, the increase in power arises at low wind speeds. These results need to be seen in context with the estimated costs for the power electronic modules, which will be considered in the next chapter.

Chapter 4

Power Electronic Components, Costs and Performance

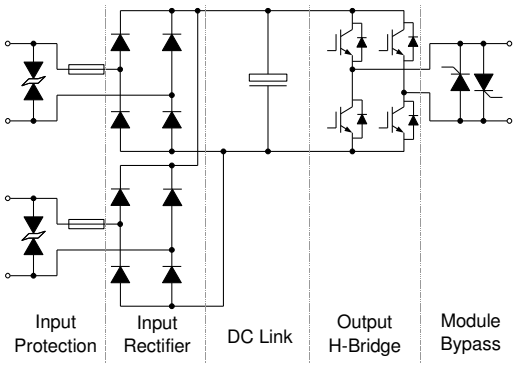
In previous chapters a modular power conversion scheme for a lightweight direct drive generator for wind turbines was introduced. Several architectures and control schemes for the modules were considered in terms of annual power extraction, with a system using a boost rectifier on the input and fundamental switching on the inverter output, with an enhanced speed range, providing the greatest power extraction. This chapter will investigate the design of these modules, including the cost and the estimated power losses. The systems considered in the previous chapter are as follows:

- Passive rectifier input with inverter switched at the fundamental frequency.
- Passive rectifier input with PWM-switched inverter, with 20% and 40% DC-link voltage variability.
- Boost rectifier input with inverter switched at the fundamental frequency, with normal and enhanced speed range.

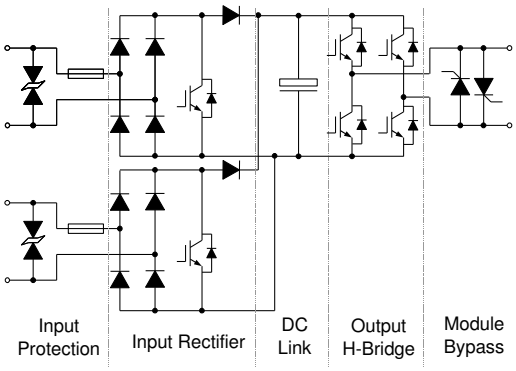
The boost rectifier input system is divided into a system following a simple power-speed profile, as described in Section 3.2.1, and a system following the torque-limited power-speed profile described in Section 3.2.3 with an enhanced speed range. These will be described as the simple and enhanced boost rectifier systems in this chapter. The systems with a PWM-switched inverter, with 20% and 40% DC-link voltage variability will be described as the 20% and 40% PWM systems.

It should be noted that where the inverter is switched at the fundamental frequency, the switching of the different modules is timed such that an accurate sinusoidal output is produced, as described in [27] and [31]. In this case the DC-link voltage of the individual modules is determined by the peak inverter output voltage. If the inverter is switched using PWM, the DC-link voltage is free to vary within certain limits determined by the module and machine design.

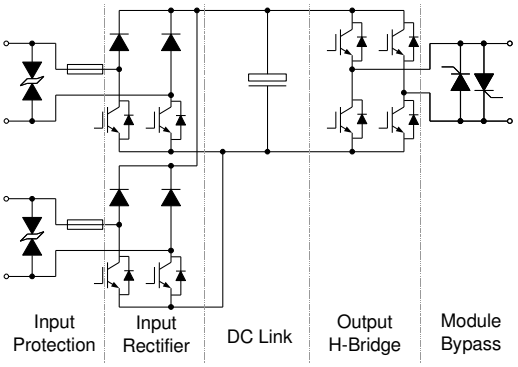
A module schematic using a passive rectifier input is shown in Figure 4.1a below. A boost rectified arrangement is shown in Figure 4.1b, with the rectifiers each consisting of a passive rectifier followed by a boost converter, with the boost converter utilising the coil inductance as the boost inductance. This design will have a reduced electrical efficiency compared with the passive rectifier as the current will have to pass through three devices in the circuit compared with two in the passive rectifier case, along with the switching losses of the active switch device. An improved circuit integrates the passive rectifier and boost converter, and is shown in Figure 4.1c.



(a) Module with passive rectifier input.



(b) Module with boost rectifier input.



(c) Module with improved boost rectifier.

Figure 4.1: Module schematic designs.

In all cases insulated gate bipolar transistors (IGBTs) will be used for the main switching devices as they offer the best switching speeds and easiest gate driving, with good efficiency at this power level. A high switching frequency on the rectifier side of the module is important due to the low inductance of the generator coils.

4.1 Fault Tolerance Considerations

One of the motivations behind using a modular power conversion scheme is that of fault tolerance, meaning that the system must continue to operate, with reduced output power, in the event of several modules failing. With 13 modules per inverter string, each string should be capable of operating with the loss of two modules, which would require an increase in the voltage of each module of 18%.

Fault tolerance depends on the ability of a faulted module to still conduct current on the inverter side, so that the string of modules is not broken. On the machine side, while the increase in torque from one shorted coil is small compared with the total, it would be desirable to disconnect the coils in the event of a module short circuit fault. Both of these issues depend on the failure modes of the IGBT modules used. If a failure occurs in the control system it is likely that the module will fail with all the switching devices off, although this is not guaranteed.

4.1.1 IGBT Failure Modes

The main failure mode for direct bonded copper (DBC) IGBT modules of the type likely to be used is the lifting of the bond wires from the top contacts of the devices in the module. This is believed to be due to thermal cycling and different coefficients of thermal expansion of the wires compared with the other parts of the module [32]. This can result in the formation of an arc, which can destroy the inside of the module, with failure often being in the form of a short circuit caused by the evaporation of the silicone encapsulant inside the module and the deposition of conductive material. However a short-circuit fault cannot be relied upon.

Another method of IGBT encapsulation is the Press-Pack, as used in traditional thyristor applications. The Press-Pack is designed for the application of high voltage switches in power transmission applications such as HVDC, where it is desirable for the device to fail in short circuit so as not to affect the entire stack of devices [32].

This is achieved by sandwiching the device between two pressure plates, so that if one of the devices in the module breaks down the pressure contact closes the circuit. In the event of a load short circuit the pressure connection is able to withstand high current.

4.1.2 Grid Side – Module Bypassing Methods

As the modules are distributed around the generator, Press-Pack devices would be difficult to use, so another method must be used to bypass the module in the event of a fault. The proposed bypass method is to use back-to-back thyristors – a mechanical switch could be used but would be less reliable. A method must be used to trigger the thyristors which is independent of the rest of the module, as the module having power and the control functions working cannot be relied on. A circuit should be used where the thyristors will trigger unless supplied with a voltage from the controller. If, for some reason, the gate drive circuit fails, the thyristor will still switch on once the forward blocking voltage of the device is exceeded, and this could be used as a failsafe triggering method.

4.1.3 Machine Side – Input Protection

To protect the machine from module faults, fuses will be used between the generator coils and power modules. Fuses could also protect the modules from insulation faults in the coils if the voltage rating is high enough. In the event of a module failure the coils would still be subjected to a high short circuit current until the fuse blows, but it is believed that the generator would be able to handle the mechanical stress as it would be low compared with the total machine torque. A transient voltage suppressor would be attached across the coils to absorb the energy stored in the coil inductance when the fuse blows.

4.2 System Modelling

At this stage all simulation was carried out based on a constant DC-link voltage – the effects of the DC-link capacitance were not considered, meaning that dynamic interactions between the inverter and rectifier were not considered. With the fundamentally switched inverter output the DC-link voltage is determined by the

required inverter voltage, while in the PWM case the inverter voltage determines the minimum DC-link voltage.

In a star-connected system with 11kV output and a string of 13 modules, Equation 3.2 dictates that the peak output voltage will be 726V at the rated real and reactive power, thus dictating the DC-link voltage. If two modules are lost this rises to 858V. The boost rectifier system with increased speed range will have a higher power output and hence the module voltages will be 730V with 13 modules and 863V with 11.

The systems with PWM output had the generator EMF selected in the last chapter in order to give the required speed variability, while allowing 10% overspeed to smooth the power flow above the rated wind speed. Simulation was used to determine the DC-link voltage necessary to draw the module rated power at the rated turbine speed.

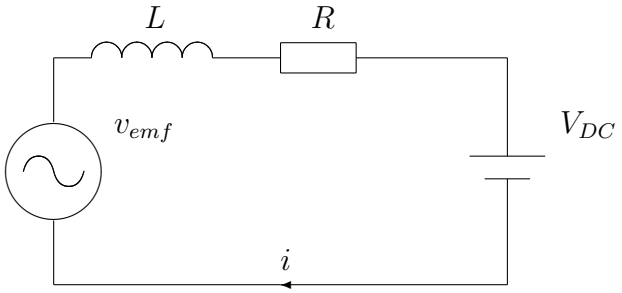
4.2.1 Simulation of the Rectifier

The rectifier with constant DC-link voltage was simulated using Simulink, without the use of any circuit simulation blocksets. This was done in order to increase the speed of the simulation as the level of detail provided by the SimPowerSystems blockset was not required. This is also the rectifier model that was used in the previous chapter.

The generator coil was modelled as in Section 2.1 as a sinusoidal voltage source in series with an inductor and resistor, representing the coil EMF, inductance and resistance. The DC-link was modelled as a constant voltage source. The passive rectifier was considered to be capable of existing in three states, depending on which diodes were switched on and which were off. These states are shown in Figure 4.2.

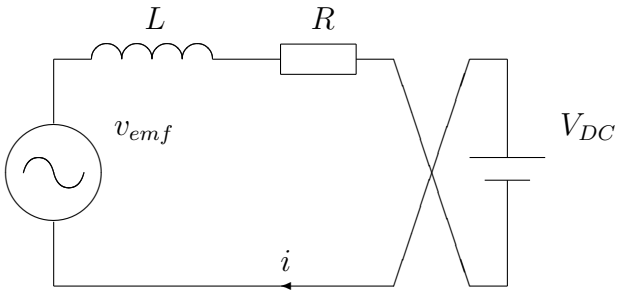
Based on these states the equation governing the rate of change of the coil current can be determined, which is integrated numerically in Simulink to determine the current. Transition between the states is given by the following rules:

- If the rectifier is conducting, in states a) or b), then it will remain in that state until the current drops to zero, whereupon it will switch to state c).
- If the rectifier is not conducting, in state c), then it will start conducting when the magnitude of the input terminal voltage exceeds the DC-link voltage. The



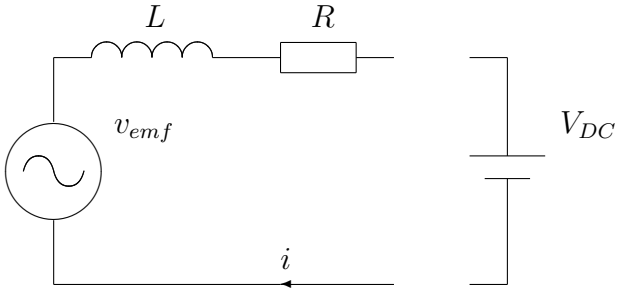
$$\frac{di}{dt} = \frac{1}{L}(v_{emf} - iR - V_{DC})$$

(a) Rectifier conducting in the forward direction.



$$\frac{di}{dt} = \frac{1}{L}(v_{emf} - iR + V_{DC})$$

(b) Rectifier conducting in the reverse direction.



$$\frac{di}{dt} = 0$$

$$i = 0$$

(c) Rectifier not conducting.

Figure 4.2: Rectifier conduction states.

direction of conduction is determined by the sign of the input terminal voltage. This state is only likely to occur around the zero-crossings of the coil current and the voltage applied to the coil.

In the boost rectifier system, the switching is represented by switching the rectifier dc side voltage between zero volts and the value of the DC-link voltage.

4.2.2 Control of the Boost Rectifier

At this stage the simulation of the boost rectifier is carried out with the position of the generator EMF known by the rectifier controller. An actual implementation of the controller would require a system to estimate the position of the EMF.

Hysteresis current control

The first method considered to control the coil current was to use a hysteresis controller, working in the analogue domain. This will force the current to accurately follow an analogue reference current, with the boost rectifier switching in order to keep the current within chosen tolerance bands of the reference current. In this case the analogue reference current is the coil EMF divided by an equivalent resistance and the equivalent resistance is varied to control the power extracted from the coil.

Two limitations were found with this approach: firstly there is a need for a fast analogue circuit and digital analogue converter to convert the digital current to analogue; these are expensive. Secondly the switching frequency will vary, and there is no way to interleave the switching of the two boost rectifiers for the two coils – this, if achieved, would reduce the current ripple and hence the DC link capacitor size requirement, although this is of less importance than the first limitation.

Open loop current control

The PWM capability of a digital signal processor (DSP) or microcontroller was judged to be the best way to produce the PWM output to drive the boost rectifiers, offering the most flexibility and minimum number of components. The rectifier is controlled by varying the duty cycle, d, of the PWM output, which will vary the time averaged voltage seen by the coil as shown in Equation 4.1

$$v_{app} = (1 - d)V_{DC}sign(i) \qquad \text{where } 0 \leq d \leq 1 \tag{4.1}$$

d, where $0 \leq d \leq 1$, is the duty cycle of the PWM waveform and v_{app} is the time averaged voltage applied to the coil. The $sign(i)$ term represents the effect of the front-end diode rectifier. An equivalent circuit is shown in Figure 4.3, where v_{emf} is the coil EMF and L and R are the coil inductance and resistance. For this analysis it will be assumed that v_{app} can take any value, limited by the DC-link voltage, and the problems of this assumption will be covered later.

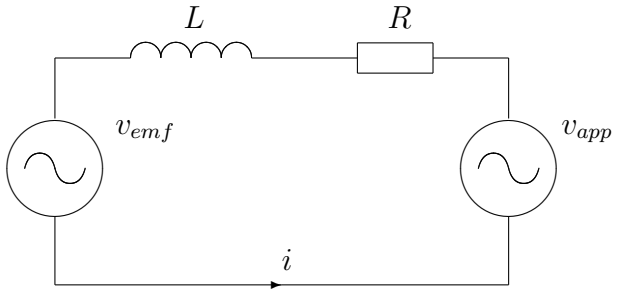


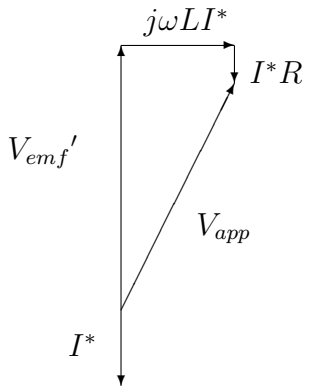
Figure 4.3: Boost rectifier equivalent circuit

If the coil EMF, current and applied voltage are all sinusoidal then they can be represented in a phasor diagram, shown in Figure 4.4. For unity power factor with respect to the coil EMF, the current has to be exactly out of phase with the EMF, with the magnitude of the current determined by the amount of power required from the coil.

If the magnitude and position of $\vec{V}_{emf}$ is known, i.e. $\vec{V}_{emf}{}' = \vec{V}_{emf}$, then the magnitude and phase of $\vec{V}_{app}$ necessary to achieve the desired current I^* can be calculated and used to set the PWM duty cycle, assuming the coil resistance and inductance are known. This can be implemented in a DSP or microcontroller without the need for analogue circuits. The switching of the two rectifiers can also be interleaved, which has the effect of cancelling the DC-side current ripple at the switching frequency, leaving only the sidebands of the modulation frequency, and higher harmonics.

4.2.3 Boost rectifier switching frequency

If, during the boost rectifier switching cycle, the coil current drops to zero at any point, the boost converter will be in the discontinuous conduction mode. Here



$$\vec{V}_{app} = \vec{V}_{emf}{}' + j\omega L\vec{I}^* + \vec{I}^*R$$

if $\vec{V}_{emf}{}' = \vec{V}_{emf}$

then $\vec{I} = \vec{I}^*$

Figure 4.4: Boost rectifier equivalent phasor diagram

the average voltage is no longer simply controlled by the duty cycle as shown in Equation 4.1 but will also depend on the level of discontinuity. This makes controlling the average voltage difficult, so it is desirable to avoid the discontinuous conduction mode as much as possible. The minimum current at which discontinuous conduction starts to occur is given by Equation 4.2, where f_s is the switching frequency [33].

$$I = \frac{V_{DC}}{2f_sL}d(1-d) \tag{4.2}$$

For the 1.8MW system previously discussed, a switching frequency of 4kHz was found to be necessary to prevent discontinuous conduction over the operating range of the turbine. A system could be used in which a higher frequency is used at low power levels to prevent discontinuous conduction, with a lower frequency used at high power levels to reduce switching losses, but this will not be considered here.

4.3 Component Selection

Component voltage ratings are dependent on the variation of the DC-link voltage, with the nominal DC voltages for the systems with fundamentally switched inverters having been found in Section 4.2. The voltage for normal operation is the required output voltage with all 13 modules functioning while the maximum voltage is the output voltage with 2 faulted modules.

The nominal, maximum and peak voltages for the different module systems are given in Table 4.1. For the systems with PWM inverter output the DC-link voltage necessary to draw rated power at rated generator speed was found through sim-

ulation, which gives the average voltage under normal operation. The maximum voltage is the DC-link voltage necessary to draw rated power at the 10% overspeed condition. For all systems an additional 10% was added to the maximum voltage to account for the voltage ripple at the second harmonic of the grid voltage due to passing a single phase current from the H-bridge output of each module, which gives the peak DC-link voltage.

		Average DC Voltage		Peak DC
Inverter	Rectifier	Normal	Maximum	Voltage
Fundamental	Passive	726V	858V	944V
PWM – 20%	Passive	767V	857V	943V
PWM – 40%	Passive	965V	1075V	1183V
Fundamental	Boost – simple	726V	858V	944V
Fundamental	Boost – enhanced	730V	863V	949V

Table 4.1: Inverter DC-link voltage

In selecting switching devices, isolated base modules were selected in preference to discrete devices. This was done in order to simplify the construction of the power electronic module as device to heatsink insulation would not need to be considered.

4.3.1 Output H-Bridge

Ignoring all electrical losses, the real output power will be 1968kW for the boost rectifier system with increased speed variability and 1744kW for the other systems, which gives powers of 2224kVA and 1971kVA apparent power with the maximum reactive power. This gives module powers of 28.5kVA and 25.3kVA respectively, and inverter rms currents of 58.36A and 51.73A. These voltage and current ratings are shown in Table 4.2.

Inverter	Rectifier	Peak V	RMS I
Fundamental	Passive	944V	51.73A
PWM – 20%	Passive	944V	51.73A
PWM – 40%	Passive	1183V	51.73A
Fundamental	Boost – simple	944V	51.73A
Fundamental	Boost – enhanced	949V	58.36A

Table 4.2: Inverter current and voltage ratings.

The peak voltage of the system with passive rectifier and PWM with 40% DC-link voltage variation is above 1200V, meaning that 1700V IGBTs must be used. A

suitable 1700V transistor module is the Semikron SKM 100GB176D, which is a half bridge module as before, meaning that two will be required for a full H-bridge.

For the other systems, the voltage requirements mean that 1200V IGBTs can be used. The current requirements are similar enough that the same IGBTs can be used in all cases, and a suitable transistor module is the Semikron SKM 75GB123D, which is a half bridge module as before.

4.3.2 Input Rectifier

With the boost rectifier inputs the coil EMF is independent of the DC link voltage, but the peak EMF must always be less than the DC link voltage if the rectifier is to control the current. The peak EMF will occur when the turbine is operating at the maximum speed, which is 10% higher than the rated speed. At this point rated power will be being produced, and the minimum DC link voltage will occur when the rated reactive power is being absorbed, which will be 681V for the simple case and 680V for the enhanced power capture case. Allowing a margin of 10% for voltage ripple the peak EMF cannot exceed 612V, or 433V RMS during overspeed, which will require an RMS EMF of 394V at rated speed. From this the rated current can be calculated, and these parameters are shown in Table 4.3 below.

A suitable IGBT module is the Semikron SK60 GAL123, which is a boost cell featuring a low-side IGBT and high-side diode, so two would be required for each rectifier.

Rectifier	Peak DC V	Rated Speed	Coil RMS V	Coil RMS I
Boost – simple	944V	22rpm	394V	28.4A
Boost – improved	949V	25rpm	394V	32.0A

Table 4.3: Boost rectifier current and voltage ratings.

The required EMFs at rated power for the systems with passive rectifiers were calculated by simulation in the previous chapter. Using the same simulation the RMS coil currents can be calculated, and these are shown in Table 4.4. Based on this information the Semikron SK50B12 bridge rectifier would be suitable for the fundamental and 20% PWM cases with the SK50B16 suitable for the 40% PWM case.

Inverter	Peak DC V	Coil RMS V	Coil RMS I	Coil Peak I
Fundamental	944V	623V	22.6A	43.5A
PWM – 20%	944V	685V	20.9A	40.7A
PWM – 40%	1183V	839V	17.1A	34.1A

Table 4.4: Passive rectifier current and voltage ratings.

4.3.3 DC-Link Capacitors

The selection of the DC link capacitance depends mostly on the desired lifetime of the capacitors, which depends on the operating temperature of the capacitors. The operating temperature depends on the AC ripple current and the equivalent series resistance (ESR) or the capacitor, while the ESR depends on the frequency and the temperature. The ESR will be lower at higher frequencies and temperatures.

In both the active and passive rectifier systems, the DC current from the rectifier was found by simulation, based on the DC-link voltage being constant. For the inverter side, the DC current was found by multiplying the AC current by a waveform representing the switching of the inverter. For the fundamental switching inverter a module was chosen with more or less symmetrical switching, so the current harmonics are similar to that of a square wave output.

For the PWM switching inverters, a peak duty cycle was found by dividing the required module output voltage by the nominal DC-link voltage, and this was multiplied by a sinusoidal waveform. The resulting waveform was then compared with a triangular carrier waveform to obtain the PWM output. A carrier frequency of 400Hz was used, when this is combined with the outputs of the other modules a switching frequency of 5200Hz will result. The 400Hz carrier was synchronised with the 50Hz mains frequency.

The currents from the inverter and rectifier side were added, with the DC current cancelling, and the current spectra found. These are shown in Figure 4.5 for the rated power scenario. For the systems with boost rectifier, sidebands of the PWM modulation frequency can be seen, with the current at the PWM modulation frequency itself being cancelled by the interleaving of the two rectifier switching cycles. There is a large current at the second harmonic of the grid frequency, as well as higher harmonics.

For the systems with PWM switched inverter, there is a significant harmonic at the inverter frequency of 400Hz as well as the second harmonic of the grid frequency.

There is also a significant current at the fourth harmonic of the generator frequency, at 160Hz, where the generator is operating at the rated speed, with a frequency of 40Hz. The systems with PWM switching show a lower grid second harmonic current, due to the higher DC-link voltage, with the system with 40% speed variation showing the lowest second harmonic current. However the system with 40% variation shows the largest current at 400Hz.

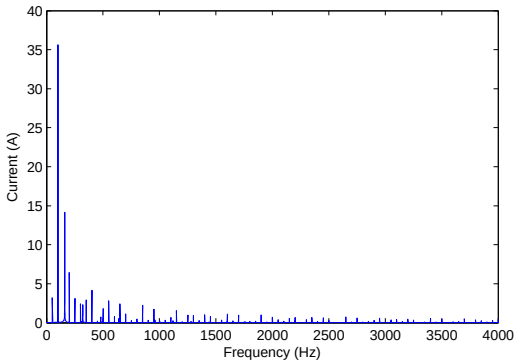
The capacitor lifetime was calculated according to the instructions in [34]. For each power module system and proposed capacitor bank each RMS harmonic current was divided by the number of parallel capacitors then squared and multiplied by the ESR at that frequency, and the results added to find the total loss. Using the thermal resistance of the capacitor core to the surrounding air, the core temperature was found. Using the revised core temperature the ESR for each frequency was re-calculated and the above process repeated several times to find the core temperature. From the core temperature the capacitor lifetime was found from information provided by the manufacturer. An ambient air temperature of 50°C was used.

A number of capacitor banks were considered, using the BHC Aerovox ALC10C 102EL400 capacitor, which has a capacitance of 1000μF and a voltage rating of 400V. A lifetime of 175,200 Hours at the rated turbine power was required, this being equivalent to 20 years at rated power. The resulting banks are listed in Table 4.5. All the power module systems require 15 capacitors, apart from the PWM inverter module with 40% DC-link voltage variability which requires 16.

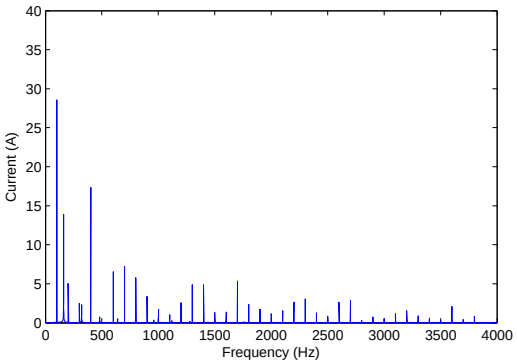
System configuration	Bank size		Total DC-link Capacitance (μF)	Temperature Rise (°C)	Lifetime (k hours)
	Parallel	Series			
Passive, fund.	4	3	1333	8.33	156
	5	3	1667	5.79	216
PWM – 20%	4	3	1333	7.49	168
	5	3	1667	4.91	240
PWM – 40%	4	4	1000	6.59	192
Boost, simple	4	3	1333	8.29	156
	5	3	1667	5.40	228
Boost, enhanced	5	3	1667	6.79	186

Table 4.5: Capacitor bank lifetimes

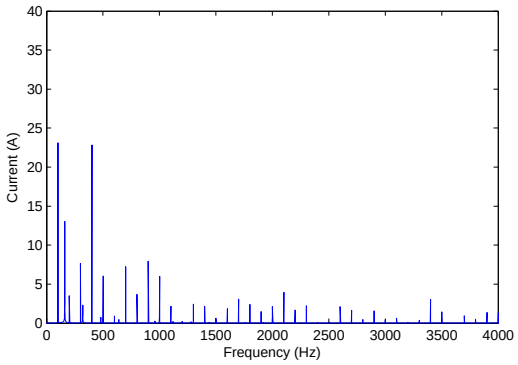
Work carried out with other researchers in Durham University has suggested that in a system with a fundamentally switched inverter, a DC-link capacitance that is too low will result in a large third harmonic distortion in the inverter voltage



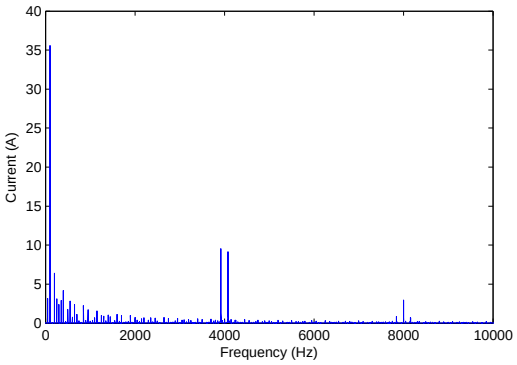
(a) Passive rectifier and fundamental output.



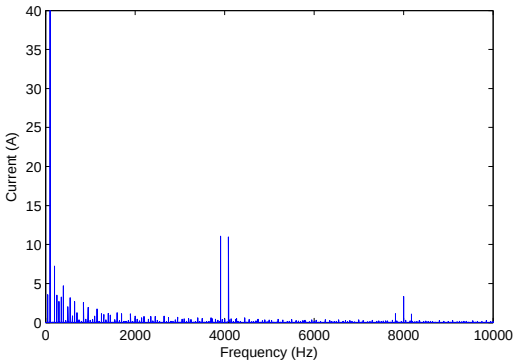
(b) Passive rectifier and PWM output – 20% variability.



(c) Passive rectifier and PWM output – 40% variability.



(d) Boost rectifier and fundamental output.



(e) Boost rectifier and fundamental output – enhanced profile.

Figure 4.5: DC Link capacitor current spectra.

waveform [35]. This distortion is due to the interaction of the second harmonic DC-link voltage ripple and the inverter switching. The level of distortion can be greatly reduced by increasing the DC-link capacitance, with 4000μF providing a much lower distortion than 2000μF, and any increase above this providing only a small effect.

This problem will not affect the systems with PWM output as the modulation depth can be varied to compensate for the DC-link voltage ripple. This ripple is clearly a problem for the fundamentally switched inverter as increasing the capacitance would be costly, so some other method must be found to compensate.

4.4 Estimates of Module Cost

The costs for the components used is given in Table 4.6, based on the number of components to build one module, and taken from the catalogues of the major component suppliers. The total costs for the different power module systems are given in Table 4.7, along with an estimate of the controller cost. The controller cost for the systems with boost rectifier is slightly greater than the passive rectifier controller due to the extra computation power requirement and the more complicated gate drive circuits. A breakdown of the cost of each module system by part is shown in Figure 4.6.

Rectifier	Semikron SK60GAL123 Boost cell	£16.99
	Semikron SK50B12 Bridge rectifier	£21.53
	Semikron SK50B16 Bridge rectifier	£18.54
DC-Link	BHC ALC10C102EL400 Capacitor	£13.20
Inverter	Semikron SKM75GB123D half bridge	£54.02
	Semikron SKM100GB176D half bridge	£122.69

Table 4.6: Component costs

	Power Components	Controller	Total
Passive, fundamental	£349.10	£100	£449.10
PWM – 20%	£349.10	£100	£449.10
PWM – 40%	£493.69	£100	£593.69
Boost, simple	£374.00	£120	£494.10
Boost, enhanced	£374.00	£120	£494.10

Table 4.7: Module total cost

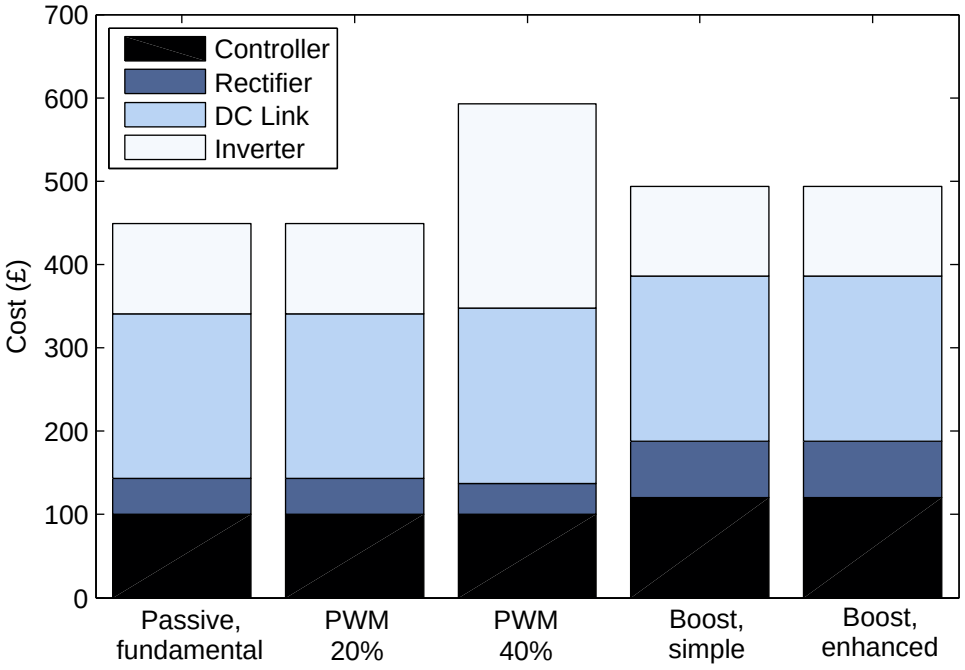


Figure 4.6: Module cost breakdown

It is clear that the DC-link capacitors make up a significant proportion of the cost in all the systems considered, although all the modules have a broadly similar capacitor cost. The system with PWM output and 40% variability has the highest cost, due to the need to use 1700V IGBTs, which are much more expensive than the 1200V equivalent. Of the other systems, the boost rectifier systems both have the same components as the ratings are similar. The passive rectifier systems are slightly cheaper due to the simpler rectifier and controller, with the addition of a small level of PWM speed variability leading to no increase in cost over the fundamental output.

4.5 Estimates of Losses

Of all the losses, the DC-link capacitor loss has already been calculated in Section 4.3.3 for the purpose of temperature rise estimation, while the generator coil loss can be calculated by multiplying the RMS coil current squared by the coil resistance. The RMS coil current has been found by simulation, while the coil resistance depends on the number of turns in the coil, which is chosen to give the desired EMF. The EMF has been previously selected for the different module designs, and is based on multiplying the EMF of the reference design from Table 3.1 by a factor

k, signifying the increase in the number of turns in each coil.

This change will increase the inductance by k and increase the resistance by k^2, as the length of wire is being increased by k while the cross sectional area is being decreased by $\frac{1}{k}$. The coil resistances and RMS currents are shown in Table 4.8 along with the loss for one coil. The losses in the boost rectifier systems due to the high frequency current ripple are not considered in this analysis.

	Resistance (Ohms)	Current (A RMS)	Loss (W)
Passive, fundamental	0.914	22.6	467
PWM – 20%	1.101	20.9	481
PWM – 40%	1.663	17.1	486
Boost, simple	0.345	28.4	295
Boost, enhanced	0.304	32.0	295

Table 4.8: Coil current, resistance and loss

The voltage drop for the IGBTs and diodes in the system is represented by a non-linear relationship with current. However this can be approximated by a fixed voltage drop and a resistance in series. This can be used along with the rectifier current waveforms to calculate the power loss in the passive rectifiers. The inverter conduction loss can be calculated in the same way.

The boost rectifier systems are more complicated, with the losses depending on the state of the boost transistors. If the boost transistor is on then the current path will feature a diode and transistor in series, while if it is off the current path will feature two diodes in series. The current waveforms in each state were found and the losses calculated from these.

Switching loss in IGBTs are given as an energy loss per switching event, which is proportional to the current being switched, at a given DC-link voltage. As the proportionality is almost linear the average current can be used to find the average switching loss. This is then multiplied by the switching frequency and the number of devices switching to find the switching power loss. These losses are shown in Table 4.9 for the different module configurations.

A breakdown of all the electrical losses by component is shown in Figure 4.7, while total loss and efficiency for the power electronics and the complete electrical system are listed in Table 4.10. It can be seen that the boost rectifiers have a significantly higher loss than the passive rectifiers, with the other losses being similar.

	Loss (W)				
	Both rectifiers		DC	Inverter	
	Conduction	Switching	Link	Conduction	Switching
Passive, fundamental	75.6	–	20.7	223.8	1.4
PWM – 20%	67.2	–	17.6	223.8	5.7
PWM – 40%	50.6	–	25.2	149.1	19.2
Boost, simple	176.0	72.8	19.3	223.8	1.4
Boost, enhanced	207.6	82.0	24.3	264.7	1.6

Table 4.9: Power electronics losses

The boost rectifier losses are balanced by the reduced coil losses, from drawing a sinusoidal current.

The PWM inverter system with 40% variation shows the lowest inverter conduction loss. This is due to the use of trench IGBTs, which feature a lower forward voltage drop than the standard IGBTs used in the other systems, although they posses a higher switching loss. As the switching frequency is very low in the inverter in all the systems under consideration, the use of trench IGBTs would be desirable in the other systems, however they are not available in the desired current rating. The devices selected for the 40% PWM system are of a higher current rating than is necessary for the application, as devices with a lower current rating are unavailable at the required voltage rating, and as such have a significantly higher cost.

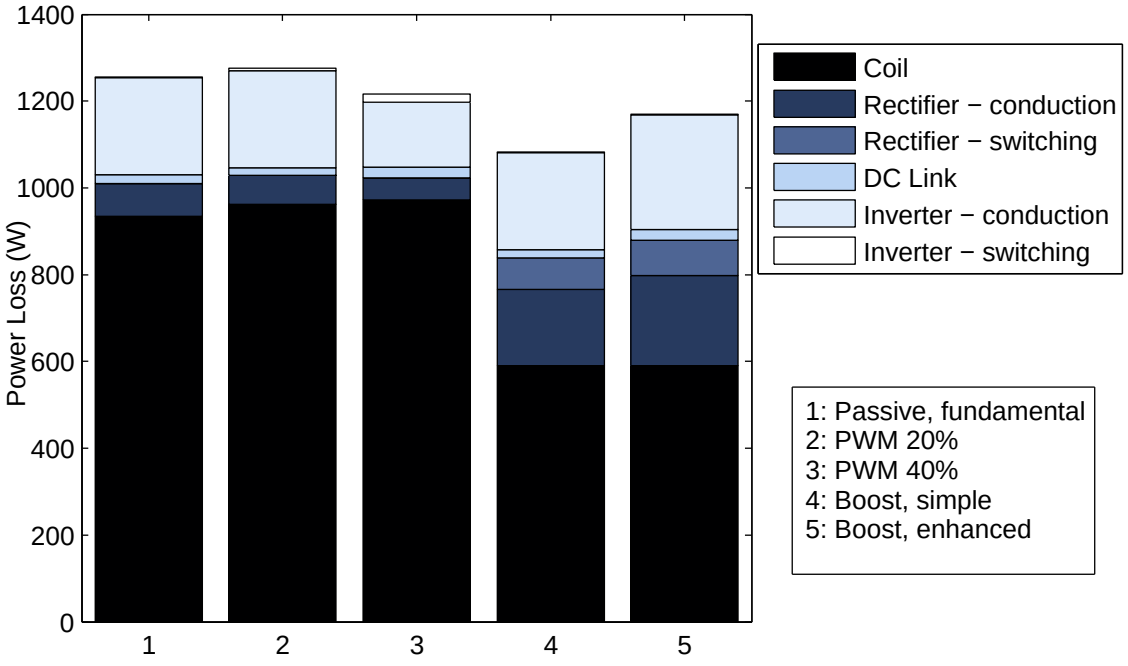


Figure 4.7: Module losses

	Electrical Loss (W)		Efficiency	
	Power Electronics	Total	Power Electronics	Total
Passive, fundamental	321.5	1256	98.6%	94.4%
PWM – 20%	314.3	1276	98.6%	94.3%
PWM – 40%	244.1	1216	98.9%	94.6%
Boost, simple	493.3	1083	97.8%	95.2%
Boost, enhanced	580.2	1170	97.7%	95.4%

Table 4.10: Total electrical losses and efficiency

4.6 Module Design Choice

The systems with the boost rectifier input have a higher power electronic loss, due to the extra complexity of the active rectifier, but lower coil power loss due to the sinusoidal current, which will allow a greater power to be extracted from a given generator. The passive rectifier systems have a much greater coil loss due to the high crest factor of the coil current, which is due to the low inductance of the coils, and cannot easily be compensated. The boost rectifier systems have a much greater power loss in the rectifier, but it would be considerably easier to improve the cooling of the power electronic modules than the generator coils, where cooling is affected by the geometry of the machine.

Another potential problem with the passive rectifier systems is that the DC-link voltage ripple, caused by the pulsating power drawn by the inverter, could modulate the power drawn from the coils. To test this the model developed in Section 4.2.1 was modified to include the DC-link capacitance and the current drawn from the inverter. The current from one coil in the PWM system with 20% variability is shown in Figure 4.8. There is a significant effect from the DC-link voltage ripple on the coil current, and hence the generator torque ripple.

Because of these problems with the passive rectifier systems, a boost rectifier system will be used despite the added complexity and increased rectifier losses. The boost rectifier systems also offer increased power capture due to their greater speed range.

The boost rectifier system with enhanced speed range was found to require the same components as the standard boost rectifier system, due to the component ratings being similar. For the sake of simplicity, the standard power-limited power-

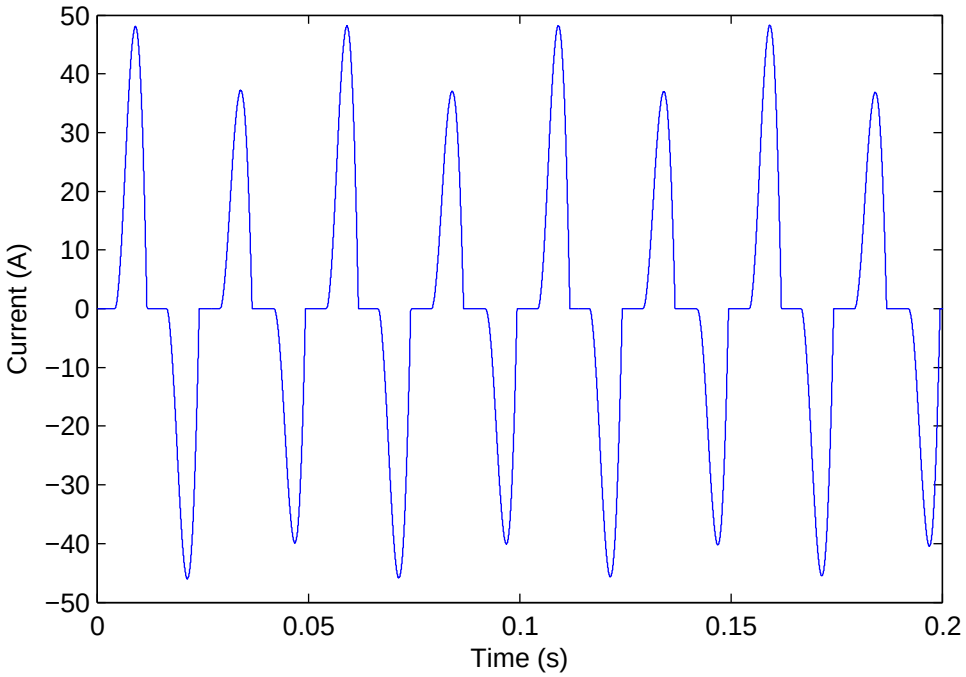


Figure 4.8: Coil current in a passive rectifier system, showing the effects of the DC voltage ripple.

speed characteristic, described in Section 3.2.1, will be used in developing the prototype system, although the enhanced speed range characteristic could be implemented later using the same hardware.

The switching losses in the PWM-switched inverters were found to be low compared with the other losses, meaning that PWM switching of the inverter in the boost rectifier systems could be considered. This would have several advantages:

- The effects of the DC-link voltage ripple on the output voltage waveform could be reduced or eliminated, which would remove the need to increase the DC-link capacitance to reduce the voltage ripple, reducing the cost.
- The DC-link capacitors would be operating closer to their rated voltages, meaning that the capacitor current would be lower, increasing the capacitor lifetime.
- The DC-link voltage would be allowed to fluctuate more, decreasing the demands placed on the DC-link voltage control algorithm.

Chapter 5

Analysis of Generator High Voltage Issues

Chapter 1 introduced the concept of a modular direct drive generator for wind turbine applications, and the need for a modular power conversion scheme, which leads to greater reliability and a higher output voltage. Chapters 3 and 4 have concentrated on the operating regions of the turbine and generator, and the power electronic topology to be used in the modules. This chapter will analyse some of the problems with using high voltages in the generator and power electronics. The problems are:

- Power electronic modules would need to be mounted on the generator in order to avoid excessive lead lengths.
- The modules will therefore be exposed to high electrical stress.
- The modules will also be exposed to extreme environmental conditions.
- Lightning could raise the module potential far above the nominal level, neccessetating some form of protection.

This chapter will begin by reviewing the machine geometry for the proposed 1.8MW generator design. The insulation requirements for the coils will be considered for normal operation, followed by the power module insulation. Finally, lightning strike protection will be considered.

5.1 Machine Geometry

The 1.8MW machine design under consideration was introduced in chapter 3, and will be considered in greater detail in this chapter. The machine has an airgap diameter of 6.88m and an axial length of around 1m. The stator is inside the rotor, and both the rotor and stator feature a lightweight iron core consisting of iron wire, to carry the magnetic flux, embedded in resin for strength. This is used instead of a traditional laminated iron core, which would be difficult to manufacture.

The remainder of the rotor and stator is a composite structure, of glass fibre reinforced resin. 162 coils are mounted in the air gap, and are wound on nylon bobbins before being individually encapsulated in an appropriate resin to provide the necessary insulation. The coils each measure 130mm wide by 1m long and are approximately 15mm thick.

The 162 coils are connected to 81 power electronic modules, mounted on the inside of the stator rim, spaced evenly around the generator. This allows approximately 20m x 1m for the modules, or 250mm x 1m for each module.

The rotor and stator are connected to the hub via alloy or composite spokes, with around 16 spokes on each side of the rotor and stator. The issue of lightning protection requires the spokes to contain conductive material and be at ground potential. The generator could be open or contained within a nacelle. A diagram of the generator, with a reduced number of coils and magnets, and with power electronic modules mounted on the stator, is shown in Figure 5.1.

5.2 Normal Conditions

5.2.1 Insulation Requirements

The generator coils must be completely isolated from each other and from the metal parts of the generator, such as the stator back iron and spokes. The power electronic modules can either be completely isolated from their environment, in which case a way must be found to isolated the switching devices from the heatsink such that heat can still be transferred. Alternatively the modules must operate at live potential. The latter option would introduce problems of surface tracking and corona discharge. The insulation would be required to withstand a voltage of $2U_n + 1\text{kV}$,

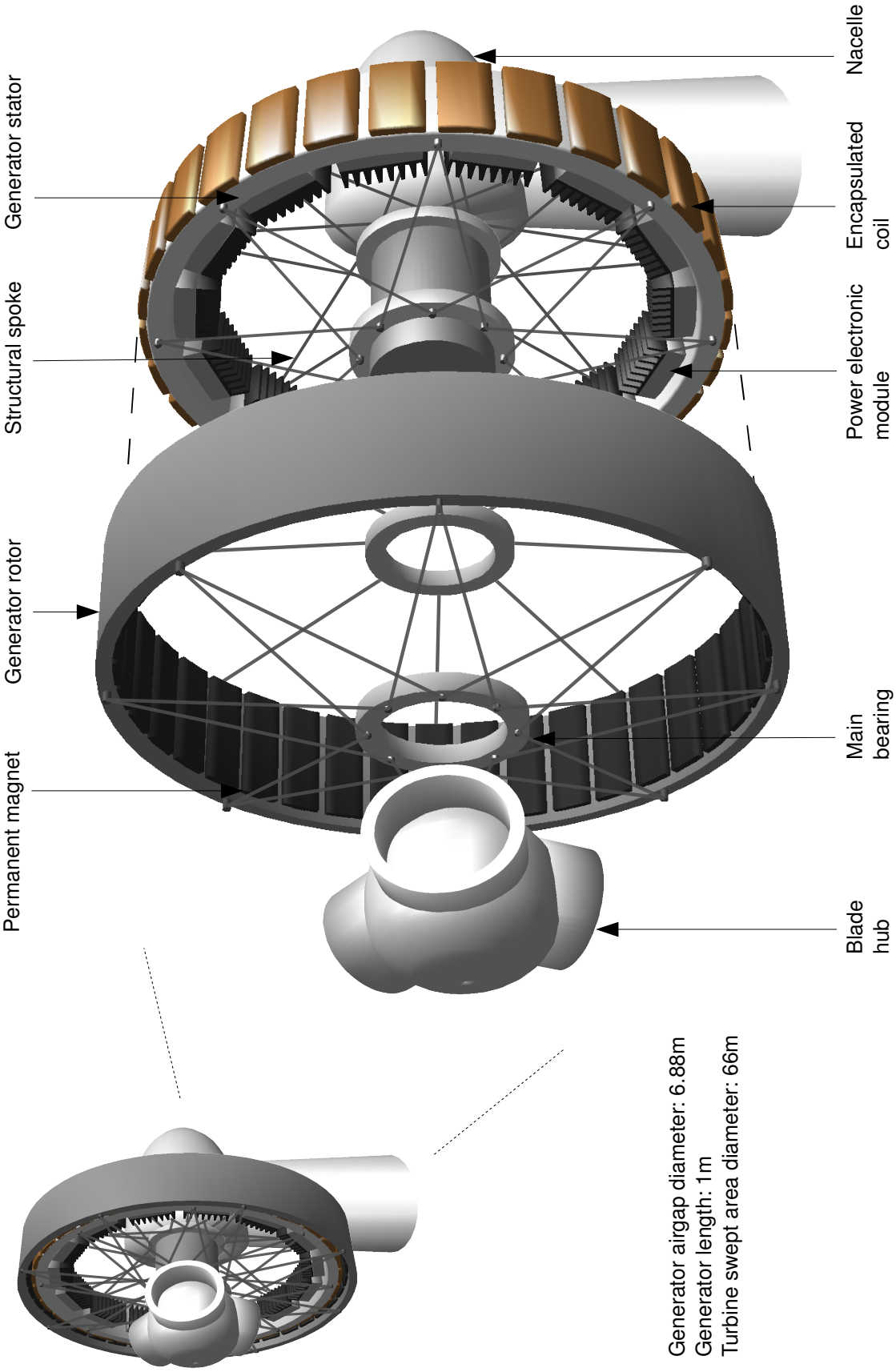


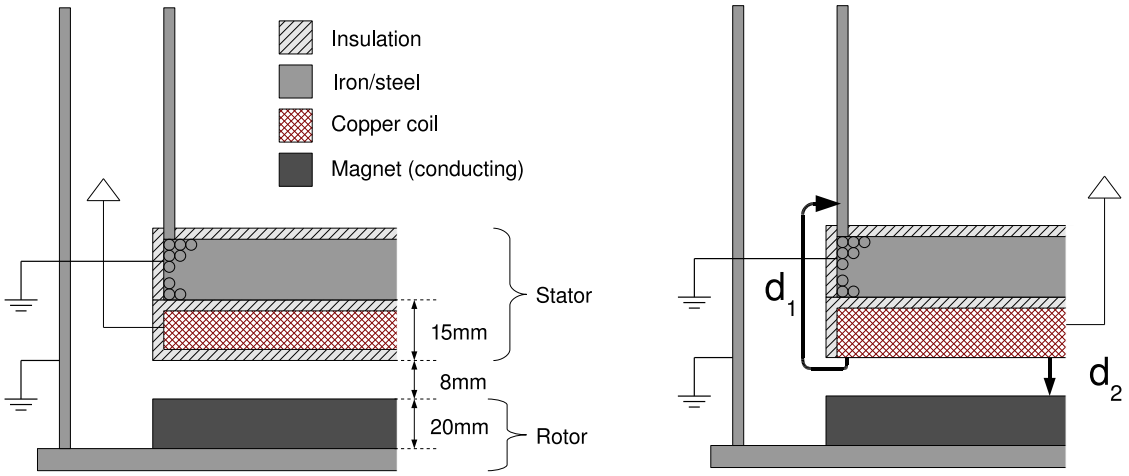
Figure 5.1: Simplified diagram of the generator structure.

so for U_n=11kV the insulation must be designed to withstand 23kV.

5.2.2 Insulation of Generator Coils

The insulation of the stator coils requires a similar approach to that adopted for the field coils of conventional synchronous generators. Insulated copper wire or strip is wound onto bobbins manufactured of polymeric, insulating material capable of carrying the electrical, mechanical and thermal stresses involved. This is then impregneted with an insulating resin.

There are two ways to insulate the coils, the first of which is to encapsulate the coil in a layer of resin thick enough to handle the full 23kV applied to any surface, as shown in Figure 5.2a. The second is to insulate the coil only where it meets the stator back iron, with minimal insulation elsewhere. This is shown in Figure 5.2b. The second approach has the advantage of greater volume for copper and improved heat transfer. The disadvantage is a possiblility of surface tracking, along path d_1 on the diagram, and breakdown of the air in path d_2.



(a) Fully Insulated Coil (b) Partially Insulated Coil

Figure 5.2: Generator Rim Cross Section

Various issues must be considered with both insulation systems:

Structure

The winding bobbins will probably be manufactured from nylon, which has a very good dielectric withstand, and excellend mechanical strength. Nylon softens at

temperatures above 120°C, so operating temperatures will need to be limited below this.

Interturn Voltage

Random winding will be used and the interturn insulation requirements will be low compared with teh coil to ground requirements. In addition a machine designed to be connected to a PWM-based power electronic converter must be insulated to cope with the additional stress of the high dv/dt of the converter and fast transients [17]. These fast transients may be greater than double the normal DC link voltage, but with the proposed power convertion scheme this will be around 1600V, which is small compared with the peak voltage experienced.

Polyimide insulated copper wire or strip will be suitable to provide the necessary interturn insulation, even when subjected to high dv/dt transients. An important factor in the size of the transient voltage, identified in [17], is the cable length connecting the machine and power electronics. In this case the power electronic modules are mounted on the machine so this length is short, so transient voltages will be minimal.

Coil Insulation and Impregnating Resin

The common impregnant for large electrical machine windings is epoxy resin, usually reinforced with glass fibre for mechanical strength, and mica paper to limit the effects of discharge activity. However, these latter components will not be required if the resin is used to impregnate nylon bobbin wound coils of pre-insulated copper wire or strip.

A suitable epoxy resin could be Epoxylite 347, which has a dielectric strength of around 28kV/mm, although in practice a rated stress of 3-5kV/mm is usually used to reduce the risk of discharge activity at points of elevated stress and at voids in the insulation resin. Therefore a surface coating of around 5.8mm of resin would be required to support 23kV to the resin surface if that was grounded. The resin should be injected into the wound coil bobbin assemblies using Vacuum Pressure Impregnation to ensure full impregnation and to avoid the formation of voids. Epoxy resin is also very hard-wearing.

As the coils are only 15mm thick, the required 5.8mm insulation would add

significantly to the airgap size, reducing the generated EMF. It is possible that the resin thickness could be reduced as the electrical stress will be more uniform that in a conventional slotted machine. The partially insulated system, increasing the airgap size by half the amount of the fully insulated system, would reduce this problem.

The partially insulated system relies on the air in the airgap for insulation from the magnets on the rotor. Air has a dielectric strength of 3kV/mm, so 7.7mm of air is required for insulation in the uniform field likely to be found in the airgap. As this is only slightly smaller than the 8mm airgap, the size of the airgap might need to be increased in order to allow for the variation of the airgap size around the machine circumference.

Heat Transfer

In a traditional slotted electrical machine, heat in the stator coils is transferred to the stator iron, then either conducted to the outside of the machine or into air which passes through air ducts in the stator. Water cooling can also be used. In the case of the proposed generator, the stator back iron will be impregnated in resin, and the composite structure of the stator will lead to poor thermal conductivity. Heat transfer will mostly be into the airgap, with the airgap winding providing a large surface area for heat transfer.

Heat transfer will be superior with the partially insulated system as the insulating layer on the airgap side is significantly thinner. If the generator is open to the outside air, a ready supply of cooling air will be present.

Connection Leads

The coils will be manufactured with each individual coil completely enclosed. The leads from the coils to the power electronic modules will be fitted at the time of manufacture, meaning that the coils will have no terminals, and flying leads will need to be provided for termination at the power electronic modules.

Surface Erosion and Tracking

Surface tracking will be an issue with the partially insulated system, with tracking being along path d_1 in Figure 5.2b between the coil face and the stator support

structure. Dirt adhering to the non-insulated inner surface of the coil could cause a non-uniform electric field in the airgap, leading to corona activity.

Even with the fully insulated system, any counductive compounds landing on the coil surface will be raised to coil potential by capacitive coupling. This could lead to surface corona activity leading to a roughening of the surface and greater dirt adhesion, eventually leading to insulation failure due to surface tracking. To avoid this, the outsides of the windings of large generators are coated with a semi-conductive compound which is then tied to ground potential [36].

Coating with a semi-conductive compound is expensive, and not possible with the partially insulated system. If the epoxy resin is properly cured to a glassy smooth surface this should be highly resistant to surface tracking, however a surface coating of anti-tracking paint will be desirable.

Maintenance

The design of the generator is such that it would be difficult to access the coils for maintenance and cleaning without removing and dismantling the generator, so the coils would need to be designed to operate reliably for the entire lifetime of the generator, i.e. around 20 years. Furthermore, the coils will be exposed to outside air, so the insulation must be able to withstand a dirty environment and the anti-tracking paint will help achieve this objective.

Generator Flexibility

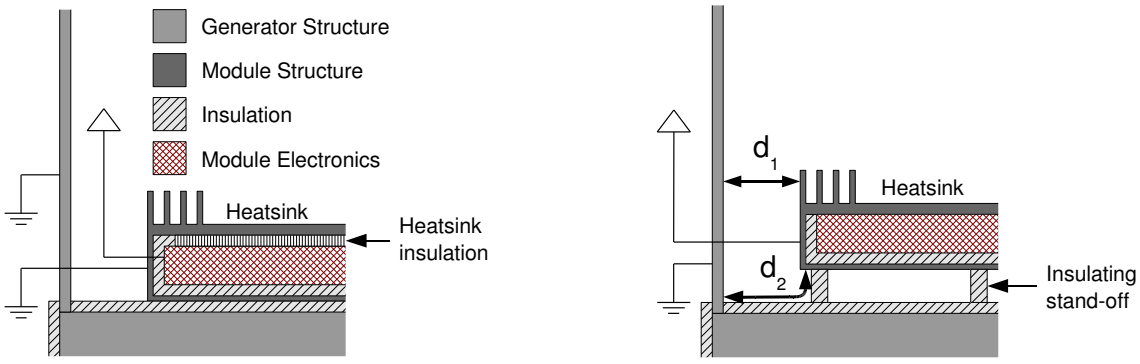
The lightweight nature of the generator structure could lead to considerable flexibility, leading to possible fluctuations in airgap size. It is not inconceivable that the rotor and stator could come into contact, and seismic motion of generator parts could lead to abrasion of the coil flying lead insulation so the design will need to protect against this.

5.2.3 Insulation of Power Modules

The power electronic modules can either be fully insulated, as shown in Figure 5.3a, or uninsulated, as shown in Figure 5.3b. With a fully insulated module, the outer surface of the module and the heatsink will be at the machine ground potential. The module electronics must be surrounded by a layer of insulation capable of

withstanding the full 23kV insulation requirement, and a way must be found to transfer heat from the power devices to the heatsink.

With an uninsulated module, the outer surface of the module and the heatsink will be at the module local ground potential, with insulation from metal parts of the generator being provided by air and the insulation around the iron core of the generator. In this case problems may occur with corona discharge in the air and surface tracking on the generator core insulation.



(a) Fully Insulated Power Module (b) Non-Insulated Power Module

Figure 5.3: Power Module Insulation

Module Encapsulation

In order to provide a high degree of environmental protection and mechanical support the modules will be encapsulated. A good encapsulant would have a high dielectric strength as well as a high thermal conductivity, and would be flexible enough to cushion the module from vibration and stresses from thermal expansion.

A class of encapsulant which fulfils these requirements is silicone elastomer, which also has the advantages of high resistance to surface tracking and high environmental stability [37]. As an example, the properties of two thermally conductive encapsulants, SE4410 and SE4447, from Dow Corning are shown in Table 5.1, along with the Epoxilite 347 resin from the previous section. It can be seen that the epoxy resin is a much harder and stronger compound, which is necessary for providing mechanical support for the coil, while the elastomer encapsulants are more flexible and have greater thermal conductivity.

The modules would most likely be potted in an aluminium container to provide additional protection and mechanical support, as well as controlling electromagnetic

Material	Dielectric Strength (kV/mm)	Thermal Conductivity (W/mK)	Tensile Strength (N/mm^2)	Elongation at Break
SE4410 Silicone	26	0.92	6.83	60%
SE4447 Silicone	10.6	2.5	0.14	20%
Epoxilite 347	28	0.21	110	1.5%

Table 5.1: Comparison of encapsulation compounds

interference. For a fully-isolated module, the container would be connected to the machine ground in order to prevent it being raised in potential to the module voltage by capacitive coupling. For a non-isolated module the case will be connected to the module local ground, along with the heatsink.

Heatsink Isolation

IGBT modules are typically made by bonding copper on to either side of a ceramic stubstrate, usually aluminium oxide or aluminium nitride, a process known as Direct Bonded Copper (DBC) [38]. The semiconductor devices are then soldered onto the surface of the top copper. Typically the substrate is around 0.6mm thick, and with the dielectric strength of aluminium oxide being 16.7kV/mm this gives a theoretical breakdown voltage of 10kV.

Unfortunately imperfections in the applied copper can lead to onset of partial discharge at much lower voltages, usually around 3.5kV. This problem can be solved using an Active Metal Brazing (AMB) process instead of DBC, although this is much more expensive. Recent advances in the field of DBC substrate manufacture allow the breakdown voltage to approach the theoretical value [32].

For a non-isolated power electronic module, the heatsink is connected to the module local ground, so the IGBT module only has to insulate against the module local voltage, meaning that standard IGBT modules can be used. For an isolated power electronic module, the IGBT module must insulate against the full 23kV insulation requirement.

In theory, a 1.4mm layer of aluminium oxide or 1.35mm layer of aluminium nitride would be sufficient to isolate the required voltage, using the theoretical maximum dielectric strength. With the thermal conductivity of aluminium oxide at 18W/mK and aluminium nitride at around 150W/mK, the thermal resistance for a 5x10cm power electronic module, consisting of multiple switching devices on a

ceramic substrate, would be 0.016K/W for aluminium oxide and 0.0018K/W for aluminium nitride. With semiconductor power losses in one module estimated to be around 500W, a temperature rise of 8°C would occur with aluminium oxide and 0.9°C with aluminium nitride.

The disadvantage of this approach is that it requires custom made power electronic modules, which eliminates the cost advantage of using standard parts. As power module substrates are usually made with a standard thickness of 0.6mm, thicker substrates may not be available or may be expensive. Liquid cooling using a non-conductive fluid is another option for full isolation, but increases complexity and introduces a single point of failure for the system, in a location where repairs are difficult.

Connection Leads

The connection leads to the generator coils are attached to the coils themselves, so an electrical connection must be made to the power electronic modules, as well as the series connections between them. For the non-isolated modules, the connections will be standard low voltage connections, with insulating sleaves covering the connections to protect them from the environment.

The isolated modules require proper high voltage bushings for the connections, specified according to the relevant engineering standards. These require electricians with specific high voltage skills to make the connections, increasing the manufacturing costs.

It is expected that communication and synchronisation signals to the modules will be carried by fibre-optic cable to provide the required isolation.

Corona Discharge and Dielectric Breakdown

Having non-isolated power modules means relying on the air surrounding the power modules for insulation between the power modules and the conducting parts of the generator, and between the power modules themselves. The air insulation can break down in two ways: either classic dielectric breakdown, where the electric field strength exceeds the dielectric strength of the air, or corona discharge.

Corona discharge occurs at electric fields significantly below the dielectric breakdown strength of air, in the presence of a non-uniform electric field, usually occuring

when the maximum field strength is over 5x the average. This can lead to localised ionisation in the areas of highest stress, allowing a current to flow [39]. This does not usually cause catastrophic breakdown, but over time can erode the conducting components until the point where failure occurs.

This type of breakdown is unlikely to occur between adjacent modules, where the voltages are low relative to the maximum voltage and the heatsink sides are almost parallel. This means that the modules can be placed close together, with the dielectric strength of air being 3kV/mm a distance of 0.7mm could theoretically be used to insulate modules at 1000V difference, allowing for 1000V switching spikes. The distance would need to be increased to provide resistance to contamination, in practice a few cm could be used.

Corona discharge is most likely between the live module heatsinks and the geenrator spokes, with the sharp edges usually found on typical extruded aluminium heatsinks leading to a high localised field strength. The likely path is shown as distance d_1 in Figure 5.3b. The electric stress required for the initiation of corona discharge is given by Peek's law, shown in Equation 5.1 below, for parallel cylinders:

$$E_i = 30\delta\left(1 + \frac{0.301}{\sqrt{\delta r}}\right) \tag{5.1}$$

where E_i is the inception stress in kV/cm, δ the relative air density and r the cylinder radius. From the inception stress, the inception voltage for various gap distances can be calculated using Equation 5.2, where S is the gap distance. If the heatsink and spokes are modelled as parallel cylinders, then some typicall corona inception voltages for various curve radii are shown in Figure 5.4.

$$V_i = E_i d \ln\left(\frac{S}{r}\right) \tag{5.2}$$

It can be seen that a smaller curve radius gives a lower corona inception voltage for a given gap distance. Furthermore, gap distance starts to have a smaller effect on the inception voltage at larger distances. Based on these results, it would be advisable to round the edges of the heatsink fins in order to reduce the maxium electric field strength, if this is done on a heatsink using 2mm wide fins then a gap distance of only a few cm will be enough to prevent corona discharge. The above is only an approximation and a more detailed analysis of the electric field strength

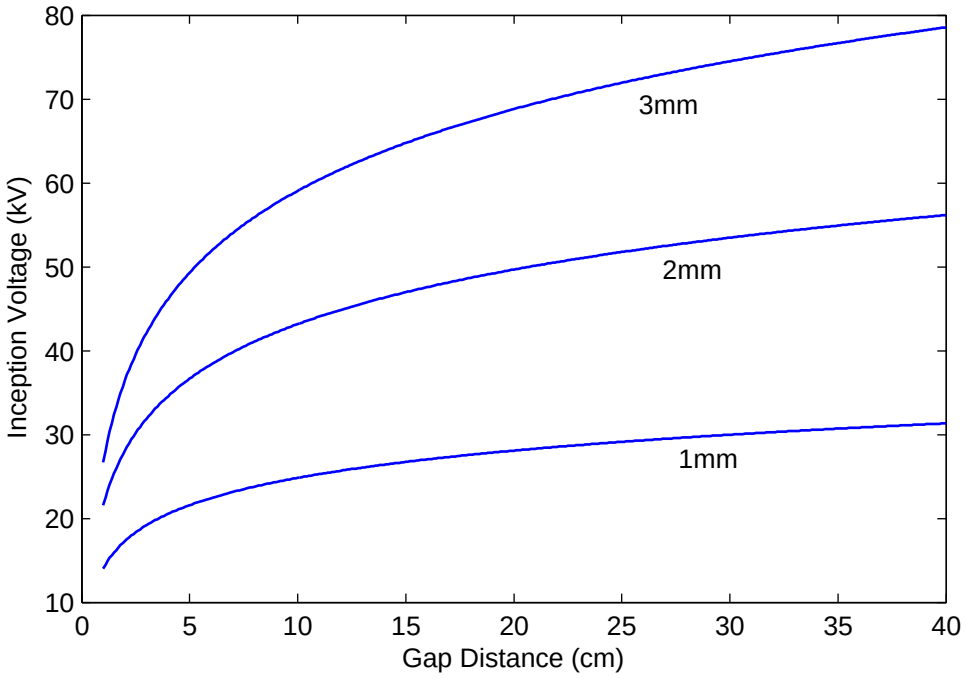


Figure 5.4: Variation of Corona Inception Voltage with Curve Radius

would be needed for accurate predictions of corona inception voltage.

Surface Tracking

Tracking is the formation of a permanent conduction path across the surface of an insulator, often caused by the degradation of the insulation itself, and usually taking many years to manifest. Tracking usually occurs with organic materials, where small discharges carbonise the insulation, causing a conducting path to form. Non-organic materials will not char, but discharges will roughen the surface, leading ot adhesion of dirt, increasing the conductivity [37].

In the fully-insulated module, tracking may occur around the joining of different insulation systems, such as around the cable bushings and around the heatsink insulation. These paths are shown in Figure 5.5 as d_1 and d_2 respectively. This should not be a problem provided large overlaps are provided between the different insulation systems and a proper bonding is achieved to minimise voids.

Tracking may occur in the non-insulated module between the metal case of the module and the metal parts of the generator, such as the spokes, along distance d_2 in Figure 5.3b. Tracking can be controlled by having a smooth hydrophobic surface finish. This prevents dirt from adhering to the insulator and ensures that water on

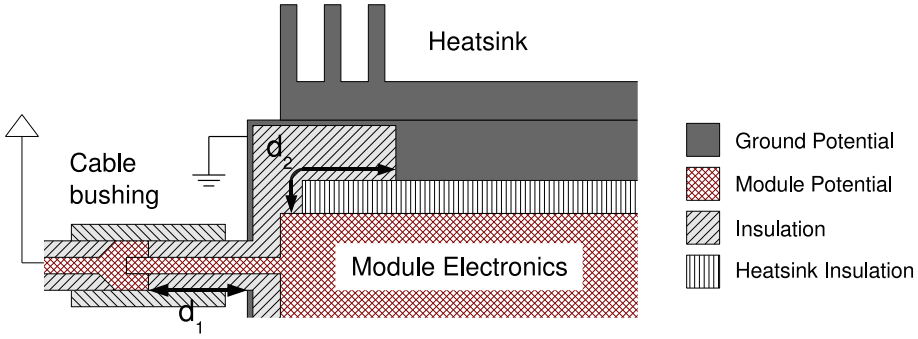


Figure 5.5: Tracking in Insulation of Fully Insulated Module

the surface will form droplets rather than a conductive film. This sort of finish is usually achieved through the use of an anti-tracking paint.

If a nacelle is not used then it is important to design the inner rim of the generator stator such that rainwater is not allowed to pool anywhere, as this could form a conduction path and also allow the deposition of dirt. Areas where this could occur include around the cables connecting the modules to the coils and the cables between modules. Another problem could be low pressure turbulent areas downwind of the modules, which could lead to deposition of dirt. The tracking distance can be increased by mounting the power module on insulated stand-offs, which would also allow air to flow underneath.

5.3 Lightning Strike Protection

Wind turbines are sited in open areas, and are usually the highest objects around, which means that a turbine is highly likely to receive a direct strike during it's lifetime. Research has shown that strikes to adjacent turbines and to the distribution network or communication systems can also affect turbines, and this is often of greater significance in turbine failures due to lightning strikes [40]. There are three risk factors to be considered [41]:

1. Damage to blades from direct strikes, caused by strikes to the blade tips or along the length of the blades.

2. Damage caused by surge currents, which can be caused by surge currents either from direct strikes or indirect strikes to power and communication lines.

3. Damage caused by voltages, which are induced in power and control circuits adjacent to the down-conductors which carry the lightning current to earth.

5.3.1 Protection of Conventional Turbines

In a wind turbine, by far the most likely point for a lightning strike to occur is the turbine blade tips. The lightning protection system consists of a metal part in the blade tip, with a lightning conductor running down the inside of the blade to the blade hub, where it connects to the earthing system of the turbine [42]. The turbine earthing system is designed to provide a low impedence connection to ground, to conduct the energy from the lightning strike away from vulnerable equipment in the turbine.

The turbine power and control electronics are usually contained within steel cubicles, which are connected to the turbine ground, and provide good resistance to surge currents and induced voltages. The connection cables are a source of vulnerability, as are any remote sensors, such as the meteological sensors usually mounted on top of the turbine nacelle. For this reason surge protectors are installed on the incoming and outgoing cables to limit the induced voltage, on both the power and data cables. A good grounding system will minimise induced voltage as well as reduce problems with electromagnetic interference.

5.3.2 Issues Specific to the Proposed Generator

It is likely that the generator will be exposed to the outside air, placing it at risk from a lightning strike, although a strike to the turbine blade tips is still far more probable. The generator coils and power electronic modules are contained within a cage formed by the rotor back iron and spokes, which are connected to ground, meaning that the rotor is the most likely location for a lightning strike on the generator. In this case the surge current will be conducted around the rotor back iron and through the spokes to the generator hub.

Even if the power electronic modules are not directly conducting the current surge they may still experience an induced voltage due to high electromagnetic fields. The aluminium boxes containing the power modules will block external electric fields, preventing high voltages from being induced inside the module electronics,

although magnetic fields could be a problem. If this is the case then the box could be made from steel instead, which would attenuate a magnetic field as well.

Surge protectors would need to be used on the input and output terminals of the modules to prevent any induced voltages from damaging the switching devices. These would be connected to the module local ground. As the modules each have a different local ground potential, any rise in the local ground potential of one module will cause a rise in the terminal voltages of the adjacent modules, causing the surge protectors on these modules to activate. This will raise the potential of the next module etc. In this way a current surge will be conducted through all the modules to the generator ground.

The cascaded nature of the surge protection scheme means that high voltages could result if the surge protection devices fail on one module. For this reason it is important that several fused redundant surge protection devices are used. The use of fused redundant protection paths is recommended in [41] for conventional turbines but it is far more important here due to the difficulty of replacing the power electronic modules.

The voltage at which the surge protector operates would need to be higher than the peak voltage output of the module, i.e. the module peak DC-link voltage, in order not to be triggered during normal operation. This means that a higher voltage rating may be required for the module switching devices, which would increase the cost. Alternatively the module DC-link voltage could be reduced, but this would reduce the output voltage of the cascaded multilevel inverter.

Data connections to the power electronic modules will be through fibre-optic cables, due to the elevated voltages of the modules, which will provide immunity to lightning-related problems.

5.4 Summary of Insulation Issues

While the insulated power module offers advantages in terms of elimination of corona and tracking problems, it does so at the cost of reduced cooling efficiency and greater manufacturing complexity. The non-insulated module is simpler to manufacture, and it has been shown that corona discharge will not be a significant issue at the distances involved.

Susceptibility ot surface tracking on a non-insulated module is unknown, and will need to be tested as it depends heavily on the machine design and cable routing, but a coating of anti-tracking paint will reduce the problem. A further advantage of the non-insulated module is that the system voltage can be increased simply by increasing the isolation distances, limited only by the geometry of the machine. Increasing the voltage of an insulated module requires increasing the thickness of the insulation.

Insulating the generator coils has been shown to significantly increase the airgap size, relative to uninsulated coils, which will reduce the efficiency of the generator. The materials and insulation thicknesses used in standard slotted electrical machines were considered – it may be possible to reduce the insulation thickness in this slotless design.

Compared to a system with a 3.3kV output and step up transformer, an 11kV system must either have a larger airgap size to accomodate the extra insulation, or a smaller coil volume. If a larger airgap is used, the size of the permanent magnets will need to be increased, increasing the cost. If a smaller coil volume is used, the coil resistance will increase, which will reduce the electrical efficiency of the generator. It is therefore important to balance the benefits of eliminating the step-up transformer with the disadvantages of having to design the generator to handle a higher voltage output.

The generator structure should provide protection to the power modules from direct lightning strikes, but they could still be vulnerable to induced voltages and current surges from the grid connection. For this reason surge protection devices must be used to limit the voltages on the module terminals to prevent damage to the switching devices. The cascaded nature of the surge protection, and the difficulty of accessing the power modules, means that redundancy and reliability of the surge protection is of much greater importance than in conventional turbine designs.

Chapter 6

Development of a Control Strategy

In chapter 4 a power module topology, featuring a boost rectifier input and fundamental frequency output, was chosen for the modular cascaded multilevel inverter. This chapter will cover the control strategy for the boost rectifier, as well as the control strategy for the DC-link voltage of the module. Control of the inverter will also be mentioned, although this has been developed in collaboration with other researchers.

6.1 Control System Structure

A major problem with multilevel inverters is that of balancing the DC-link voltages of the different levels, which must normally be controlled by the inverter [31] [43], with the inherent complexity of the control system limiting the number of levels possible. The proposed system solves the problem of DC-link voltage balancing by having the rectifiers control the DC-link voltage of each inverter module, meaning that the inverter only has to control the real and reactive power output.

The overall structure of the turbine and inverter control system is shown in Figure 6.1, and consists of a number of cascaded control systems. The function of these is as follows:

- The turbine overall controller handles the maximum power tracking of the turbine along with power limiting at high wind speed. It produces a demand for real and reactive power output for the turbine, based on the turbine speed and the grid reactive power demand.

- The inverter controller sets the phase and magnitude of the inverter output voltage, relative to the grid voltage, in order to achieve the required real and reactive power outputs. Some of the inverter control algorithm will be based in a central controller, and some of it in the individual module controllers. The inverter output voltage amplitude is adjusted by changing the DC-link voltages of the inverter modules.

- The DC-link voltage controller maintains the DC-link voltage at a value set by the inverter controller, which it does by setting the current demand to the rectifier controller.

- The rectifier controller tracks the generator coil EMF and controls the coil currents to be sinusoidal and in phase with the EMF. An estimation of the generator speed is produced, which is fed back to the turbine overall controller.

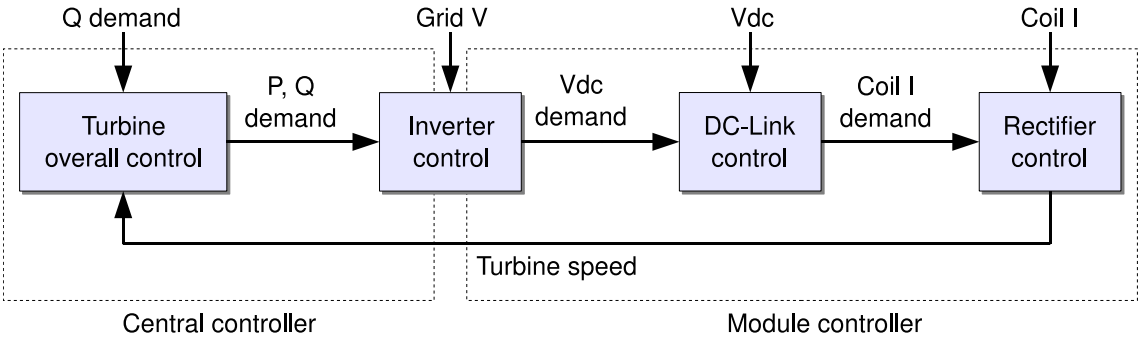


Figure 6.1: Overall control structure

These control systems will be investigated next, with the exception of the turbine overall controller. Turbine overall control was considered in chapter 3 for conventional wind turbines, and in this case will not differ significantly from the conventional methods.

The aim for the control system design is to produce a controller which can be implemented on a microcontroller or digital signal processor (DSP), with minimal analogue signal processing, and minimal peripheral components. This may limit the choice of algorithms available, but it is beneficial for several reasons:

- Having fewer components means that a smaller printed circuit board (PCB) will be required for the controller. This is important as a large number mod-

ules will need to be built, and a smaller PCB will result in space savings, particularly for a prototype system.

- Having fewer components will also reduce the cost, both of components and manufacture, with the smaller PCB requirement reducing cost as well.
- A digital system allows controller parameters to be easily adjusted, potentially while the system is in operation. Parameters in an analogue system must be adjusted by changing components on the board.
- Parameters in a digital system are exact, unlike an analogue system where they are affected by the tolerance of the components and temperature.

The control of the boost rectifier can be divided into two problems: firstly the control of the coil current, which must be sinusoidal and in phase with the coil EMF in order to maximise the coil utilisation. Secondly the position of the generator EMF must be estimated in order to correctly control the coil current. The generator EMF could be found from the generator position using a position encoder, or from search coils, but these would increase cost and complexity.

6.2 Machine and Rectifier Model

Simulation and control of the system was introduced in Section 4.2, and will be expanded in this section. The circuit for the boost rectifier, with two coils at 90° phase separation, is shown in Figure 6.2. The machine EMF e for both of the coils connected to one module is given by Equation 6.1, where θ_e is the machine electrical angle and k is a constant. The machine electrical angle is related to the mechanical angle θ_m by Equation 6.2, where N is the number of magnetic pole pairs.

For a given coil n, the average voltage at the rectifier terminals v_n, is related to the duty cycle of the rectifier PWM switching d, and the DC-link voltage v_{dc} by Equation 6.3.

$$\begin{bmatrix} e_1 \\ e_2 \end{bmatrix} = k\omega \begin{bmatrix} \sin(\theta_e) \\ \sin(\theta_e + \pi/2) \end{bmatrix} \qquad \text{where } \omega = \frac{d\theta_e}{dt} \tag{6.1}$$

$$\theta_e = N\theta_m \tag{6.2}$$

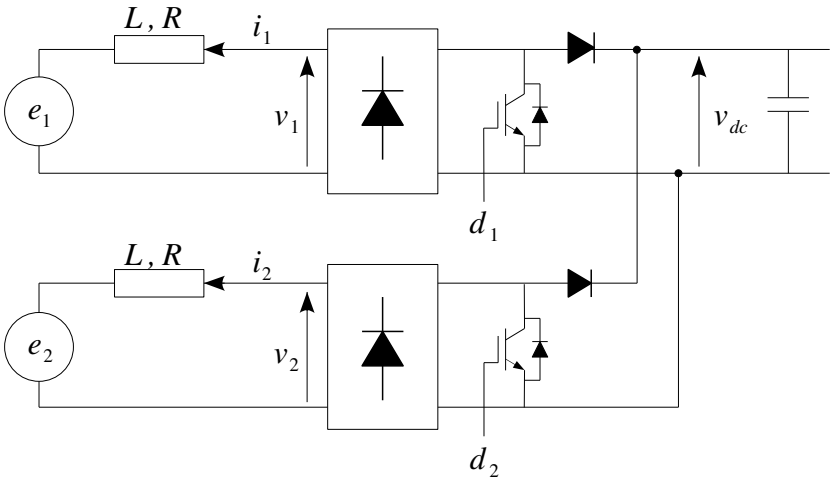


Figure 6.2: Boost rectifier circuit

$$v_n = (1 - d_n)v_{dc}sign(i_n) \tag{6.3}$$

The PWM waveforms for the coil are synthesised using a triangular carrier, shown in Figure 6.3. The carriers for the two coils are phase shifted by 180° so that the switching instances are interleaved, this will slightly reduce the current ripple from the rectifier into the DC-link. Sampling of the current is done at the minima and maxima of the carrier waveforms, at twice the switching frequency. This is done so that the sampling occurs away from switching events, which could cause interference.

6.2.1 Effects of Airgap Eccentricity

It is likely that a lightweight generator, with large diameter, of the sort being considered here will have an uneven airgap size, which will affect the magnetic flux linked by the coils and hence the coil EMF. This eccentricity could occur both in the rotor and the stator, and could also dynamically change depending on the loads applied to the generator.

The effects of eccentricity in the stator will be that different coils will experience different EMFs, but these differences will be constant with time. Eccentricity in the rotor will cause the EMF to vary depending on the rotor position. In both cases eccentricity will affect both coils almost equally, due to their close proximity on the machine.

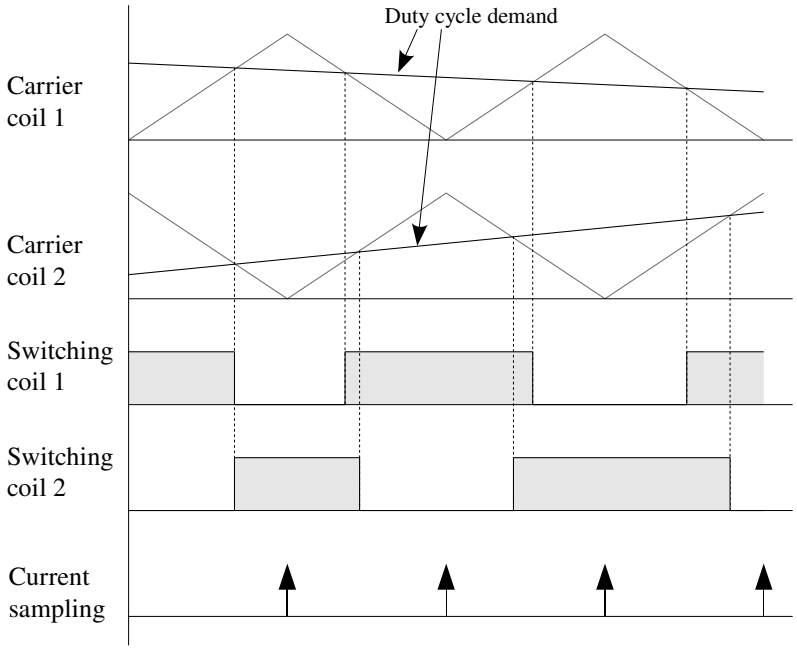
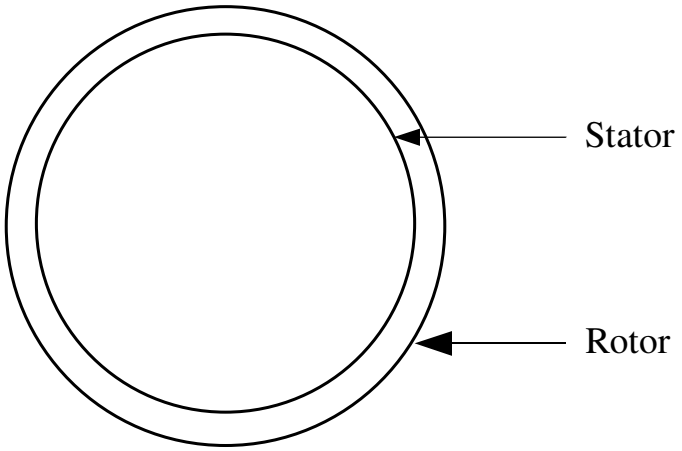


Figure 6.3: Rectifier PWM waveform synthesis

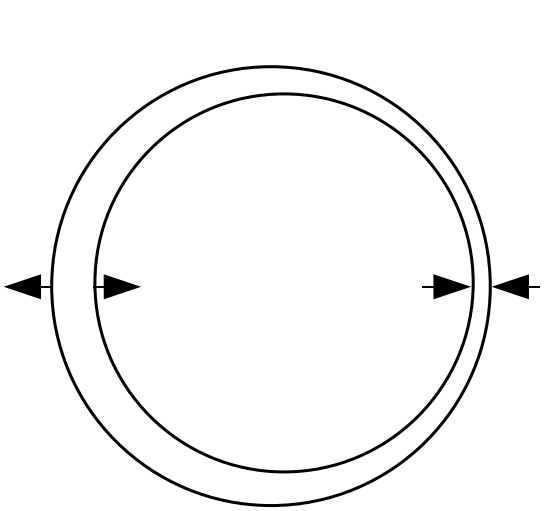
Rotor eccentricity will cause Equation 6.1 to be modified to Equation 6.4. Here the eccentricity is assumed to cause sinusoidal variations in the coil EMF which may occur at various multiples i of the generator rotation speed and various phase offsets ϕ_i. θ_m is the generator mechanical position. Any change in the airgap size, due to distortion in the machine structure, will increase the force between rotor and stator where the airgap size is reduced, and reduce the force where the airgap size is increased, and this will tend to re-inforce any structural distortion.

$$\begin{bmatrix} e_1 \\ e_2 \end{bmatrix} = \omega \left(k_0 + \sum_{i=1}^{n} (k_i \sin(i\theta_m + \phi_i)) \right) \begin{bmatrix} \sin(\theta_e) \\ \sin(\theta_e + \pi/2) \end{bmatrix} \tag{6.4}$$

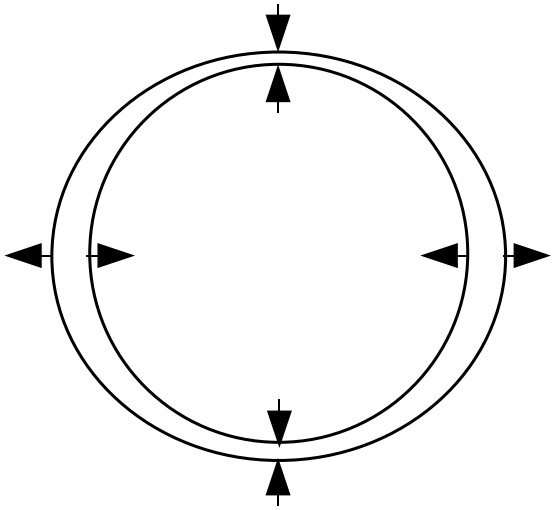
Eccentricity is most likely to be in the form of an offset of the rotor or stator, as in Figure 6.4b, which will result in a first order eccentricity at the rotation speed. Ovalation of the rotor or stator, shown in Figure 6.4c, would result in a second order eccentricity at twice the rotation speed. Higher orders may occur but would be much smaller.



(a) Generator without eccentricity.



(b) 1st order eccentricity.



(c) 2nd order eccentricity.

Figure 6.4: Generator Eccentricity

6.3 Control of Coil Current

A proportional or proportional-integral controller can be used to set v in Equation 6.3 to directly control the current to the desired value, but in practice such systems offer poor performance in terms of current waveform shape and lag relative to the voltage [44]. An improved system would feed forward a value for the applied voltage v in order to achieve the desired current.

If e, v and i are sinusoidal then they can be represented as phasors E, V and I respectively, shown in Figure 6.5. If the position and magnitude of the machine EMF vector E, is known then the relative position of V can be set in order to achieve the aim of unity power factor operation, based on the desired current I^*, the machine inductance L and resistance R. This is most easily carried out in the rotor reference frame, with the q-axis aligned to the EMF of the lead coil. The formula for calculating the feedforward voltages is given in Equation 6.5, where the magnitude of the machine EMF is estimated from the angular velocity ω and constant k.

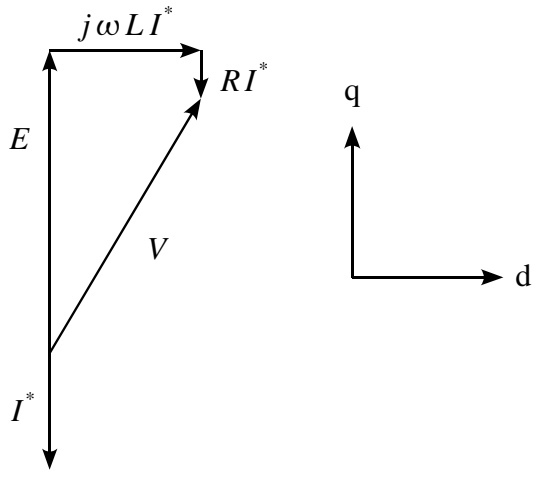


Figure 6.5: Boost rectifier phasor diagram

$$\begin{bmatrix} V_d \\ V_q \end{bmatrix} = \begin{bmatrix} 0 \\ k\omega \end{bmatrix} + \begin{bmatrix} R & 0 \\ 0 & R \end{bmatrix} \begin{bmatrix} I_d^* \\ I_q^* \end{bmatrix} + \begin{bmatrix} 0 & -\omega L \\ \omega L & 0 \end{bmatrix} \begin{bmatrix} I_d^* \\ I_q^* \end{bmatrix} \tag{6.5}$$

Transformation of the feedforward voltages from the rotor to the stator reference frame is carried out using a standard reference frame transformation, given

in Equation 6.6 in the complex notation and in Equation 6.8 in vector notation, where θ_e is the machine electrical angle. The transformation produces a 2-phase result which corresponds to the voltages for the two coils supplying the module, so no further transformations are required. The transformation from the stator to the rotor reference frame is given in equations 6.7 and 6.9 in the complex and vector notations respectively.

$$(v_1 + jv_2) = (V_d + jV_q)e^{-j\theta_e} \tag{6.6}$$

$$(V_d + jV_q) = (v_1 + jv_2)e^{j\theta_e} \tag{6.7}$$

$$\begin{bmatrix} v_1 \\ v_2 \end{bmatrix} = \begin{bmatrix} \cos\theta_e & \sin\theta_e \\ -\sin\theta_e & \cos\theta_e \end{bmatrix} \begin{bmatrix} V_d \\ V_q \end{bmatrix} \tag{6.8}$$

$$\begin{bmatrix} V_d \\ V_q \end{bmatrix} = \begin{bmatrix} \cos\theta_e & -\sin\theta_e \\ \sin\theta_e & \cos\theta_e \end{bmatrix} \begin{bmatrix} v_1 \\ v_2 \end{bmatrix} \tag{6.9}$$

This controller structure is shown in Figure 6.6 below, where it is assumed that the generator electrical angle θ_e and angular velocity ω are known, or accurately estimated. From the estimation of the generator angular velocity ω the feedforward voltage V is calculated in the rotor reference frame, based on the current demand I^*. This voltage is then transformed to the stator reference frame using the generator electrical angle θ_e to produce sinusoidal feedforward voltages v_1 and v_2, with the reference frame transformation being denoted in the diagram as $e^{j\theta_e}$. The duty cycles for the PWM system, d_1 and d_2 are calculated and applied to the rectifiers, and the result is coil currents i_1 and i_2.

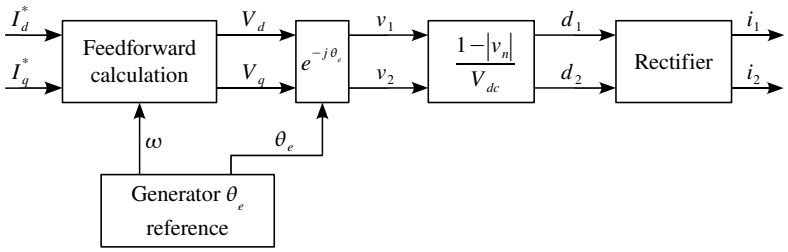


Figure 6.6: Basic current controller structure

In Section 4.2 it was assumed that v could take any value. Unfortunately the

presence of the two-quadrant bridge rectifier in the circuit means that the voltage cannot be of a different sign to the coil current. This causes a problem immediately after the zero-crossing of the current, and is illustrated in Figure 6.7. This results in distortion in the current waveform, known as 'cusp distortion' [44].

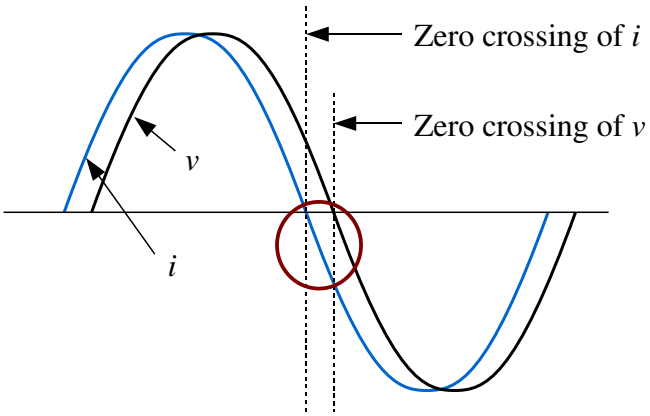


Figure 6.7: Current zero-crossing problem

There are various ways of eliminating cusp distortion, with the easiest, used in [44], being to hold the applied voltage at zero for a preset period after the current zero crossing in order to allow the current to increase to the correct level. This delay has been calculated to be twice the delay between the EMF and applied voltage. This method does not give satisfactory results in a digital system, as the exact time of the zero crossing is different from the point at which the controller detects the zero crossing, depending on the sampling instances of the controller, resulting in different current magnitudes from cycle to cycle.

The method proposed is to use a proportional controller to force the current to follow a current reference waveform, similar to the approach used in [44], a system which can be implemented digitally. This results in a controller structure like that in Figure 6.8. Here, in addition to calculating the feedforward duty cycle d_{ff} as before, the instantaneous current demand i^* is also calculated. A proportional controller then controls the applied voltage to achieve the desired current, with the the feedforward duty cycle added to the output of the controller. Away from the current zero crossing the output of the proportional controller should be zero.

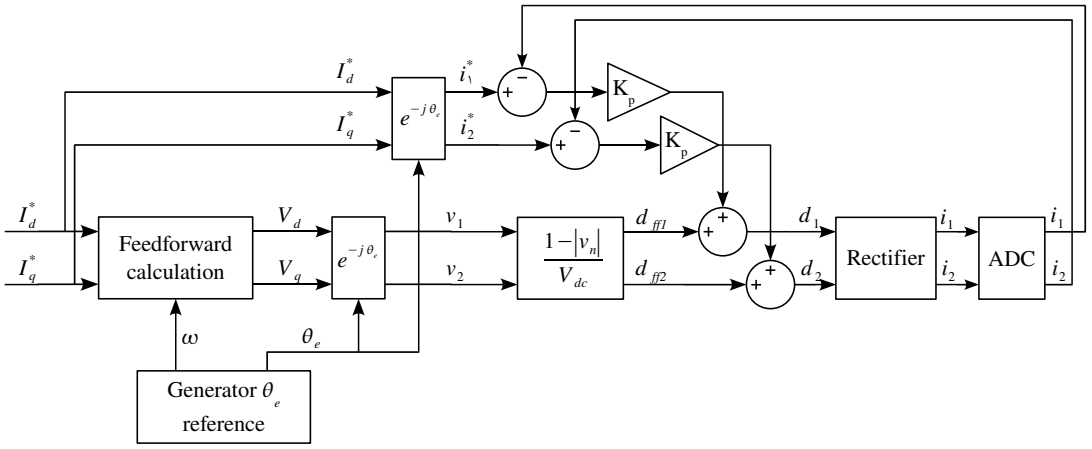


Figure 6.8: Improved current controller structure

6.3.1 Simulation of Coil Current

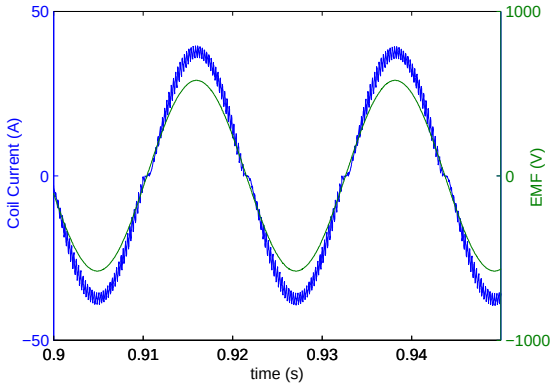
The rectifier was simulated using Simulink, using the method described in Section 4.2.1. The basic controller simulation was structured as in Figure 6.6, with the EMF and feedforward voltage being derived from the same phase reference. The feedforward voltage was calculated at an interval of 8kHz, corresponding to the sampling instances shown in Figure 6.3.

The improved controller simulations was structured as in Figure 6.8, with the EMF and feedforward voltage being derived using the same method as the simple case. The analogue to digital converter (ADC) was modelled as a zero order hold circuit, sampling at 8kHz.

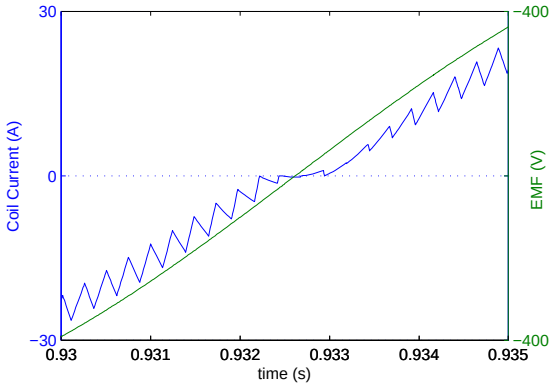
Simulation was carried out for the 1.8MW system at the peak power condition of 22rpm generator speed and 28.4A rms coil current, with a constant DC-link voltage of 700V. Simulation was also carried out for the improved current controller at the minimum power condition of 7.1rpm and 1.2A rms coil current.

Using the basic current controller, cusp distortion leads to some third harmonic distortion in the current waveform, shown in Figure 6.9a, with the zero crossing instance shown in more detail in Figure 6.9b. With cusp distortion compensation applied, an improvement is seen, shown in Figures 6.9c and 6.9d. However the current in each cycle will fluctuate slightly, as shown in Figure 6.9e.

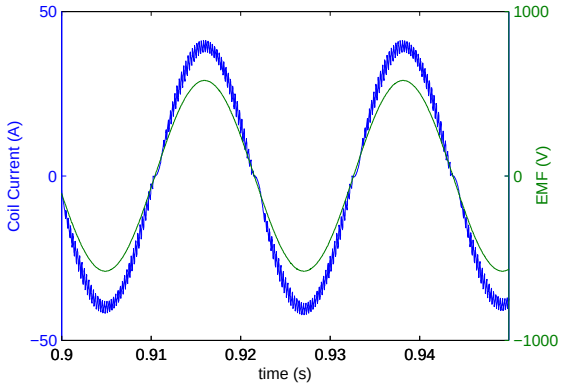
The improved control method, featuring the current proportional controller, produces a waveform with low distortion, shown in Figures 6.10a. Testing at the minimum power conditions produces a waveform shown in Figures 6.10b and 6.10c. In



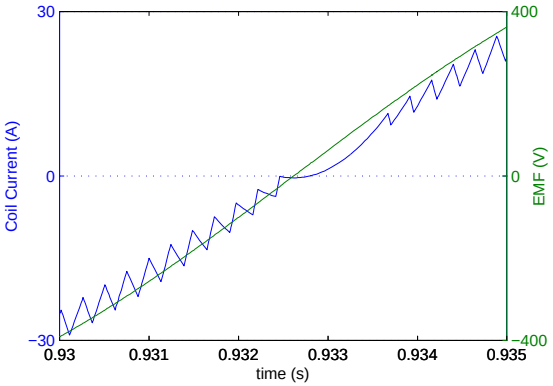
(a) Basic control of coil current



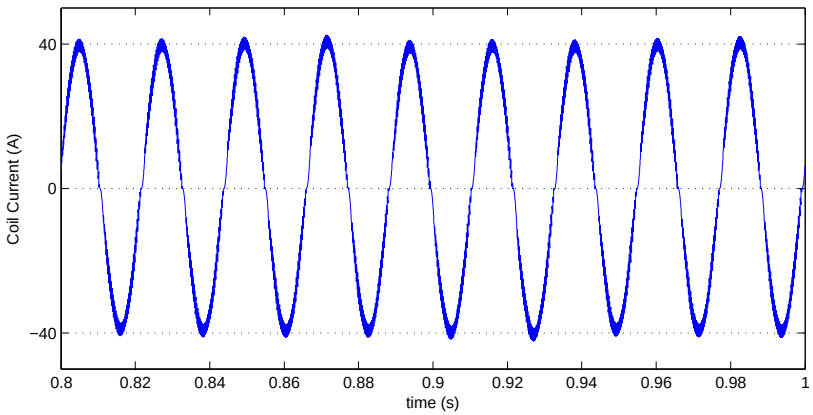
(b) Cusp distortion in basic controller



(c) Controller with cusp distortion correction



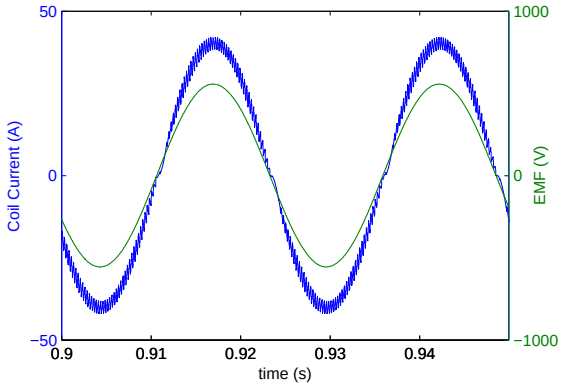
(d) Correction at current zero crossing



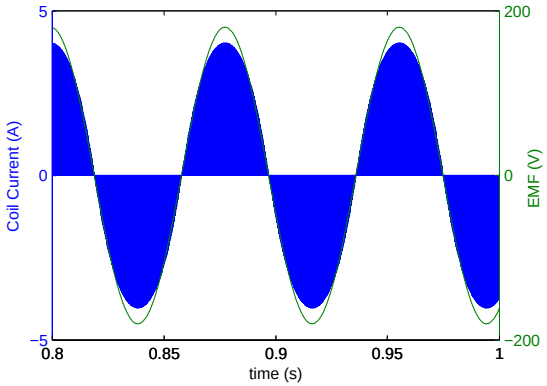
(e) Current fluctuations due to cusp distortion correction

Figure 6.9: Simulated coil current waveforms

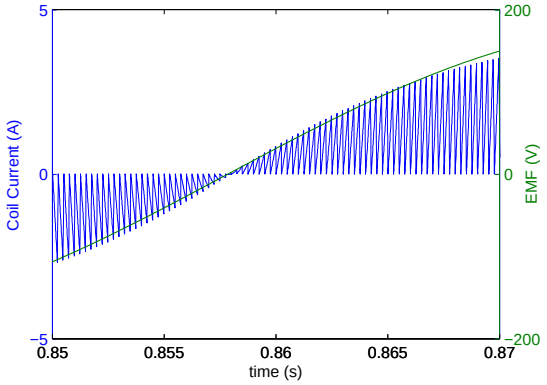
these conditions the coil current is starting to become discontinuous. No fluctuation in current between cycles is visible, as shown in Figure 6.10d.



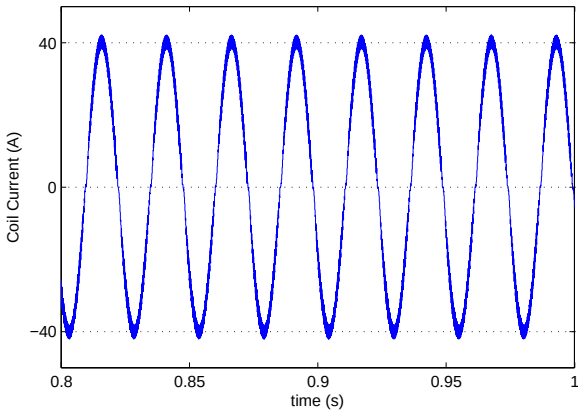
(a) Coil current at maximum power conditions



(b) Coil current at minimum power conditions



(c) Switching ripple at minimum power conditions



(d) Coil current at maximum power conditions

Figure 6.10: Simulated coil current waveforms for improved controller

6.3.2 Airgap Eccentricity Considerations

Airgap eccentricity will cause the estimated EMF to differ from the actual value if the EMF is assumed to be proportional to the machine speed. If a basic controller is used, where a feedforward voltage controls the current, the actual current could differ significantly from the desired current.

The variation of EMF magnitude leads to a change in the reactive power the rectifier attempts to draw. However the two-quadrant nature of the rectifier means that the current and voltage cannot differ in sign, so the result will be a reduced coil current. If a proportional control loop is used to control the coil current then the variation in current will be much less significant.

Simulation results for airgap eccentricity are shown in Figure 6.11 for the basic controller, and Figure 6.12 for the improved controller with the current proportional control loop. Both simulations were run for the full power condition of the turbine, and an airgap variation of 10% of the EMF magnitude at twice the rotor speed was used. Power output from two coils connected to a module was calculated, and the power flow should be constant due to the 90° phase difference between the coils.

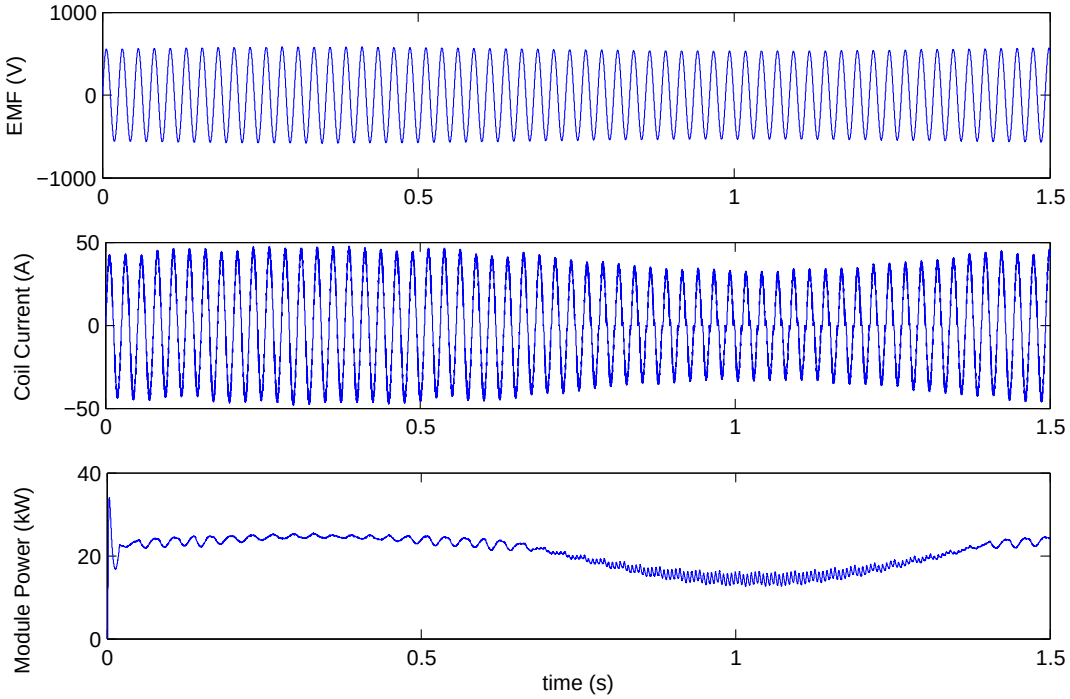


Figure 6.11: Effects of rotor eccentricity using basic controller

The system using the basic controller shows a significant variation in power output of up to 50% of the average, as well as power ripple due to the cusp distortion correction. This is due to the rectifier attempting to draw power at a non-unity power factor. The improved controller shows a smaller variation of around 15%, but this is still significant, so in both cases the magnitude of the generator EMF must be estimated as well as its position.

Much of the variation in power output with the improved controller is due to the variation in EMF as the current variation is small. In order to draw constant power, the coil current demand must be increased when the EMF is low and decreased when it is high.

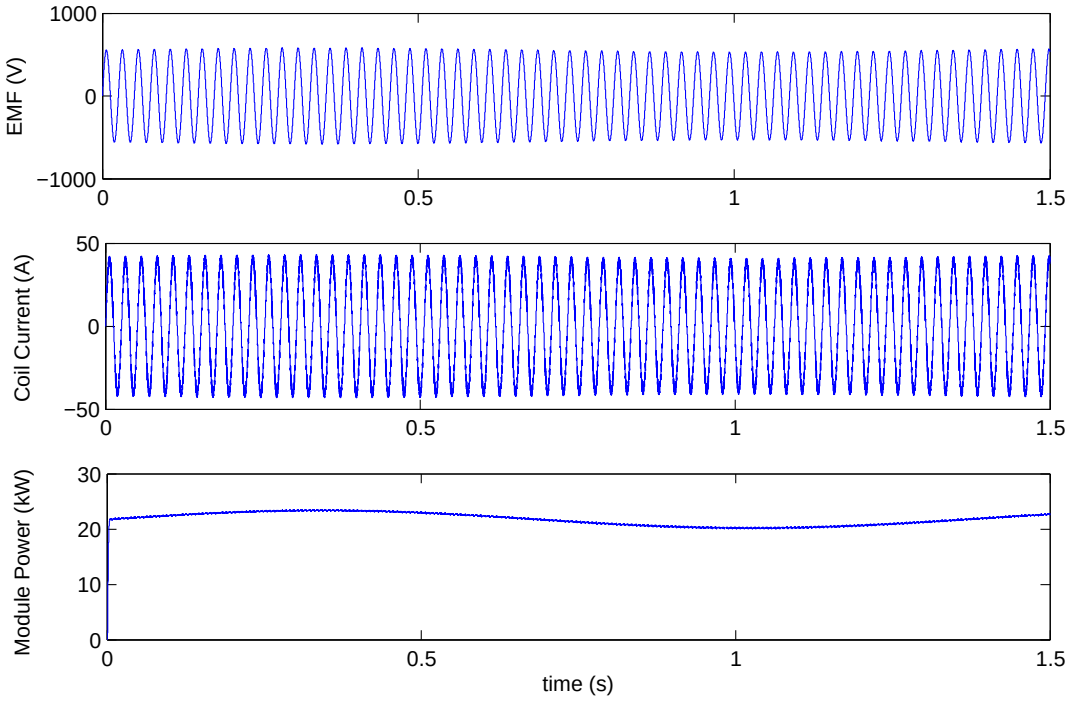


Figure 6.12: Effects of rotor eccentricity using improved controller

6.4 Estimation of Generator EMF

6.4.1 Phaselock Loop for EMF Position Estimation

The generator EMF position can be estimated using an observer system based on a phaselock loop (PLL), which can track the phase of a signal even with a high degree of noise. The structure of a basic phaselock loop is shown in Figure 6.13, and consists of the following components [45]:

- A phase detector, which compares the phase of a periodic input signal to the reference phase θ and produces an error signal e, which is the phase difference between the signals.
- A loop filter, which can be simply a low pass filter in a simple PLL, and which determines the bandwidth of the loop and hence the level of noise immunity. The output of the loop filter is a reference frequency f.
- An integrator, which produces a reference phase θ from the reference frequency. This phase is then fed back to the phase detector.

The loop is said to be 'locked' when the reference frequency f is exactly equal to the frequency of the input signal, and the response of the PLL reaches a steady state.

The phase detector and loop filter will be considered in the context of estimating the position of the generator EMF.

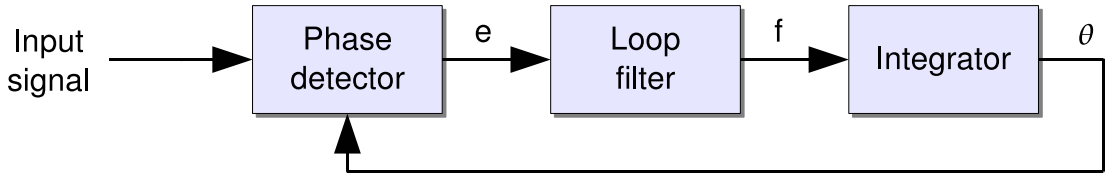


Figure 6.13: Basic phaselock loop structure

6.4.2 Phase Detector

The exact position of the internal generator EMF cannot be measured, but it can be estimated from the applied voltage, the measured coil current, and the knowledge of the coil resistance and inductance, a system used in [46]. This is shown in Figure 6.14 below. Here the feedforward voltage V, which has been applied to the coil terminal, has been calculated based on an estimated angular velocity $\hat{\omega}$, using Equation 6.10, with an estimated EMF $\hat{E}$ given by Equation 6.11. The feedforward voltage is calculated in a rotating reference frame based on the estimated electrical angle $\hat{\theta}$ which differs from the actual electrical angle by an angle ϕ. This results in a coil current I which is different from the desired current.

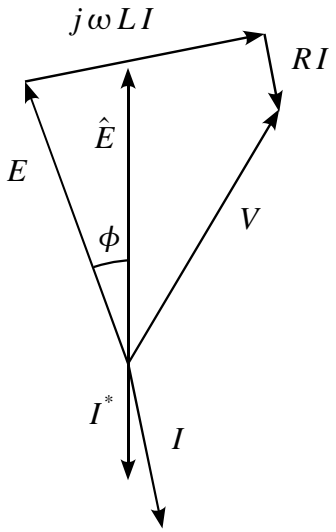


Figure 6.14: Phasor diagram with incorrect EMF estimation

$$\begin{bmatrix} V_d \\ V_q \end{bmatrix} = \begin{bmatrix} \hat{E}_d \\ \hat{E}_q \end{bmatrix} + \begin{bmatrix} R & 0 \\ 0 & R \end{bmatrix} \begin{bmatrix} I_d^* \\ I_q^* \end{bmatrix} + \begin{bmatrix} 0 & -\hat{\omega}L \\ \hat{\omega}L & 0 \end{bmatrix} \begin{bmatrix} I_d^* \\ I_q^* \end{bmatrix} \tag{6.10}$$

$$\begin{bmatrix} \hat{E}_d \\ \hat{E}_q \end{bmatrix} = \begin{bmatrix} 0 \\ k\hat{\omega} \end{bmatrix} \tag{6.11}$$

Equation 6.5 can be rearranged and the desired values replaced by the actual values to give Equation 6.12, which will accurately estimate the position of E so long as the estimated angular velocity $\hat{\omega}$ is accurate. From this the phase error of the EMF reference frame relative to the actual EMF, ϕ can be calculated.

$$\begin{bmatrix} E_d \\ E_q \end{bmatrix} = \begin{bmatrix} V_d \\ V_q \end{bmatrix} - \begin{bmatrix} R & 0 \\ 0 & R \end{bmatrix} \begin{bmatrix} I_d \\ I_q \end{bmatrix} - \begin{bmatrix} 0 & -\hat{\omega}L \\ \hat{\omega}L & 0 \end{bmatrix} \begin{bmatrix} I_d \\ I_q \end{bmatrix} \tag{6.12}$$

The resulting phase detector is shown in Figure 6.15. The coil currents i_1 and i_2 are converted to the rotating estimated EMF reference frame, giving currents I_d and I_q. The previously calculated feedforward voltages V_d and V_q, in the rotating reference frame, are used with the currents I_d and I_q to calculate the EMF estimation error ϕ, which is used to drive the PLL loop filter.

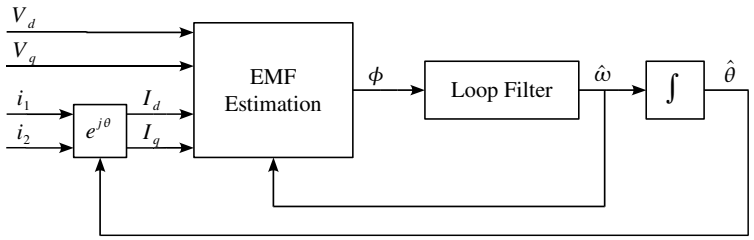


Figure 6.15: Phase detector with EMF estimation

If a proportional controller is used to force the current to follow a reference waveform, then the phasor diagram will be more like Figure 6.16. Here the feedforward voltage V_{ff} is modified by a voltage ΔV from the proportional controller, and the current will be similar to the desired current, depending on the proportional gain. In this case the voltage applied to the coil V will be different from the calculated feedforward voltage V_{ff}, and must be calculated from the duty cycle using Equation 6.3

before being transformed to the rotating estimated EMF reference frame. This phase detector is shown in Figure 6.17.

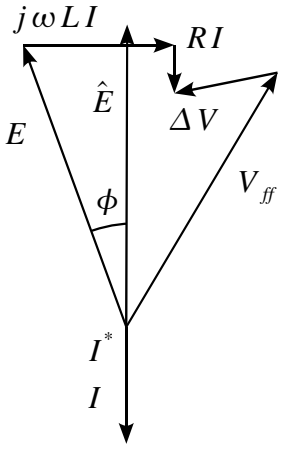


Figure 6.16: Phasor diagram with current proportional controller

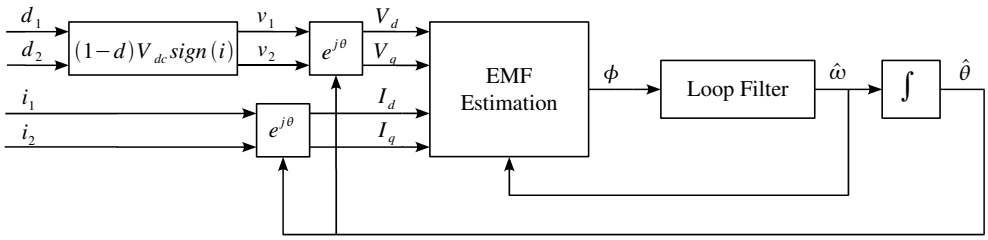


Figure 6.17: Phase detector for current proportional controller system

6.4.3 Loop Filter

The loop filter determines the bandwidth of the PLL, affecting the noise rejection characteristics, so a calculation of the required bandwidth and the system noise is essential. The minimum bandwidth is determined by the turbine rotor dynamics, in that the PLL must be able to track the rotor position faster than the position can vary. At frequencies above the PLL bandwidth, the generator can be regarded as a fixed speed generator, behaving like a stiff spring connected to the synchronous speed. This can lead to resonances in the drive train, as well as high torques and consequently high coil and rectifier currents.

The aerodynamics of the turbine blades means that the rotor dynamics are non-linear, and the rotor time constant will vary depending on the conditions. If it is assumed that the turbine will be controlled such that the generator torque T

is varied proportionally to the rotor speed Ω squared, i.e. $T = K\Omega^2$, then the variation in speed $\Delta\Omega$ about a speed Ω_0 due to a change in wind speed ΔU is given by Equation 6.13 [21].

$$\Delta\Omega = \frac{(\partial T/\partial U)_0 \Delta U}{Is + B + 2K\Omega_0 - (\partial T/\partial\Omega)_0} \tag{6.13}$$

In this equation, I is the rotor moment of inertia and B is the drivetrain viscous friction. B is likely to be small in a direct drive turbine. The time constant of the resulting system is given in Equation 6.14. Using this equation the variation of rotor time constant can be found in the power tracking part of the turbine operating region, and this is shown in Figure 6.18. The turbine rotor is more responsive at higher wind speed as the time constant depends on the variation of aerodynamic torque with rotor speed $\partial T/\partial\Omega$, which will be greater at higher wind speeds.

$$\tau = \frac{I}{B + 2K\Omega_0 - (\partial T/\partial\Omega)_0} \tag{6.14}$$

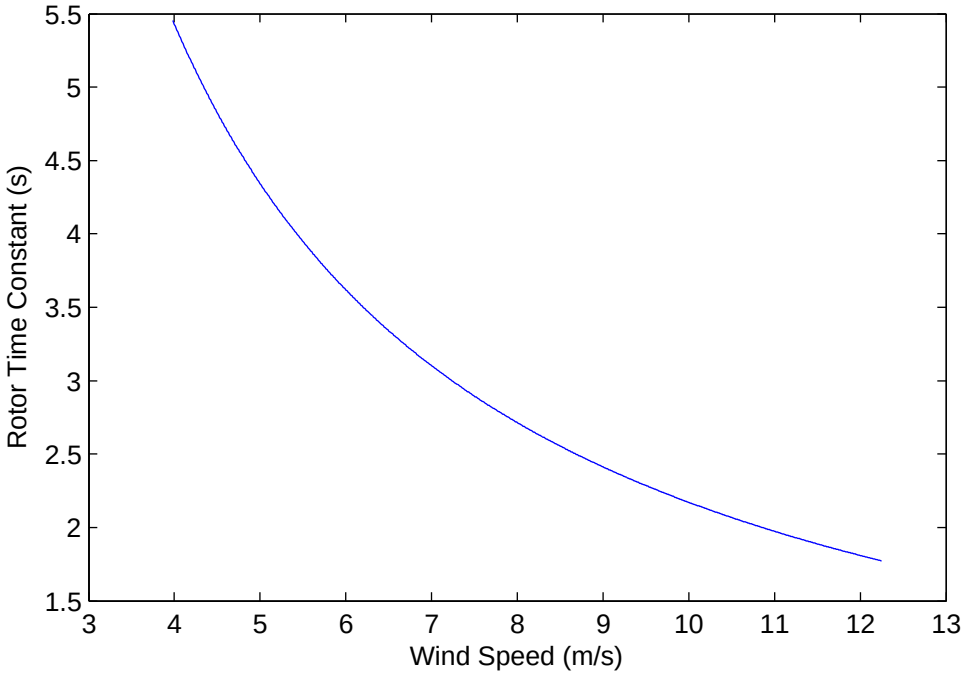


Figure 6.18: Variation of rotor time constant with wind speed

Another important minimum frequency is the resonant frequency of the generator, estimated to be around 3Hz by the designers of the generator considered here. If the PLL bandwidth is similar to this frequency then unwanted interactions could occur while a higher bandwidth could allow the oscillations to be damped.

The phase detector should not produce any interference if the input signals are sinusoidal and have equal magnitude in the two coils (phases). Unfortunately the distortion around the current zero crossing point causes spikes in the output of the reference frame conversions. This occurs twice in a cycle, and with two phases at 90° separation this leads to spikes at four times the EMF frequency.

In chapter 3 it was determined that the turbine speed could vary between 7rpm and 22rpm, and with the proposed generator of 216 magnetic poles, the frequency will vary between 12.6Hz and 39.6Hz. This will lead to interference between 50.4Hz and 158.4Hz. Unbalance in the outputs of the two coils could lead to ripple at twice the EMF frequency, but it is judged that this ripple is likely to be small.

In order to avoid a steady state phase error at constant turbine speed, which would lead to an incorrect coil current, the loop filter should include a proportional-integral (PI) controller. To minimise the effects of the interference from the phase detector, the bandwidth will be kept low at around 5Hz, which will still allow the controller to track effects of the generator resonant frequency.

The root locus of the PLL system is shown in Figure 6.19. The two cascaded integrators in the loop cause the locus to form a circle around the zero from the PI controller. It is desirable for the closed loop poles not to be to the left of the controller zero, so this zero is placed such that the closed loop poles are above and below it, achieving the desired natural frequency of 31.4rads/s and a damping ratio of 0.707. This is achieved at a proportional gain of 45.

The controller $C(s)$, including the second integrator, is given by Equation 6.15. Using the standard form of a PI controller, given by Equation 6.16 and equating the constants, the proportional gain K_P is 45 and the integral gain K_I is 1000. The response of the PLL system to a step in phase angle is given in Figure 6.20. The response shows slightly greater peak overshoot than expected, this is due to the close proximity of the PI controller zero to the closed loop poles.

$$C(s) = \frac{45(s + 22.21)}{s}\frac{1}{s} \tag{6.15}$$

$$C(s) = \frac{K_P(s + K_I/K_P)}{s} \tag{6.16}$$

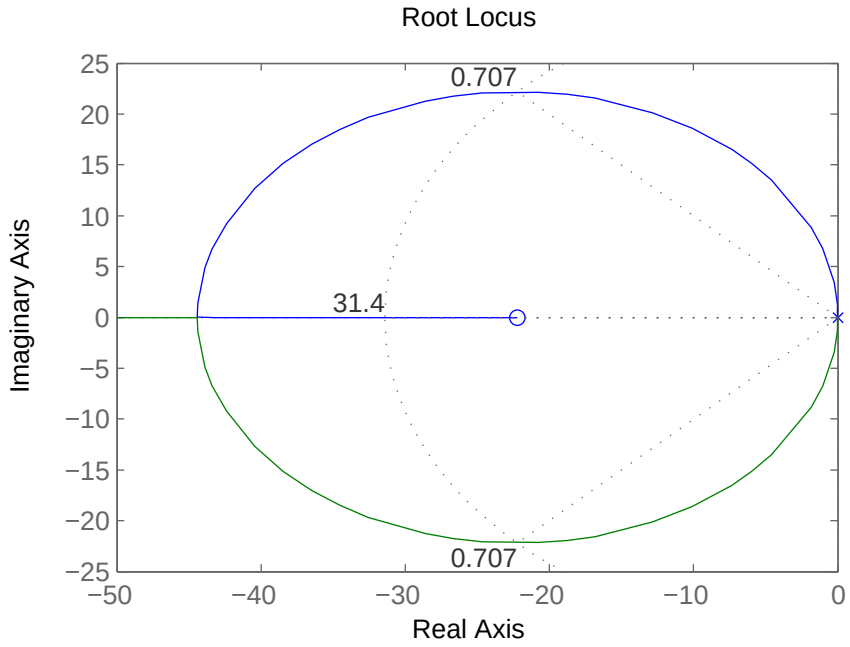


Figure 6.19: Root locus of PLL system

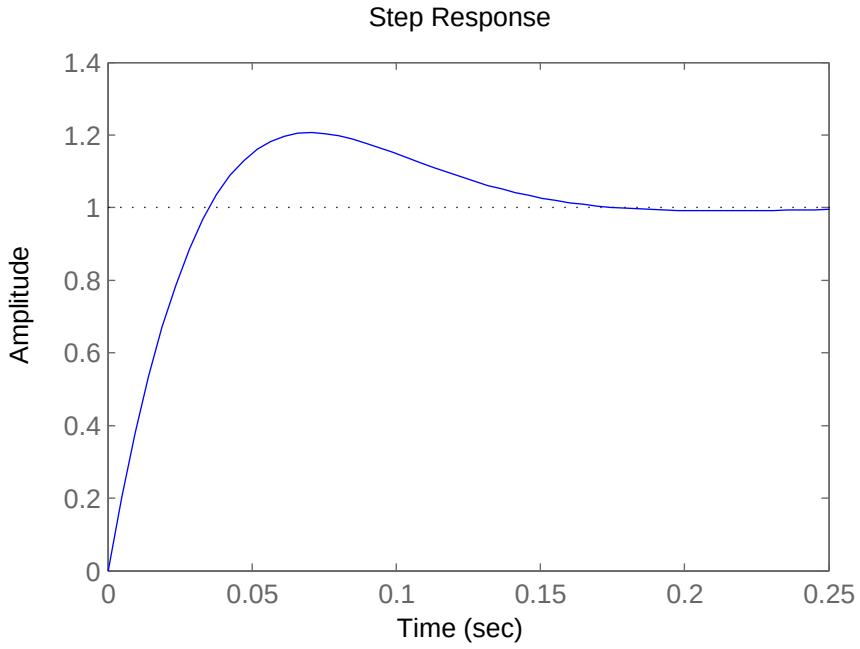


Figure 6.20: Response of PLL phase angle estimation to step in phase angle

6.4.4 Simulation of EMF Position Tracking

Simulation of the rectifier current control is identical to that in Section 6.3.1, using two rectifiers connected to two coils with 90° phase separation. The estimation of the EMF phase is provided by the estimator described previously, which is implemented as a discrete system sampling at 8kHz.

The EMF estimator is combined with the current controller to produce a structure shown in Figure 6.21. The EMF estimation loop was formed using discrete-time integrators – as the loop bandwidth is significantly lower than the sampling frequency, the behaviour should match that of the continuous-time loop formulated in the previous section.

Steady State Tracking

Simulation was carried out for the maximum and minimum power scenarios detailed previously, using a constant generator speed. The machine EMF and voltage applied to the coils were recorded, along with coil current, EMF estimation in the rotating reference frame and estimated generator speed. The results are shown in Figure 6.22 and 6.23.

Distortion around the coil current zero-crossing regions can clearly be seen in the estimated EMF and generator speed for the maximum power condition. This is due to the discontinuities in the applied voltage around the zero crossing point and distortion in the current. This effect is not visible in the minimum power waveforms as the delay between the EMF and applied voltage is much smaller. Instead a different distortion appears, due to the current entering the discontinuous conduction mode.

The spikes in the estimated generator speed due to a current zero-crossing in one coil lead to small spikes in the voltage applied to the other coil, which leads to a small amount of distortion in the coil current. This could be solved by filtering the estimated generator speed, when used for feedforward calculation. This would not affect the dynamics of EMF estimation as the feedforward system is not a part of the phaselock-loop.

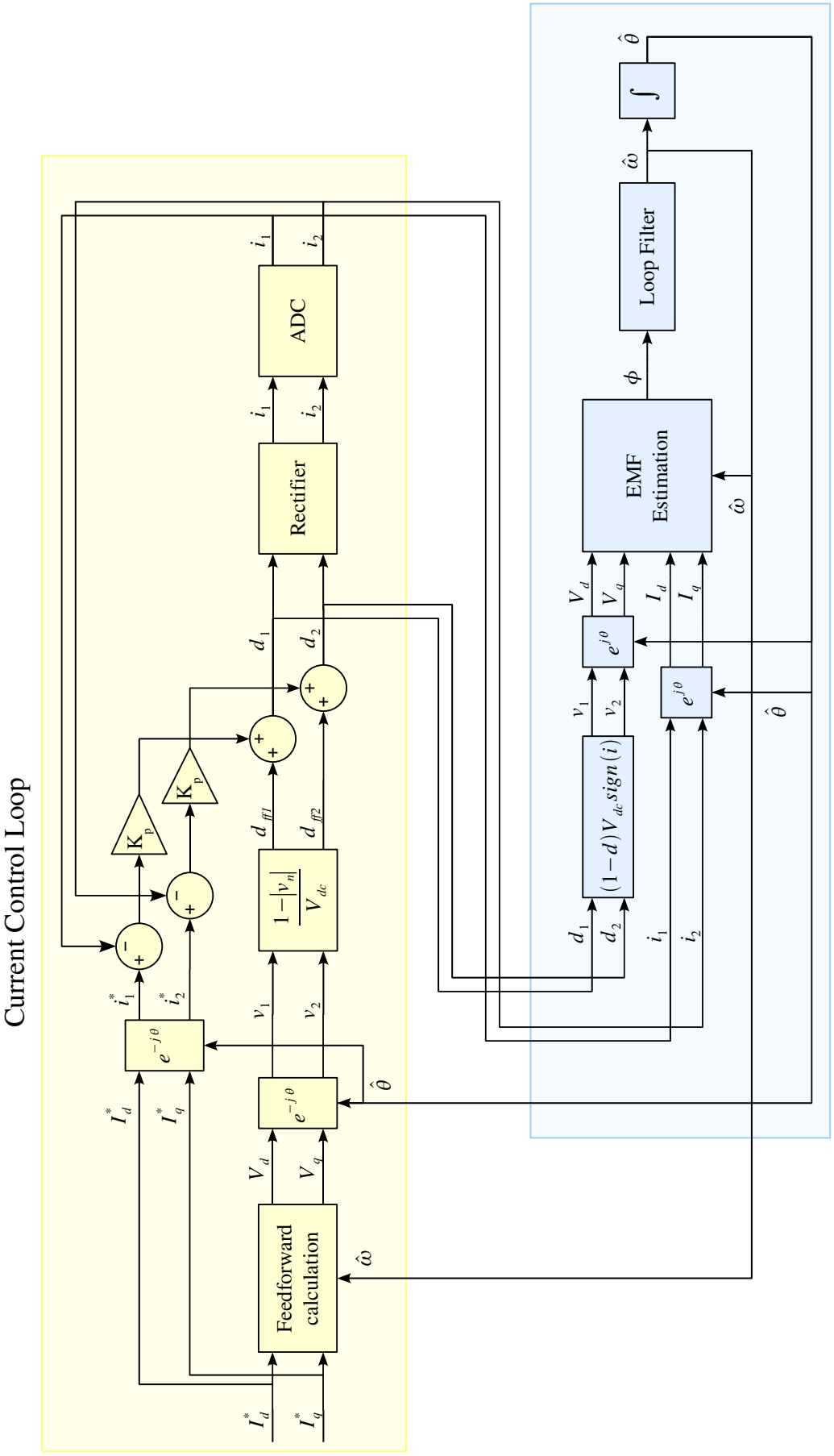


Figure 6.21: Simulated rectifier overall control structure

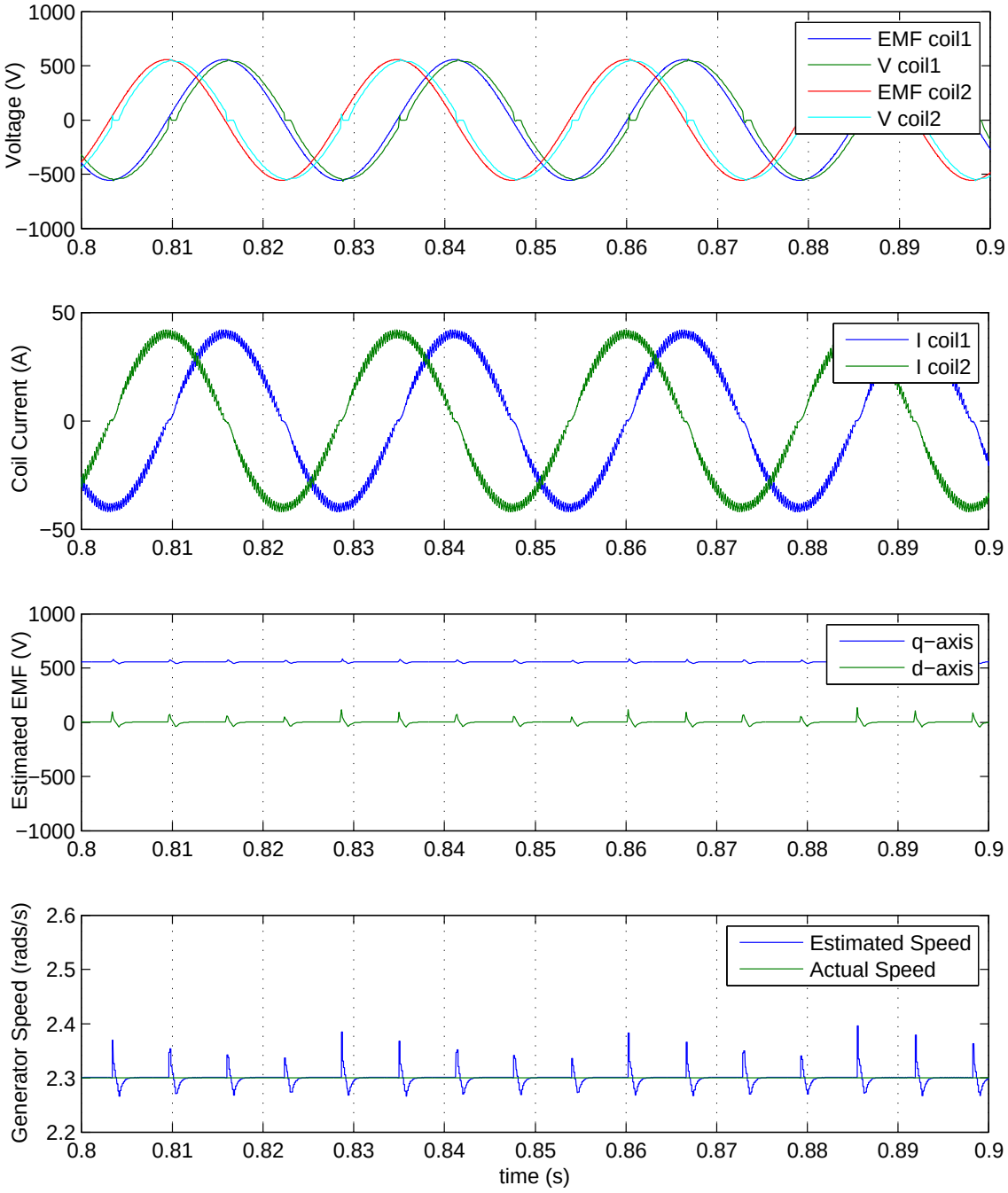


Figure 6.22: Steady state EMF tracking at maximum power conditions

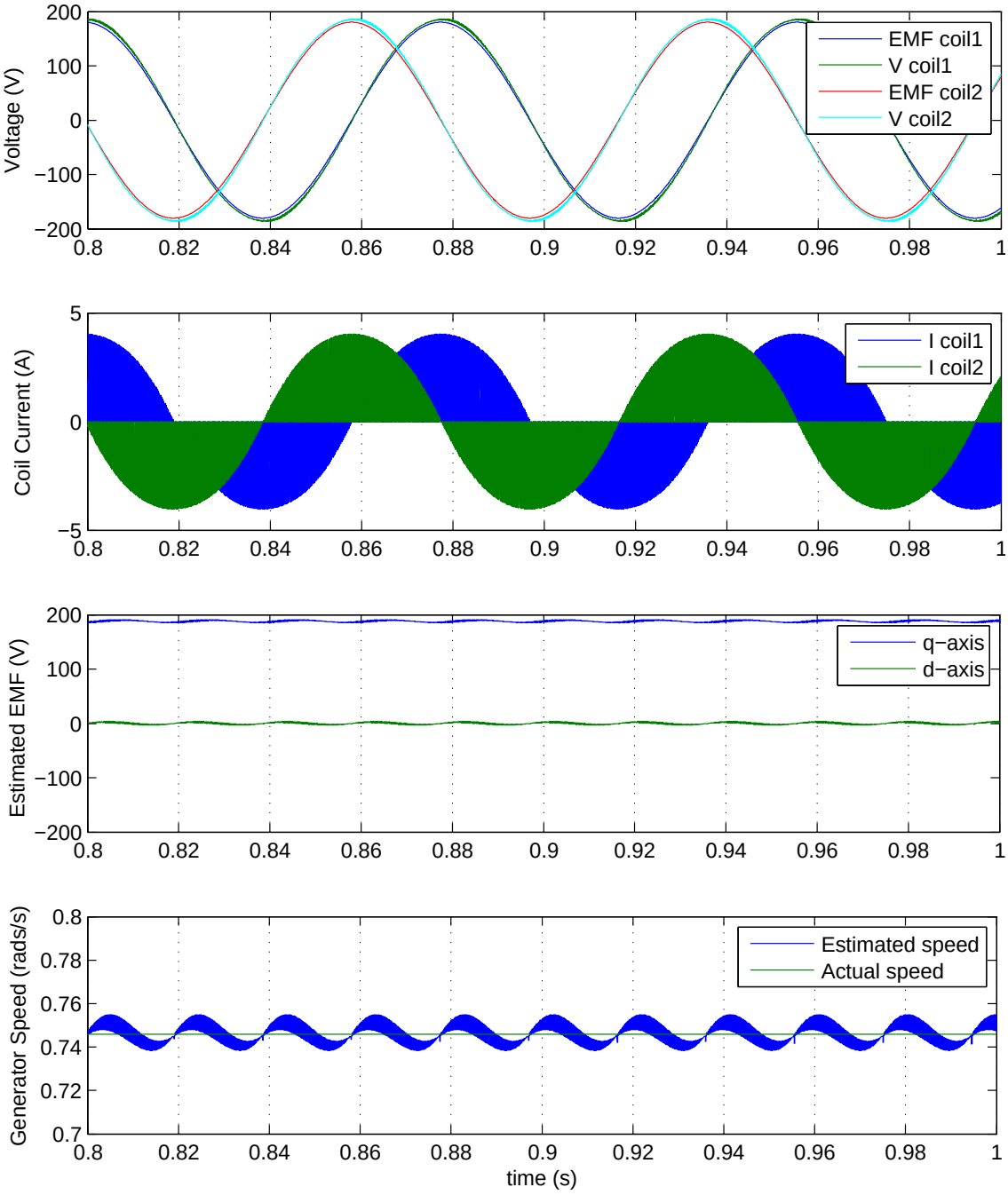


Figure 6.23: Steady state EMF tracking at minimum power conditions

Step Response

Loop dynamics were tested by starting the simulation with the initial estimated generator speed at a slightly lower value than the actual value, in effect applying a step in generator speed. The response of the phaselock-loop is shown in Figures 6.24 and 6.25, and show a similar response to the predicted step response shown in Figure 6.20, with the minimum power condition giving a slightly slower response.

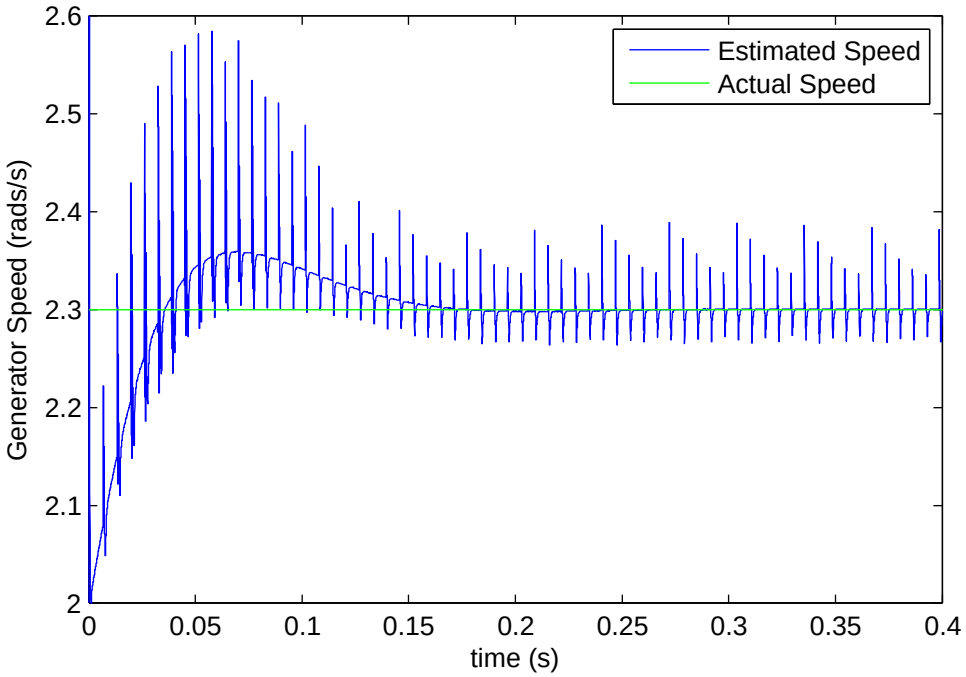


Figure 6.24: EMF tracking step response at maximum power conditions

6.4.5 Airgap Eccentricity and EMF Magnitude Calculation

Airgap eccentricity will cause the EMF magnitude to vary, while the angle remains the same, so it will not affect the operation of the phaselock-loop. It would be useful to calculate the EMF magnitude rather than simply assuming it is proportional to the generator speed. The EMF magnitude can be calculated from the values found in Equation 6.12, and this value can be filtered to reduce noise.

Once again the phase detector will produce spikes at between 50.4Hz and 158.4Hz, depending on the machine speed. The minimum bandwidth of the filter is the maximum frequency of the variation of the EMF – with a maximum generator speed of 22rpm, a second order eccentricity will give a variation frequency of 0.73Hz. A 5Hz

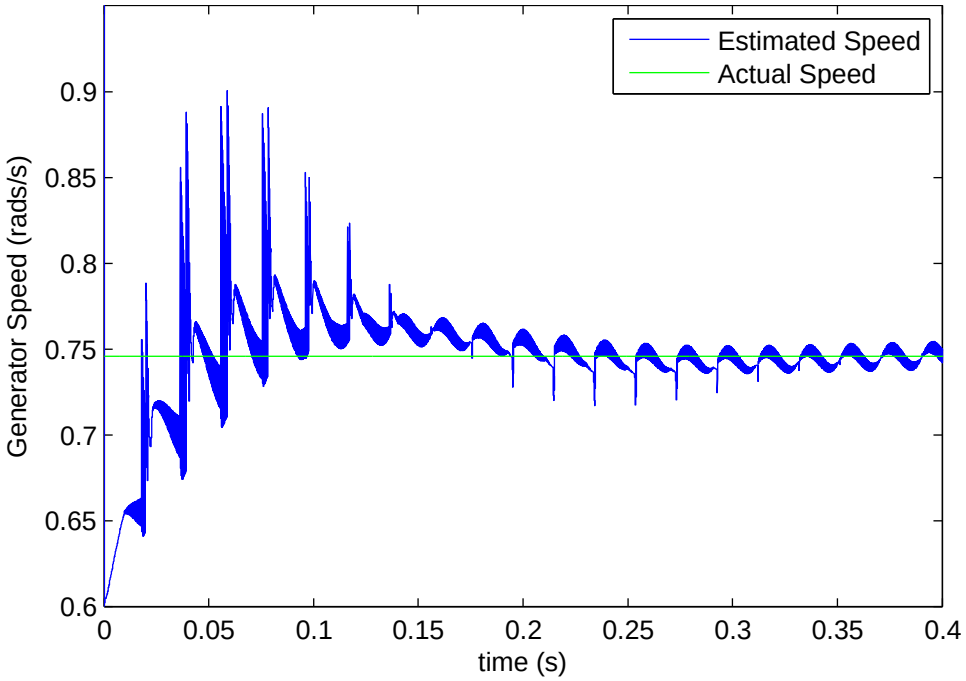


Figure 6.25: EMF tracking step response at minimum power conditions

second order butterworth filter will provide ample bandwidth while still providing at least 40dB attenuation of the phase detector spikes.

This system was simulated as in Section 6.3.2, using the EMF position estimation loop and the magnitude estimation described above. Results are shown in Figure 6.26, and it can be seen that the estimated EMF magnitude tracks the actual value, although there is a delay due to the filter. Coil current magnitude remains constant at all values of EMF, as required.

The EMF magnitude estimator has the further advantage of eliminating the distortions in the voltage applied to the coil around the current zero-crossing of the other coil. Power output still fluctuates as the EMF is varying. This could be solved by having the rectifier output current demand as the controlled parameter and calculating the coil current demand from this.

6.5 Inverter Control

Although the inverter control algorithm has been developed with other researchers, part of it must be implemented in the module controllers, so the theory will be described in this chapter. The inverter control algorithm is described fully in [47].

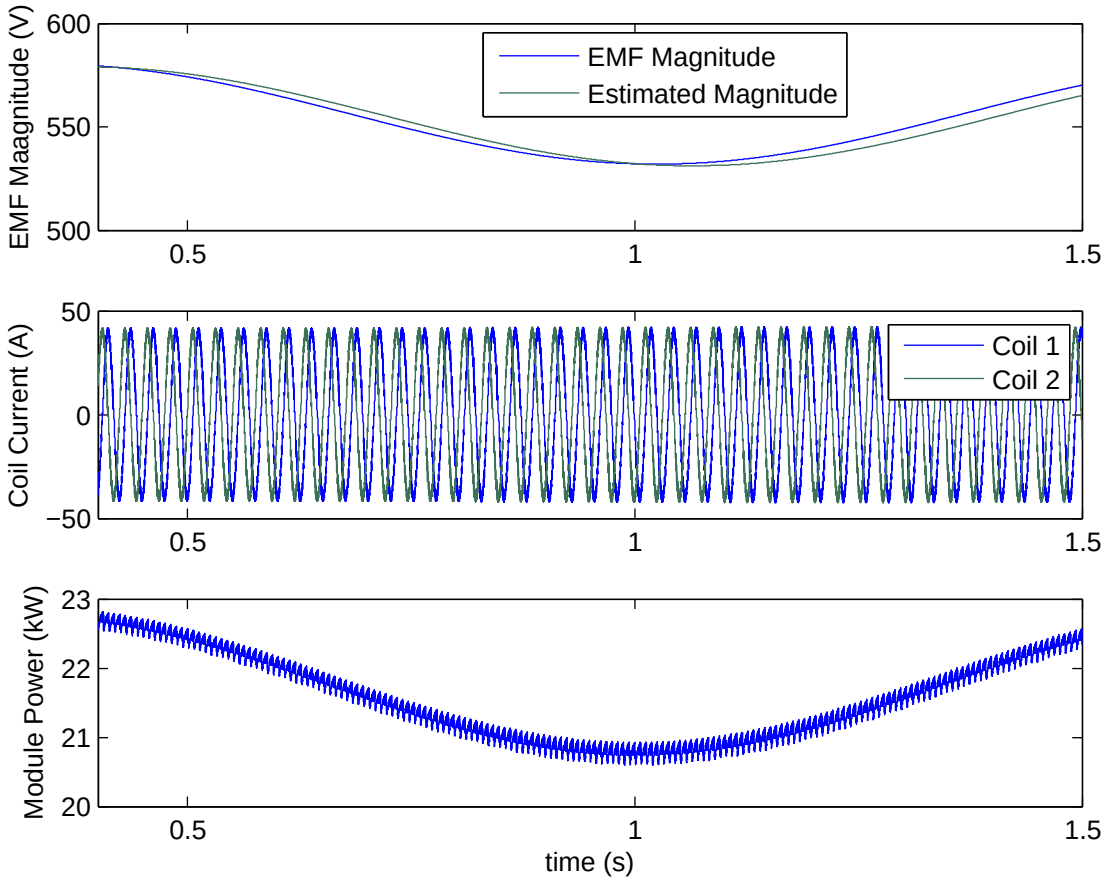


Figure 6.26: Estimation of EMF magnitude with rotor eccentricity

Compared with most multilevel inverter control algorithms, the DC-link voltages of the different levels do not need to be regulated from the inverter side, so control is simplified significantly. Power sharing between levels does not need to be exactly equal, but in order to maximise the machine utilisation the power from each inverter module should be as equal as possible. Modules could be built with different power capabilities, but in order to obtain the desired benefits of a modular system all the modules would need to be identical.

Another problem is that the single phase output of the inverter will cause a ripple in the module DC-link voltage at twice the grid frequency, and this will cause a distortion in the output voltage waveform. This distortion can be reduced by increasing the DC-link capacitance, but this is expensive and it would be far cheaper to adapt the inverter switching to compensate for the distortion.

6.5.1 Basic Inverter Switching

Each inverter module, with a DC-link voltage of V_{dc}, can produce three possible output voltages: $0V$, $+V_{dc}$ and $-V_{dc}$. As the modules are cascaded, the total output voltage is the sum of the individual module output voltages. By switching the modules in an appropriate pattern a sinusoidal output voltage can be synthesised [27], this is shown in Figure 6.27 for a 5-module, 11-level converter.

The conventional switching strategy has the disadvantage that each of the modules has a different duty cycle, so power is not equally shared. The half cycle switching scheme is shown in Figure 6.28a, in which all the modules are switched for an equal time, resulting in greatly improved power sharing.

If the inverter is not operating at unity power factor then power sharing between modules will become less equal. This problem can be rectified by using the asymmetrical half cycle switching scheme, shown in Figure 6.28b and proposed in [47].

The switching schemes were simulated for an 11-level converter, for unity power factor output as well as production and consumption of reactive power. Some results are shown in Figures 6.29a and 6.29b. The half cycle switching schemes both show good power sharing with unity power factor output, with the asymmetrical scheme also showing good power sharing with reactive power production. A simulated inverter voltage waveform is shown in Figure 6.30.

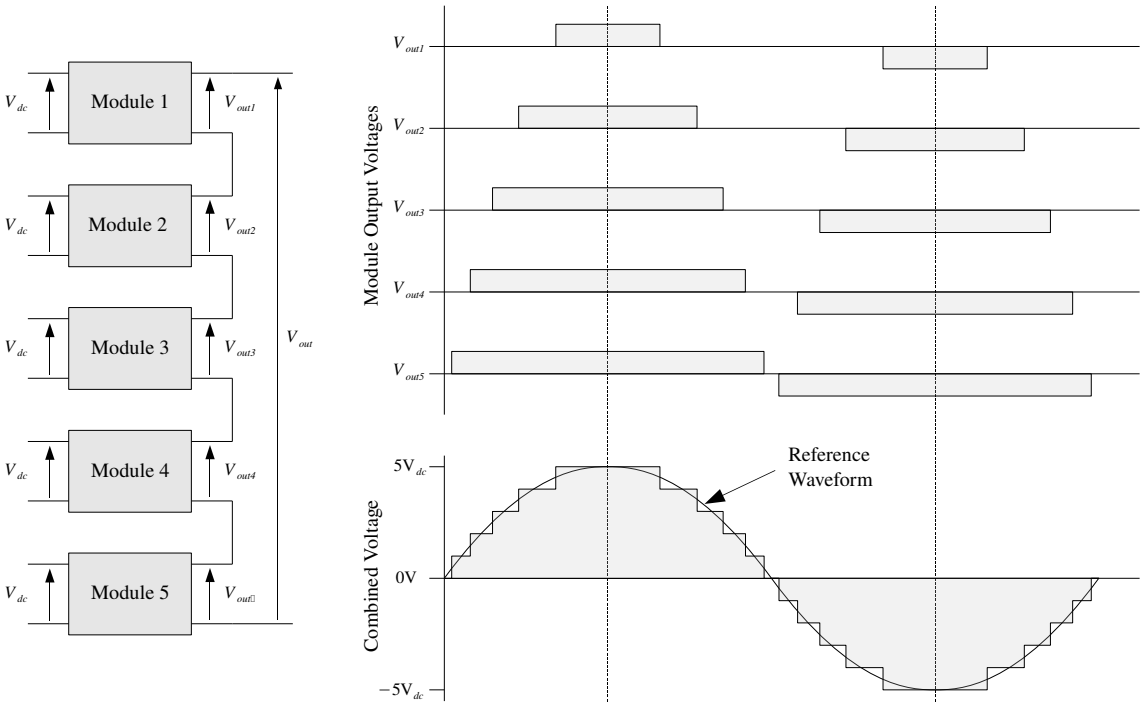


Figure 6.27: Conventional Inverter Switching

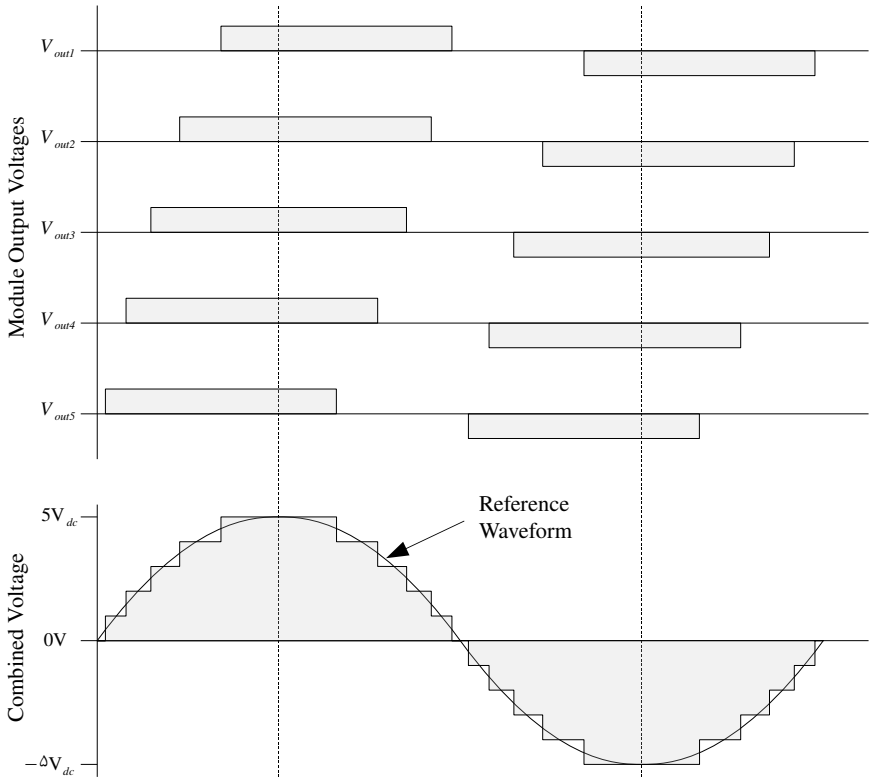
6.5.2 Harmonic Compensation Switching

As mentioned previously, the ripple in the DC-link voltage from the single phase inverter will cause distortion in the inverter voltage waveform. This distortion will lead to a distorted current, particularly in the third harmonic of the grid frequency. An example of this distortion, taken from simulations carried , is shown in Figure 6.31. This is mostly a problem when operating at high power levels, where the DC-link voltage ripple will be significant.

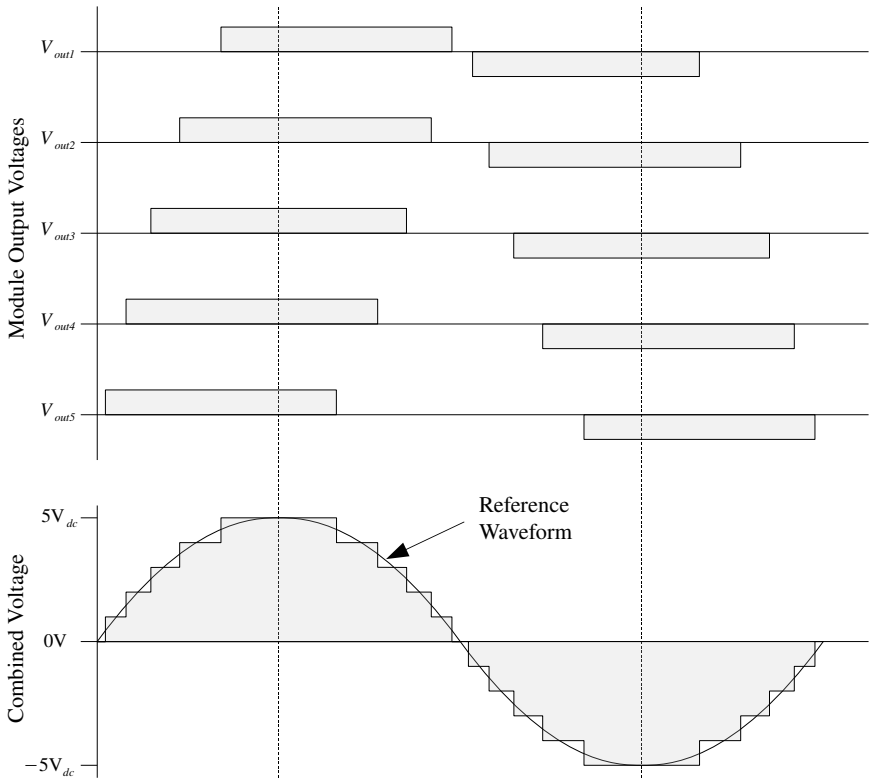
A separate active filter could be used to reduce the voltage distortion, but this would increase the cost of the system, and provide a single point of failure, eliminating the benefits of the fault tolerant system. Alternatively one of the modules could act as an active filter, however this would increase the switching stresses on that module, increasing the probability of failure.

The solution proposed in [47] is to distribute the active filtering between all modules, thus equally distributing the switching stress. A transducer will measure the voltage output of the inverter, which will be compared to the desired voltage waveform and an error signal produced using some form of controller. This error signal will be sent to all the modules.

Each module will have it's own PWM carrier, and the error signal will control

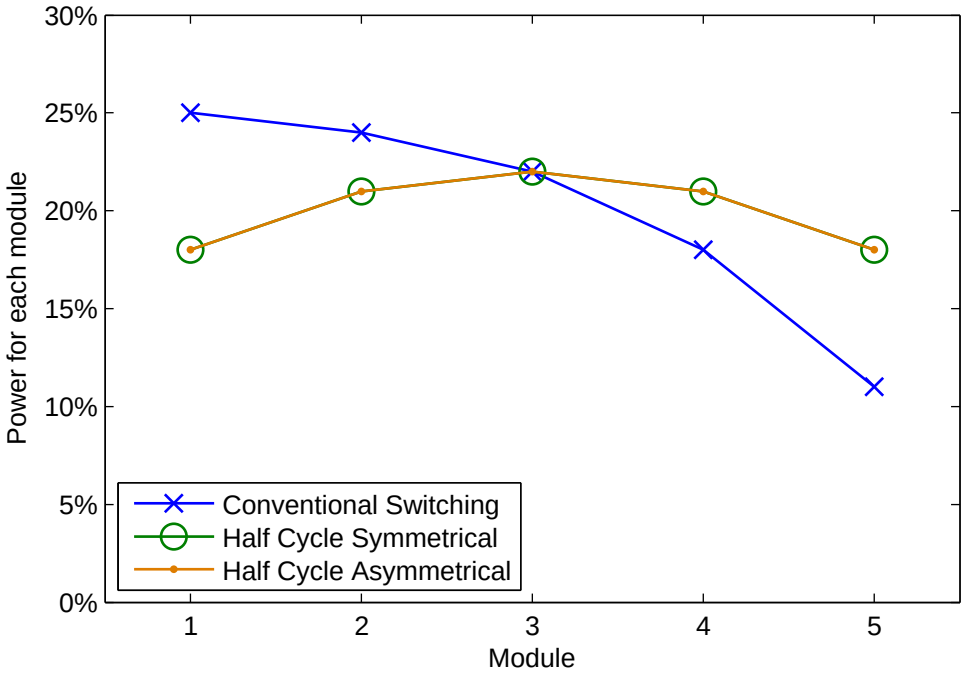


(a) Half cycle symmetrical switching

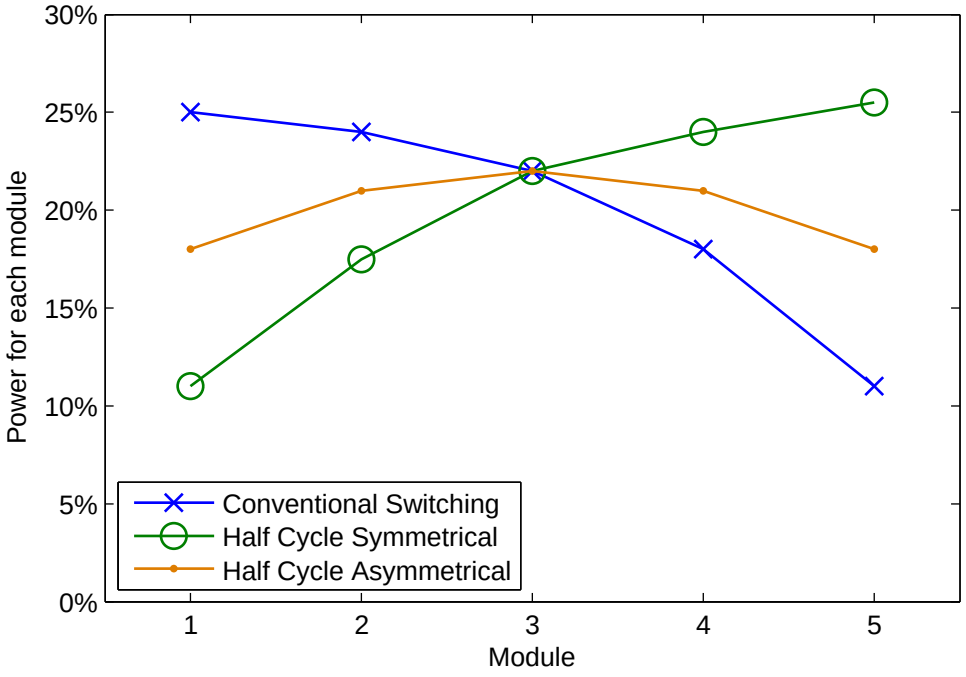


(b) Half cycle asymmetrical switching

Figure 6.28: 11-level inverter improved power sharing switching schemes



(a) Unity power factor operation



(b) Reactive power source, power factor 0.81

Figure 6.29: 11-level inverter power sharing

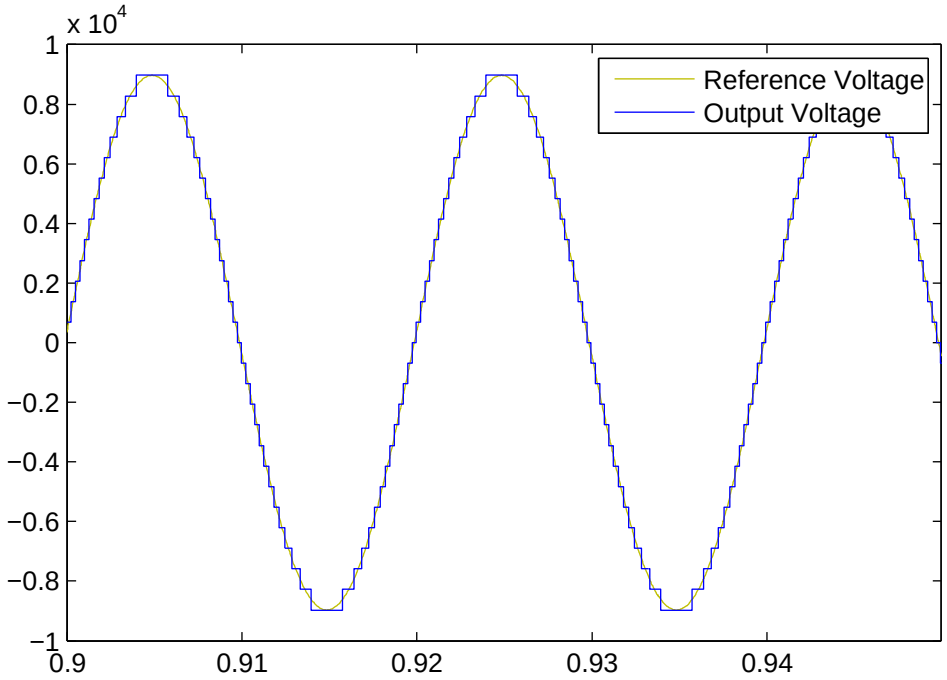


Figure 6.30: Typical voltage waveform produced by the inverter

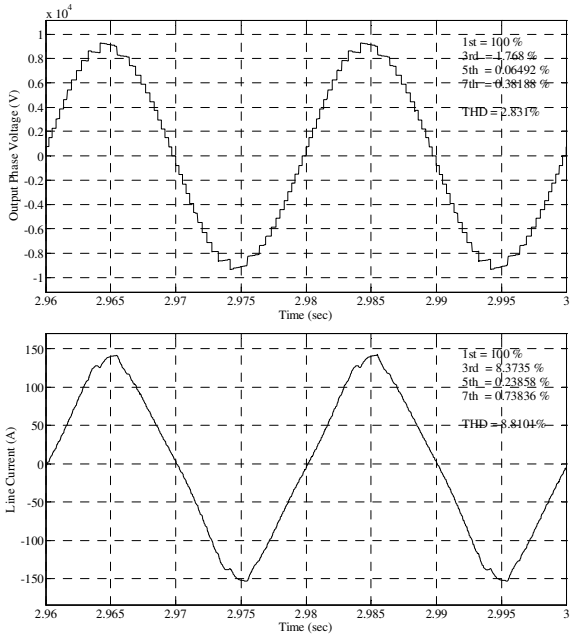


Figure 6.31: Distorted inverter voltage and current due to DC-link ripple

the PWM duty cycle. The PWM signal will then be combined with the fundamental signal described previously, to produce the switching signal for the inverter, this is shown in Figure 6.32. The PWM signal is produced in the normal way, and simply added to the fundamental signal, where both signals have the same sign the PWM pulse will be ignored.

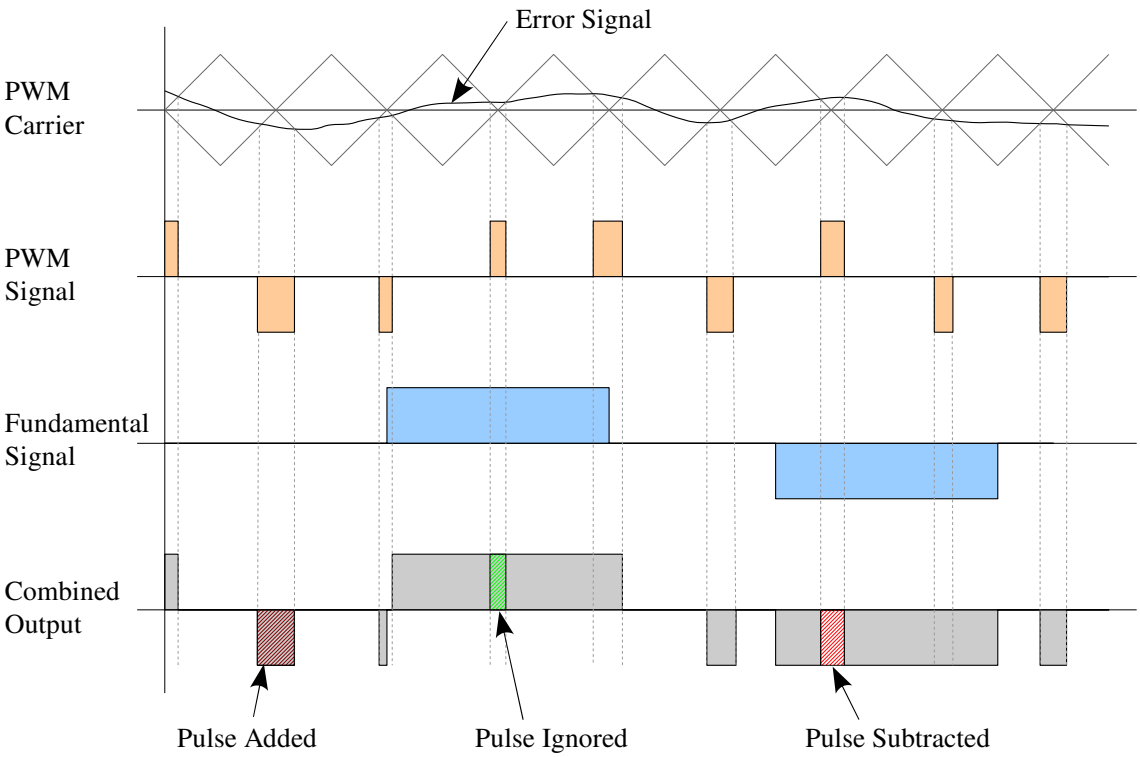


Figure 6.32: Method of synthesising the inverter output signals

The PWM carriers in all the modules are synchronised to the fundamental output, i.e. to the grid frequency, but are phase shifted relative to each other by $\frac{n}{N}T_{sw}$, where n is the module number, N is the total number of modules and T_{sw} is the time period of the PWM carrier. The result of this is that the apparent frequency of the overall PWM signal will be N times higher than the switching frequency of the individual modules, which can be very low. In this way switching losses in each module are kept to a minimum.

An example of the resulting voltage waveform is shown in Figure 6.33, where a module PWM frequency of 400Hz is used. Distortion of the voltage and current waveforms is significantly lower than the equivalent without the active filter, shown in Figure 6.31.

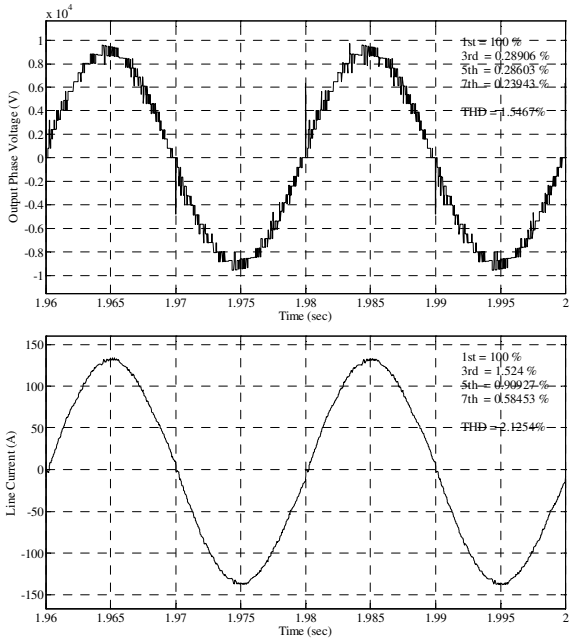


Figure 6.33: Inverter voltage corrected by distributed active filtering

6.6 DC-Link Voltage Control

In chapter 4 the size of the DC-link capacitor bank was calculated to be 1667μF for the systems using a boost rectifier. The DC-link voltage controller must set the rectifier current demand to achieve the desired voltage, determined by the inverter reactive power demand.

In this system the current drawn by the inverter is likely to change only very slowly, so in this respect the frequency response of the DC-link voltage controller does not need to be fast. However in the event of a module failure, the voltage of the remaining modules needs to be quickly increased to compensate for the missing module, so a reasonably fast controller is required.

6.6.1 Modelling the DC-Link

The DC-link model is shown in Figure 6.34. The two-phase input to the modules gives a constant power into the DC-link capacitor, giving a constant current i_r. The inverter output draws a current i_i, which will pulsate at the twice the grid frequency, causing a second harmonic ripple in the DC-link voltage. The asymmetrical inverter switching scheme will also introduce a voltage ripple at the grid frequency.

The voltage controller should, as much as possible, ignore these voltage ripples,

otherwise it will cause a ripple in the rectifier current and hence vibrations in the machine.

The effect of discontinuous conduction on the rectifier control algorithm is to impose a minimum coil current – attempts to draw a smaller current will have no effect. This current is around 1.2A rms at the cut-in speed of the generator. This is fine in steady state operation, but a lower current may be required for controlling the DC-link voltage. To allow a lower current into the DC-link, the excess current is absorbed by a braking resistor, which is activated when the rectifier current demand is below the minimum value.

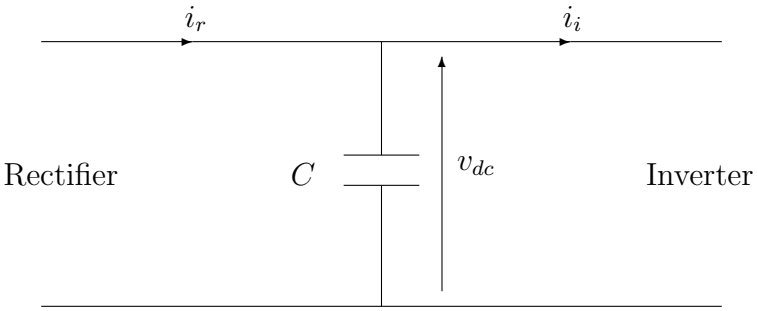


Figure 6.34: DC-Link Model

$$v_{dc} = \frac{1}{C}\int (i_r - i_i)dt \tag{6.17}$$

$$i_r = \frac{2I_c^* E}{v_{dc}} \tag{6.18}$$

6.6.2 Controller Structure

The controller structure is shown in Figure 6.35. The measured DC-link voltage is filtered to remove the ripple due to the inverter, and this is used in a PI controller, which produces a coil current demand for the rectifier.

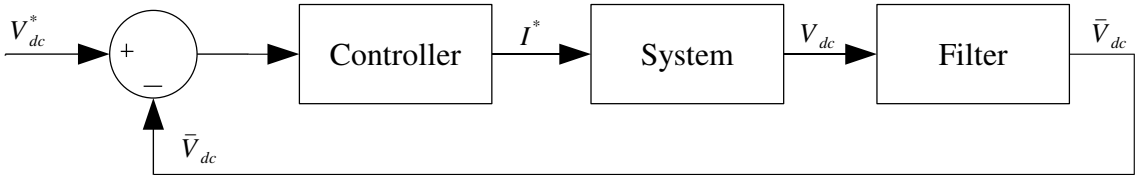


Figure 6.35: DC-Link voltage controller structure

The ripple in the DC-link voltage measurement, due to the inverter, can be filtered using a moving average filter. A 20-step moving average at 1kHz sampling frequency will remove the grid frequency ripple and all higher harmonics, so long as the grid frequency does not vary significantly from 50Hz. This frequency response is shown in Figure 6.36.

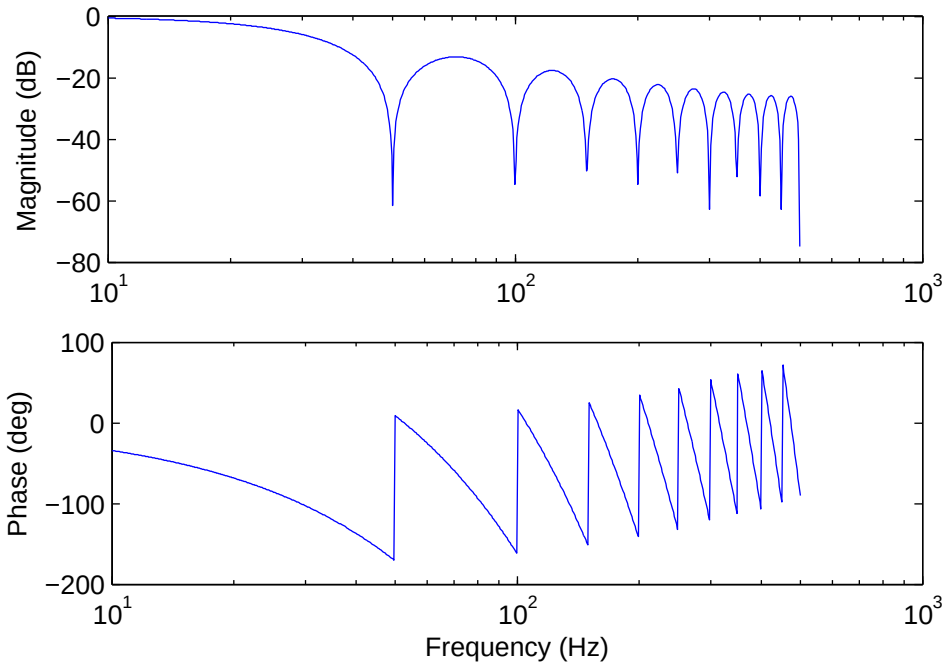


Figure 6.36: Frequency response for 20-step averaging filter

Proportional and integral gains were chosen to give an acceptable response to a step change in voltage demand, at different turbine operating conditions. These conditions are given in Table 6.1. A proportional gain of 0.2 and integral gain of 2.5 were found to give the best results over the range of conditions.

Wind Speed (m/s)	Turbine Speed (rads/s)	RMS Line Current (A)
3	0.75	0.62
6	1.13	5.38
9	1.69	18.2
12	2.30	45.8

Table 6.1: Turbine operating conditions

6.6.3 Simulation of DC-Link Voltage Control

Simulation was carried out using the rectifier model previously developed, with the addition of a simulation of the DC-link voltage. Current into the inverter, i_i, was modelled as a a sinusoidal signal multiplied by a signal representing the switching function of one of the inverter modules, as shown in Figure 6.37. The fifth module in the sequence was chosen for the switching signal as it is has some asymmetry in the switching signal but not severely so.

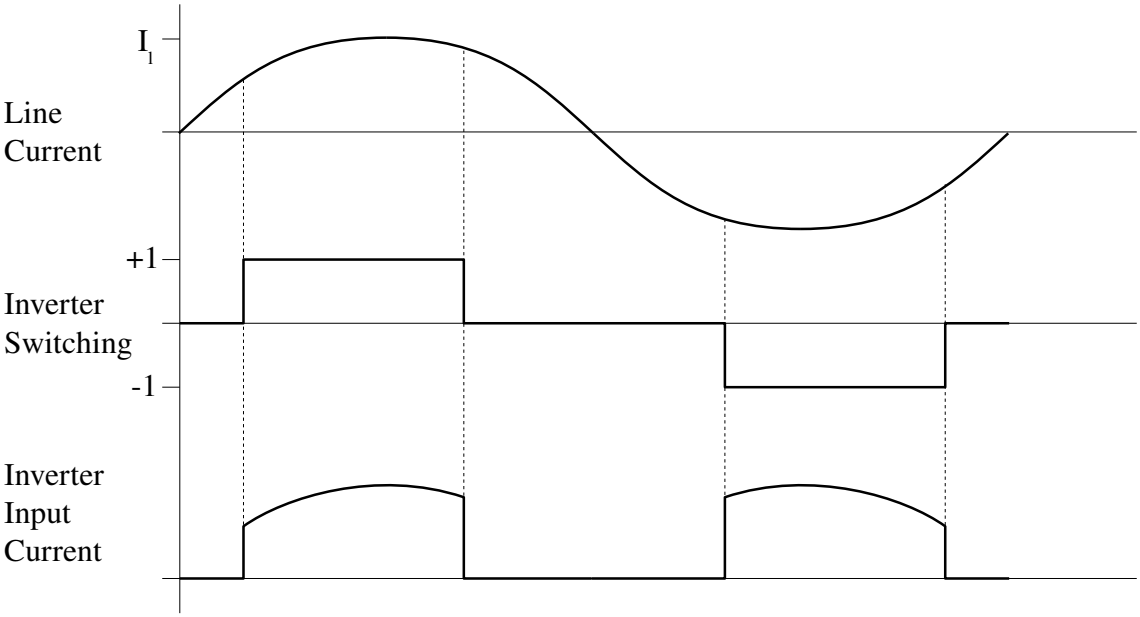


Figure 6.37: Emulation of inverter current

Steady state control of the DC-link voltage is shown in Figure 6.38, for the turbine maximum power condition. The filter is shown to effectively remove the ripple from the measured DC-link voltage signal, so the current demand does not vary significantly.

The system was simulated with a step change in DC-link voltage demand from 690V to 750V, equivalent to the required change if one module is lost. The resulting response is shown in Figure 6.39 for the different wind speed operating conditions listed in Table 6.1. It is clear that the operating conditions have a significant effect on the response of the system, with the controller parameters having to be chosen to achieve a good response in all conditions.

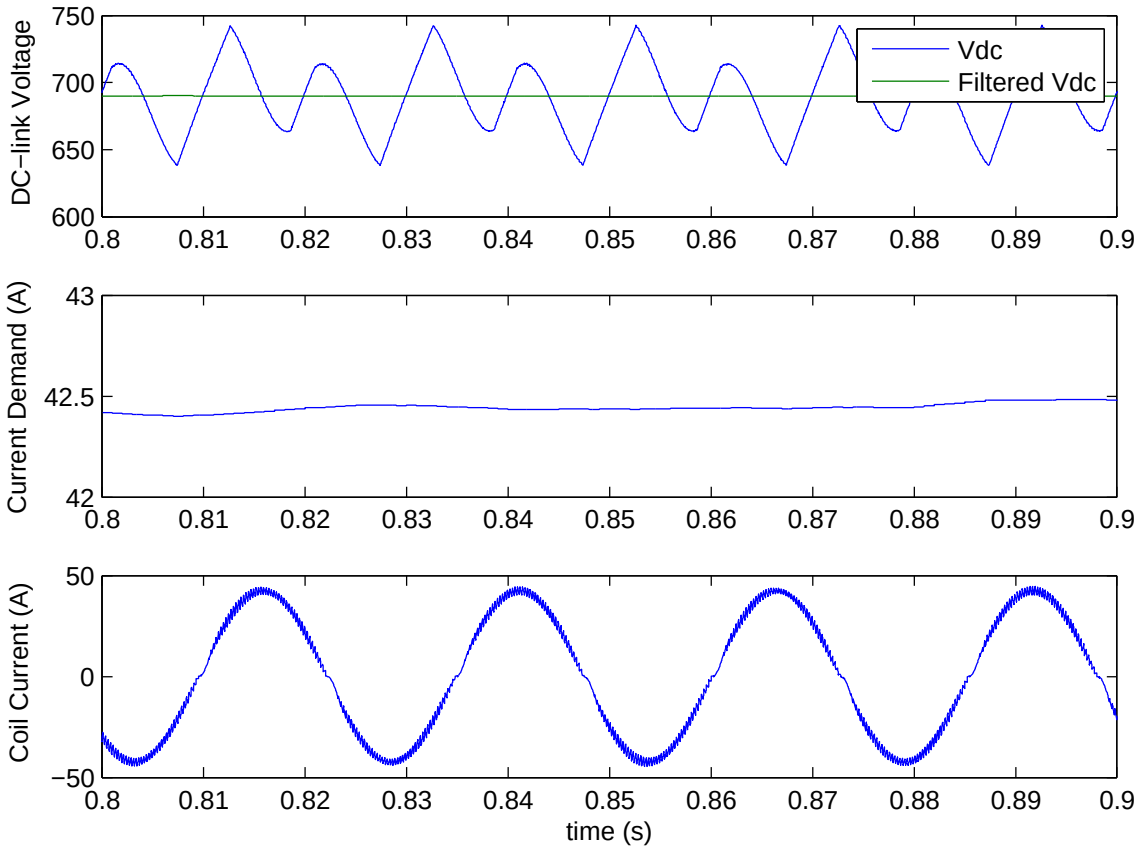


Figure 6.38: DC-Link voltage control in the steady state

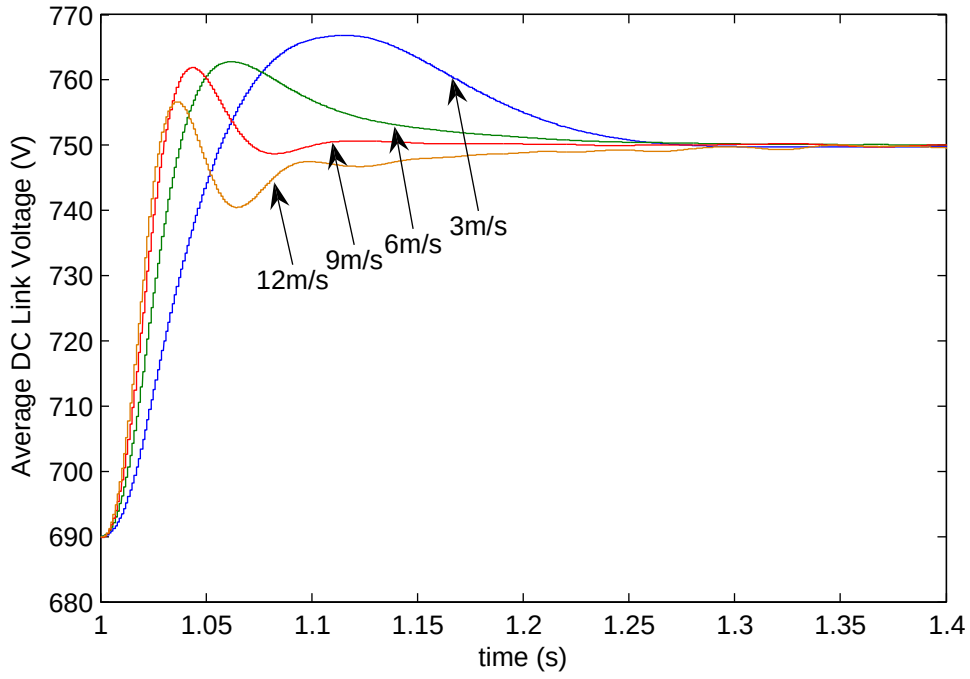


Figure 6.39: Response of DC-Link voltage control to step change in voltage demand

6.6.4 Airgap Eccentricity Considerations

In Section 6.4.5 the rectifier EMF observer was adapted to allow the EMF magnitude to be tracked, meaning that the coil current could be kept constant. However in order to maintain a constant power output the current must be varied to compensate for the variations in EMF.

This can be achieved by the DC-link voltage controller, which will vary the coil demand to keep the DC-link voltage constant with a varying EMF. This requires the bandwidth of the controller to be greater than the frequency of the EMF variation. Simulation of the system with the second order eccentricity as used in previous sections produces the result in Figure 6.40. There is a slight variation in output power, although this is significantly smaller than that previously encountered. It can be seen that the coil current demand is varied to compensate for the varying EMF magnitude.

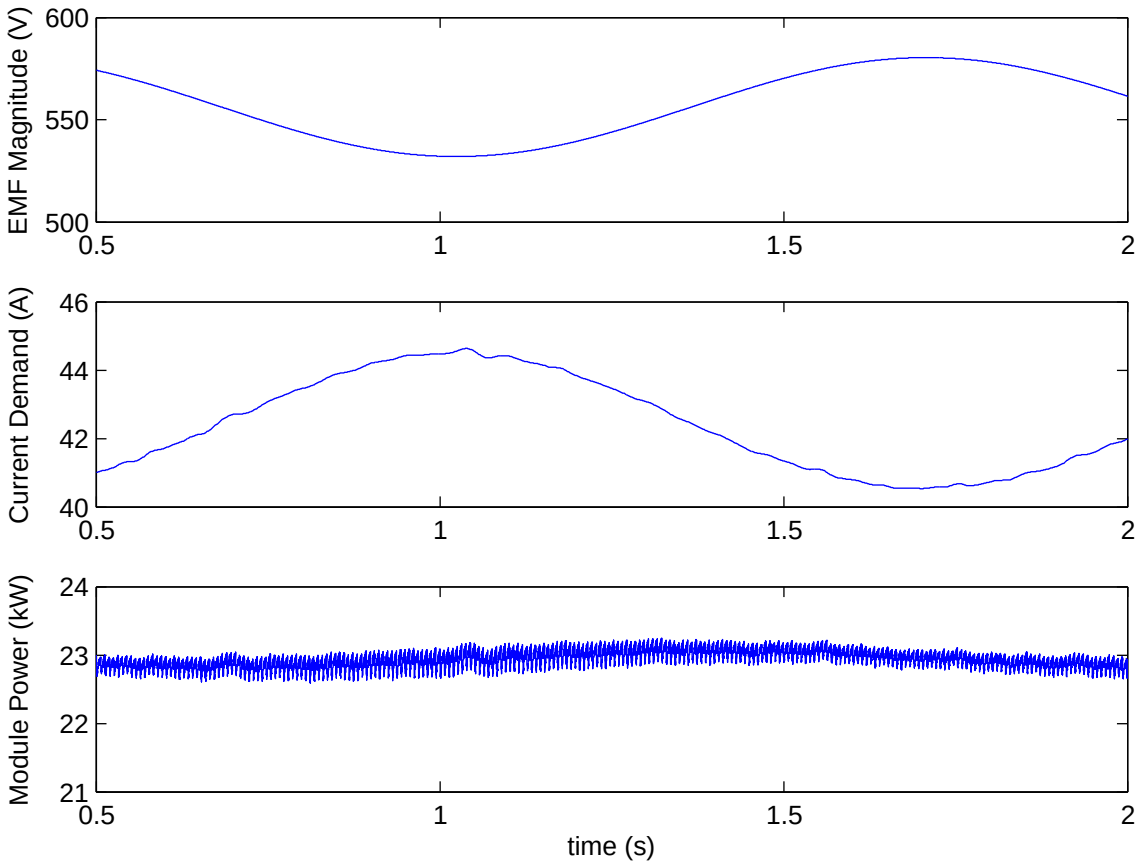


Figure 6.40: Eccentricity performance with DC-link voltage controller

A better performance could be achieved by having the DC-link voltage controller set the rectifier output current demand, with the coil current demand being

calculated from this using Equation 6.18, and the EMF magnitude calculated in Section 6.4.5. In this way the rectifier output current demand would be kept constant, with the coil current varying automatically depending on the calculated EMF magnitude. In practice, however, this system was found to be difficult to stabilise, as the EMF magnitude estimation and DC-link voltage controller interact in unwanted ways, and the original solution was deemed adequate.

6.7 Conclusion

An overview of the control system for the modular power conversion system has been given. A cascaded multilevel inverter is used, with DC-link voltage stabilisation achieved by driving each inverter module by a different set of generator coils. The control system can be broken into overall turbine control, inverter control, DC-link voltage control and rectifier control. Overall control was not considered.

An overview has been given of the inverter control algorithm, as this impacts the operation of the DC-link voltage controller and rectifier controller. It is also relevant as part of the inverter control algorithm will be implemented on the power modules, using the same microcontroller or DSP as the other controllers.

A controller has been designed and simulated to control the current in the generator coils to achieve unity power factor. Voltage feedforward is used to achieve the desired current, while a proportional controller is used to reduce the effects of 'cusp' distortion around the current zero-crossings.

A controller has been designed and simulated to estimate and track the position of the generator EMF, so that unity power factor current can be drawn. EMF position is estimated based on the voltage applied to the coils and the resulting current, and drives a phaselock loop (PLL). PLL bandwidth is selected so that the EMF position tracking operates faster than the turbine time constant.

A controller has been designed and simulated to regulate the DC-link voltage by controlling the coil current demand. A moving average filter is used to eliminate the ripple in the measured DC-link voltage caused by the single phase inverter output, and a PI controller used to set the coil current demand. System response varies depending on the turbine operating conditions.

Presence of airgap eccentricity requires that the EMF magnitude as well as posi-

tion are estimated, this will allow the coil current to be kept constant with changing EMF magnitude. The DC-link voltage controller will vary the coil current demand to compensate for the changing EMF magnitude in order to keep the power flow constant.

The next stage of the project is to develop a laboratory system to test the algorithms detailed in this chapter. This test system is the subject of the next chapter.

Chapter 7

Development of Prototype System

A prototype generator and converter system is required in order to test the power electronic and control concepts, described in the previous chapters, in a laboratory setting. The prototype system must follow the characteristics of the full-scale system, albeit at a reduced scale, where these characteristics impact on the aims of the experiment. Other characteristics can be changed to make conducting the experiment easier.

7.1 Aims of the Experiment

- To develop and verify methods of controlling the boost rectifiers on the machine side of the power electronic converter, in order to track the machine EMF and draw a sinusoidal current in phase with that EMF.
- To demonstrate the operation of a cascaded multilevel voltage source inverter (CMVSI), consisting of a large number of identical power electronic modules, as a means of interfacing a wind turbine generator to the grid.
- To analyse the effects of different inverter switching strategies on power sharing between modules, with equalised power sharing being a desirable characteristic of the experiment.
- To test methods of reducing distortion in the output waveform due to second-harmonic ripple in the DC-link voltage.
- To demonstrate the fault tolerance of the proposed system in the event of a

module fault. Module bypass systems are outside the scope of the experiment, and a fault can be simulated by having one module remain at zero output voltage while still conducting current.

- To demonstrate system stability under emulated wind conditions.
- To develop and verify methods of operation during grid fault and grid voltage dip conditions.

7.2 Motor-Generator Test Rig

The 1.8MW system has a 3-phase output, with each phase consisting of two parallel inverters of 13 modules each. For the sake of simplicity, the prototype system will consist only of a single inverter driving one phase, the operation of the other phases being identical. The number of modules in the inverter must be similar for the results to be applicable to the full size system.

A test rig was constructed using two 2.5kW axial flux generators, each with 12 coils, similar to the generator used in chapter 2 but larger. The generators were designed to have 210° phase separation between adjacent coils, giving a 90° separation between every third coil. This allows two coils to provide a constant power flow when connected to each module, giving 12 modules for a single phase inverter. Coil voltage was selected to be 23V RMS at 400rpm generator speed, if 12 modules are used then the DC link voltage will need to be 27.1V for 230V RMS output. In order to keep the boost ratio the same as the 1.8MW design, a coil voltage of 16.7V RMS is required at rated generator speed, giving a rated speed of 290rpm.

The two generators are driven by a 3kW induction machine through a step down gearbox, giving a maximum speed of 400rpm. The induction machine is driven by a vector-controlled variable speed drive, which can interface to a PC using an RS485 serial interface. The vector controlled drive and PC interface were selected to allow the motor to be controlled to emulate wind turbine dynamic characteristics.

There is insufficient space to mount the power electronic modules on the generators, and in any case for prototyping purposes it was decided to prioritise ease of access of the modules. For this reason the generator coils are connected to two junction boxes, one for each generator, with the junction boxes being connected to

a rack containing the modules. The test rig, without the power electronics rack, is shown in Figure 7.1.

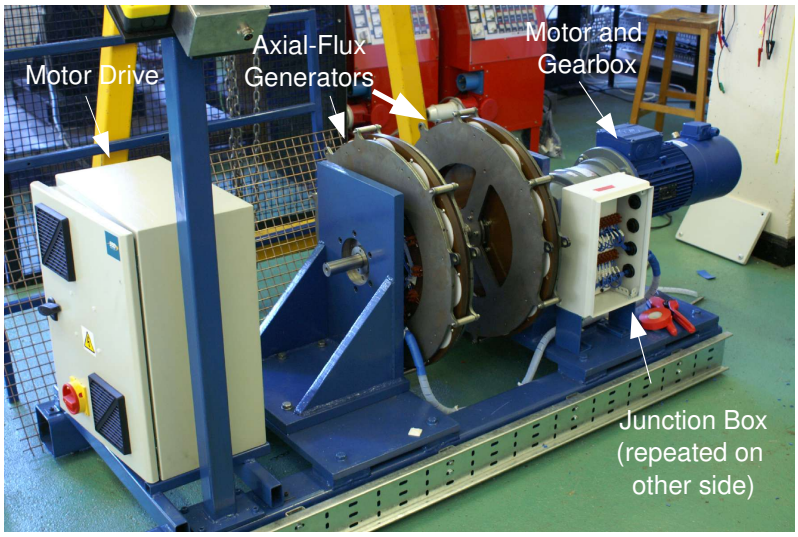


Figure 7.1: Motor-generator test rig layout

7.3 Prototype System Parameters

Using 290rpm as the rated speed of the prototype, 230V as the output voltage and 2.5kW as the rated power, other system parameters can be calculated by scaling the full-scale system power curve calculated in chapter 3. Parameters such as the generator coil inductance and resistance are determined by the generator design, while the rectifier switching frequency was chosen as in Section 4.2.3.

In order to test methods to reduce output voltage distortion due to second harmonic ripple in the DC-link voltage, the DC-link capacitance was chosen such that the per-unit ripple is the same as the full size system. The grid coupling inductance was chosen in the design of the inverter control system. The resulting parameters are given in Table 7.1.

7.4 Module Rack System

In order to allow the power modules to be easily removed for repairs and programming, it was decided to mount the modules in a Eurocard subrack. Each module has a connector at one end which carries both control signals and power, and the

Parameter	Full Size	Prototype
Phases	3	1
Strings per phase	2	1
Modules per string	13	12
Rated Power	1.8MW	2.5kW
Minimum Power	23.6kW	33W
Phase Voltage	6350V	230V
Rated String Current	47.2A	10.9A
Rated Speed	22.1rpm	290rpm
Maximum Speed	24.3rpm	319rpm
Minimum Speed	7.1rpm	93rpm
Rated Coil EMF	393V	16.7V
Maximum Coil EMF	432V	18.4V
Minimum Coil EMF	126V	5.4V
Rated Coil Current	26.7A	6.2A
Minimum Coil Current	1.2A	0.25A
Coil Inductance	8.2mH	0.46mH
Coil Resistance	0.345Ω	0.264Ω
Rectifier Switching Frequency	4kHz	16kHz
Average DC-link voltage	691V	27.1V
DC-link voltage, -2 modules	816V	32.5V
DC-link capacitance	1666μF	8800μF
Grid Coupling Inductance	20mH	3mH

Table 7.1: System Parameters

connectors plug into a backplane board, which has connections to the generator coils as well as the output and the communications signals. A front panel on each module forms the front panel of the rack. A diagram of the rack system for 4 modules is shown in Figure 7.2.

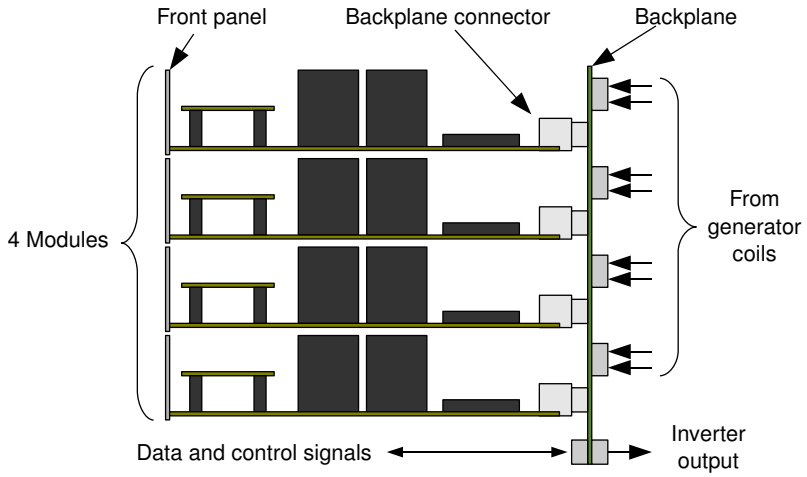


Figure 7.2: Overview of power module rack system.

The Eurocard specification defines boards of 100mm high, and are typically 160mm or 220mm long, with other increments of 60mm length sometimes used. The width of the subrack is 427mm, in units of 5.08mm, so with 12 modules a module width of 7 units or 35.5mm could be used. In practice it was found that only 6 or 8 unit front panels were available, so the module width was set at 6 units, or 30.5mm.

7.5 EMC Considerations

EMC, or Electromagnetic Compatibility, deals with the production of electromagnetic interference (EMI) by electronic systems, and the system's immunity to EMI. Power electronic systems, having high rates of change of current and voltage, will produce interference in the radio frequency range, which can be radiated or conducted to sensitive systems [48]. High rates of change of voltage are also present in communication systems, which often operate at high frequencies and over long distances.

EMI could be a problem in this system due to the high component density of the rack system, and the close proximity of power electronic and microelectronic systems.

EMI can be conducted along power conductors, coupling either magnetically or electrically with sensitive systems, or radiated as electromagnetic radiation received by other systems. Conducted interference is usually much greater than radiated.

7.5.1 Controlling EMI Emissions

EMI can be controlled in power electronics by limiting the rates of change of voltage and current through the use of a snubber circuit [48], but this has the disadvantage of increasing the switching losses, so should be avoided if possible. Resonant switching can also be used, although this increases the circuit complexity.

Electric coupling between adjacent conductors can be controlled by minimising the parasitic capacitance between them, while magnetic coupling can be minimised by minimising the area enclosed by a current loop [48]. In both cases this can be achieved by having feed and return conductors in close proximity, and minimising the lengths of conductors. This also applies to communication signals, which are best conducted by having the feed and return conductors as twisted pairs or coaxial cables.

7.5.2 System Grounding and Shielding

Each module has it's own local ground, and this will most likely be at a different potential from the system ground. The module itself has several different systems of components, and the grounds on these systems must be separated where possible in order to prevent crosstalk between systems.

Power and signal lines between systems on the module will transfer a current, leading to a corresponding current in the ground. Partitioning the grounding system allows this current to be diverted around sensitive systems or kept within an individual system. This is shown in Figure 7.3 [49].

Within the different systems of the module, and between the systems, power and signal lines must have the return conductor as close as possible, to avoid interference. This is best achieved by using a ground plane on the power and control boards. Different systems must have separate ground planes to prevent ground currents from approaching sensitive systems, as in Figure 7.3. Connections between ground planes of different systems should occur where the signals cross between the systems.

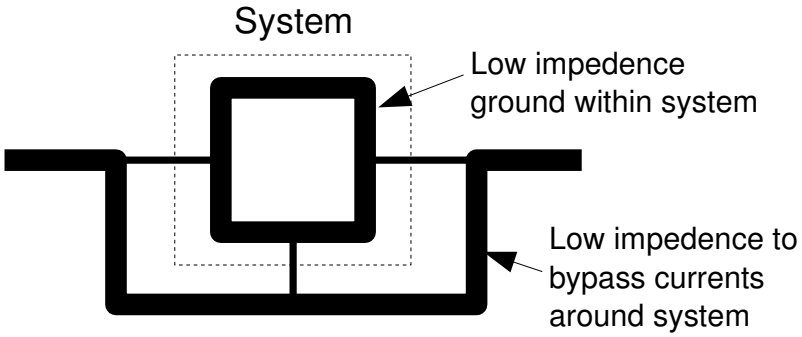


Figure 7.3: Diversion of ground currents around sensitive system.

The most critical area of the module is the control board, as it includes a sensitive analogue system and a digital system operating at many MHz. In this case, the use of a 4-layer PCB will allow two layers to be used as power and ground, providing a low impedance path for these currents, which will be relatively high and also pulsed. This reduces generated interference and also provides shielding for signal lines, with the effect being greatest when surface mount components are used [49].

Loops within the grounding system, such as when two components systems are connected together at multiple points, could allow currents to flow within the loop due to radiated interference, and should be avoided.

The entire inverter system must be screened to prevent interference with and from external systems. This is achieved by grounding the entire rack cabinet, with the module front panels completing the enclosure. If the rack system backplane features a ground plane then this will serve to shield any components behind the rack from interference.

7.5.3 Communications

A single-ended communication system, where the signal is transmitted as a voltage on a conductor relative to ground potential, is vulnerable to interference on that conductor, leading to false information being received. A differential system uses two conductors, with the signal being transmitted as the difference between the two conductors. Any interference will affect both conductors equally, provided they are in close proximity, and will not produce a false result.

Differential signalling can also have a higher signalling speed, over longer distances, as the voltage swings necessary to produce reliable signalling are lower. For

instance the single-ended RS232 standard has signals of typically ±12V, while the differential RS485 standard has signals of 0-5V on each conductor. These lower voltages allow faster swings from one state to another, with lower EMI.

EMI is minimised by twisting the conductors of the differential system together, which also reduces the magnetic fields produced by the communication system. If a PCB is used then the conductor tracks should be as close as possible.

7.6 Power Electronic Board Design

A schematic of the power board is shown in Figure 7.4, and includes the following components:

- Inverter and rectifier switching devices. Due to the lower switching voltage and higher switching speed compared with the full-scale system, MOSFETs will be used in place of IGBTs as the losses will be significantly lower.
- DC-link capacitors. To fit in with the low module height requirement, four smaller capacitors will be used in parallel, these will be electrolytic to achieve sufficient capacitance at low cost. A small polypropylene capacitor will be placed in parallel to provide a low ESR path for high frequency currents, to reduce switching noise.
- Brake resistor and transistor. The main purpose of the brake resistor is to control the DC-link voltage when the inverter is not operating. A 2Ω thin film resistor was chosen, but this was found to overheat and fail easily, so was replaced by a ceramic wirewound resistor of the same value.
- Voltage and current transducers. Currents in both coils and in the inverter output are measured using hall-effect sensors, which give an output that varies about 2.5V. DC-link voltage is measured using a potential divider.
- Input protection. Fuses are provided on the input, as in the full-scale module design. Transient voltage suppressors prevent high voltages in the coils when the fuses blow.
- Gate drivers (not shown) for all the switching devices are located on the power board.

- Isolated power supply (not shown). A 12V DC auxiliary supply is provided from the backplane to power the module control circuits. As the modules are all at different potentials, an isolated DC-DC converter is used to transform the auxiliary supply to the module potential.

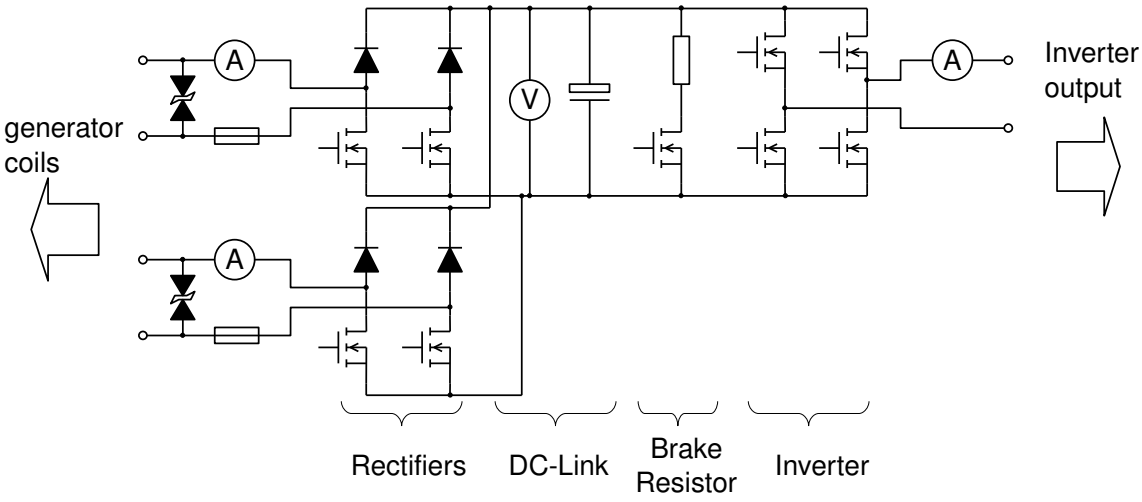


Figure 7.4: Test system power module schematic

7.6.1 Transistor Cooling

Transistor losses are calculated in a similar way to that used in Section 4.5, except that a MOSFET behaves simply as a resistor in the on state, and switching losses are small at the switching speed used. For the MOSFETS and boost diodes, components were oversized in order to reduce losses and hence the cooling required, this had a negligible cost penalty.

The MOSFET used was the IRFZ44VZPbF, which has a blocking voltage of 60V and an on-state resistance of 12mΩ at 25°C, rising to 24mΩ at 150°C, and a maximum junction temperature of 175°. The boost diode used was the STPS20L60CT, which has a blocking voltage of 60V and a forward voltage drop of 0.56V, with each package containing two diodes.

In order to simplify the module construction it was decided to use surface mount transistors, using the PCB copper area as a heatsink. The D_2PAK case of the MOSFETs and diodes under consideration has a thermal resistance of 33.6°C/W when the minimum board area is used, and 18°C/W when a 1 square inch area of

board is provided [50]. Allowing a 125°C temperature rise, the maximum loss per device is 3.7W with no extra area and 6.9W with 1 square inch area.

The losses of the various devices in the design at rated power are given in Table 7.2. Calculation was done assuming a junction temperature of 150°C as a worst case scenario. As there are two rectifiers and only one inverter, the inverter has to handle around twice the current of the rectifiers. With the MOSFET conduction loss appearing as a resistance, the loss in the inverter MOSFETs is almost four times that of the rectifier MOSFETs. Based on these losses, it appears that the rectifier MOSFETs can use the minimum space while the inverter MOSFETs and rectifier diodes will need extra space.

Device	Loss (W)
Rectifier MOSFET	0.98 per device
Rectifier Diode	2.4 per device, 4.8 for package
Inverter MOSFET	3.8 per device

Table 7.2: Estimated switching device losses

7.6.2 Prototype Power Board

A prototype power board was designed using the board space requirements calculated above, and based on a 160mm long, 100mm high eurocard design. This board was used in development of the control algorithms using a DSP development board in place of the dedicated control board. This system is shown in Figure 7.5 below.

7.6.3 Evaluation of Cooling Capability

Cooling capability was evaluated using a thermal imaging camera, which will record the temperatures of the components on the board as well as the distribution of temperatures. Testing was carried out using the prototype board, running the rectifier control algorithm detailed in the previous chapter, the inverter output was switched at a fundamental frequency square wave. Rated power conditions, as specified in Table 7.1 were used, with the inverter connected to a resistive load and the resistance varied to achieve the desired output current.

The power board was mounted vertically in front of the thermal camera, and painted matte black to reduce reflections and bring the emissivity close to 1, for

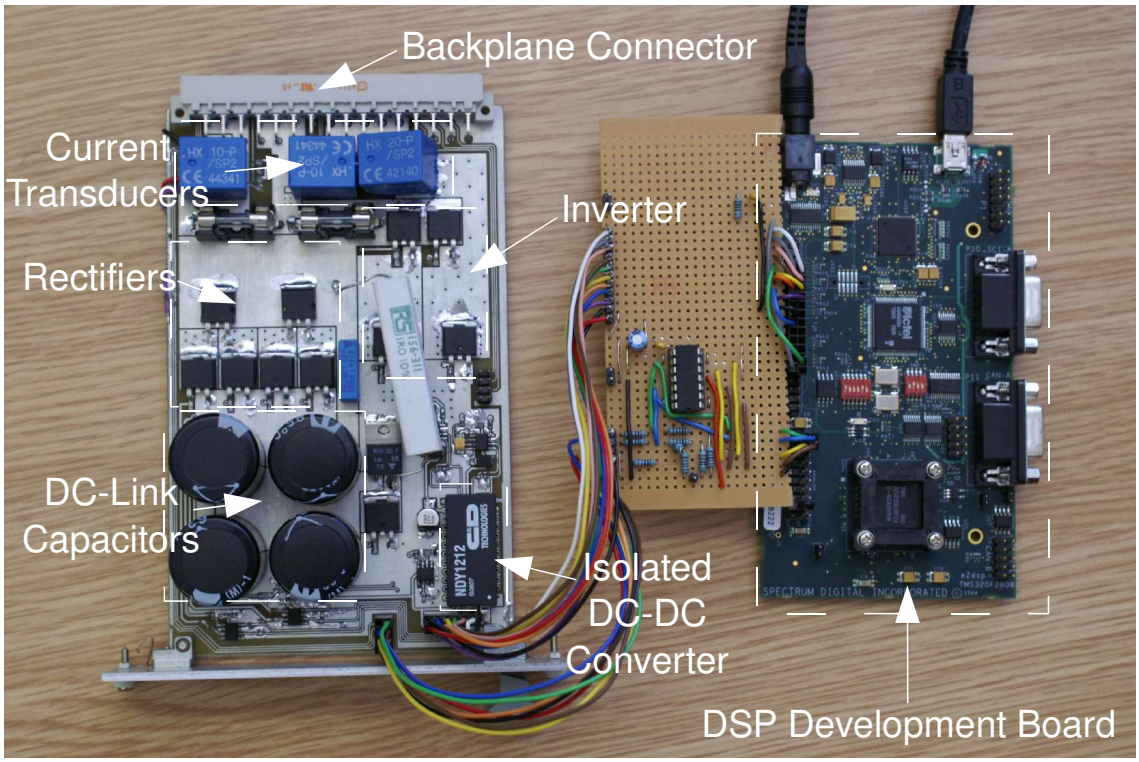


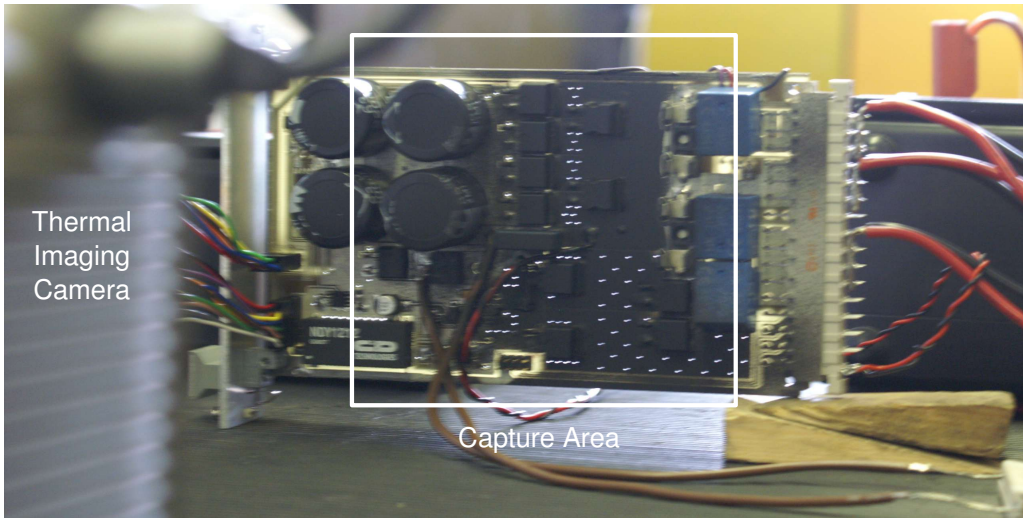
Figure 7.5: Prototype power board

the highest accuracy. Measurements were taken with passive cooling and with a fan mounted above the board. The test setup is shown in Figure 7.6a, along with the area captured by the camera.

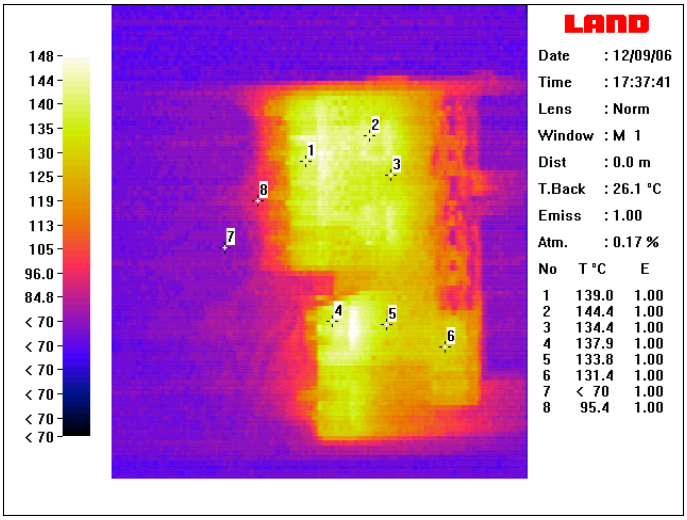
It can be seen in Figure 7.6b that high temperatures are achieved in the passively cooled test, with the upper inverter MOSFET, labeled 4 on the picture, reaching 138°C. As the junction to case thermal resistance is 1.64°C/W, this gives a junction temperature of 144°C, assuming the losses in Table 7.2. The rectifier MOSFETs are also at a high temperature, suggesting that the losses were underestimated in Table 7.2.

The results of the fan-cooled test, shown in Figure 7.6c show greatly reduced temperatures, with the inverter MOSFETS reaching a case temperature of 104°C, compared with 138°C. In particular the inverter MOSFETs are of similar temperature, and the rectifier MOSFETs are at a lower temperature relative to the other devices. This suggests that where passive cooling is used the lower devices will have a tendency to heat up the upper ones, leading to an uneven temperature distribution. This effect is greatly reduced if a fan is used.

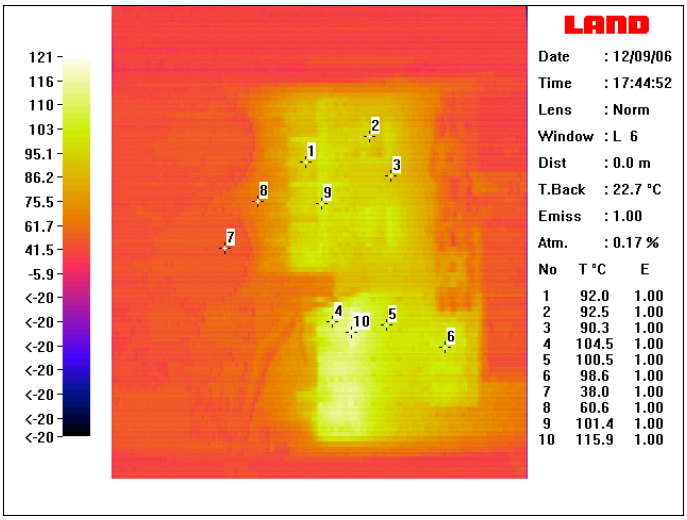
The tests show that even with passive cooling the board area given over to



(a) Thermal imaging test setup.



(b) Board temperatures, passive cooling.



(c) Board temperatures, fan cooling.

Figure 7.6: Evaluation of power board thermal performance

heatsinking purposes is adequate. However when the board is used in a rack the airflow could be reduced, leading to higher temperatures, so for this reason and for the benefits of more even heat distribution, the use of forced air cooling is recommended.

7.6.4 Final Power Board Design

In order to provide more space for the control board, the power board was redesigned using a 220mm long board rather than the 160mm used before. The ground area at the system ground at the front of the board was also enlarged to prevent the floating module ground from shorting against the front panel. The final board is shown in Figure 7.7. Full schematics of the power board are given in appendix B.

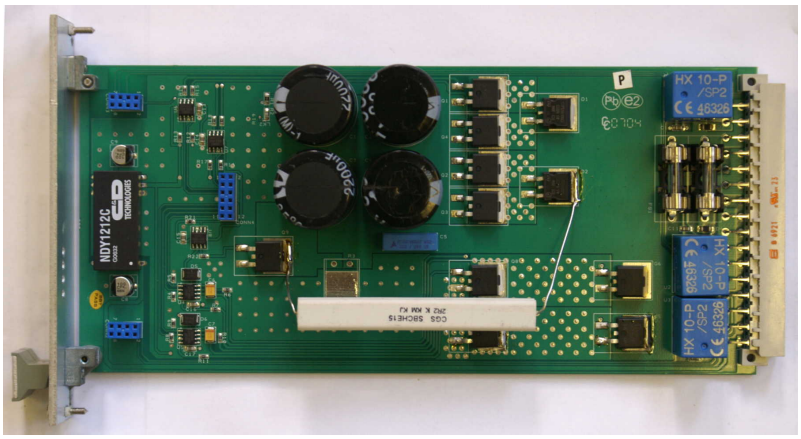


Figure 7.7: Final power board design, without control board.

7.7 Control Board Design

The module controller must record the outputs of the voltage and current transducers, and implement the rectifier control algorithm in some form of microcontroller or DSP, then produce a PWM signal for the rectifier transistors. It must also control the inverter switching, based on an internal timebase, which is synchronised to that of a central controller. It must also receive an error signal, to correct harmonic distortion in the inverter waveform, from the central controller. It would also be useful to send status information to the central controller and also to a monitoring PC.

In a classic multilevel inverter implementation, the individual levels are supplied with gating signals from a central controller, via some form of isolated connection. This requires a complex central controller, which represents a single point of failure for the system, and a large number of connections to carry the gate drive signals. A cascaded multilevel inverter system using a distributed timebase exists [51], but uses only two modules per phase rather than the twelve proposed here. For this reason the communication system between the modules and central controller is considered the most critical part of the project and will be considered first.

7.7.1 Communication and Synchronisation

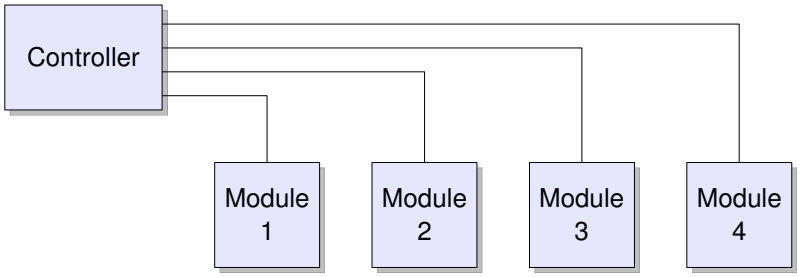
For synchronisation purposes, and for harmonic distortion correction, a low latency is required in the communication system, along with a high bandwidth. For monitoring of status signals this is less important, although some errors may need to be acted upon quickly. Fault tolerance and resistance to noise are also desirable characteristics of the communication system.

A distinction should be made here between communication based on a series of connections from the controller to the individual modules, shown in Figure 7.8a, and communication based on a common bus to which all modules are connected, shown in Figure 7.8b. The former requires a large number of connections and a controller capable of generating many communication signals, and so is not desirable for this project.

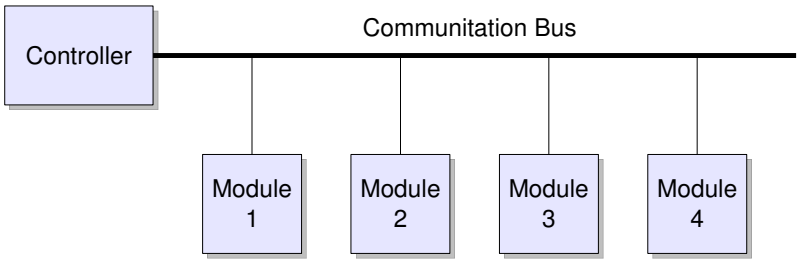
Space for the control board is limited, so it is desirable to use communication interfaces that are built into the microcontroller, which will reduce the component count of the controller. An analysis of the various options currently available on microcontrollers is given here.

Analogue and Digital IO

A simple digital signal could easily be used for synchronisation of the modules with a central controller. For instance the central controller could send a pulse, on a bus connected to all modules, at the zero-crossings of the required output waveform. This could be captured by the capture circuit used on many microcontrollers, which will record the time of the pulse relative to an internal clock on the microcontroller. This can be used to accurately synchronise the timebase.



(a) Point-to-point connections



(b) Bus connection

Figure 7.8: Communication architectures between the controller and modules.

Analogue signals can also be sent to the modules, although they will be much harder to isolate and more prone to interference. An analogue bus has been used in a modular converter system to synchronise and interleave PWM waveforms on several modules [52], but the switching frequency was much higher than proposed here, so a digital system would not have been possible.

An analogue bus would be more appropriate to carry the distortion correction signal to the modules as it would be easy to implement in software. In this case a digital signal could perform synchronisation. Another communication system would have to carry other commands to the modules and return status information, resulting in a profusion of different communications systems.

I^2C and SPI

I^2C and SPI stand for Inter-IC and Serial Peripheral Interface respectively, and both of these systems are serial connections designed to interface a processor to another processor, or to peripheral circuits. Both offer a high bandwidth of up to 1MBit/s, and low latency, but offer little in the way of error correction or fault tolerance, which must be implemented in software.

While SPI was used in a similar modular inverter system [51], the number of modules was much lower at two per phase, and it is believed that an SPI system will

increase in complexity significantly with the proposed twelve modules. Ultimately neither system is designed for the purpose required.

Asynchronous Serial

Most microcontrollers include an asynchronous serial receiver/transmitter (UART). When used with an RS485 transceiver this allows a serial communication bus with multiple receivers and transmitters. RS485 is a differential bus, giving good noise immunity over long distances, and high bandwidth.

RS485 transceivers must be switched to transmit when required, and more than one transceiver is not allowed by the specification to be switched to transmit at any one time. Preventing two modules from transmitting at once, as well as addressing individual modules, information structure and fault tolerance must be handled by a higher level protocol. This protocol must be implemented in software on the microcontroller, reducing the time available for processing the main control algorithms.

One such protocol is the Modbus protocol, designed for factory automation, and with a simple implementation on serial networks. Modbus is a master-slave system, in which a master node on the network sends requests for information to the slave nodes which then give a reply. In this way two nodes are prevented from transmitting at one time.

The Modbus serial data frame is shown in Figure 7.9 [53]. Slave nodes, i.e. the power modules, each have their own address, from 1 to 247. It is also possible to send commands to all nodes on the network, at address 0, although the nodes cannot then reply. The data frame can be sent as either binary data or ASCII characters, depending on the implementation, and the data frame also includes an error checking field, with the node returning an error if the data is corrupted.

The Modbus application protocol provides a number of functions for accessing and manipulating data on the slave device, with data being arranged in registers. Data can be either boolean (on/off) or 16-bit integers, with separate registers for each. A number of data frames, representing functions for manipulating data in registers, are shown in Figure 7.9 [54].

Latency could be low with the Modbus protocol, as the serial receiver on the microcontroller can be programmed to generate an interrupt, which will run specific code on reception of data. However there is no way for the slave nodes to alert the

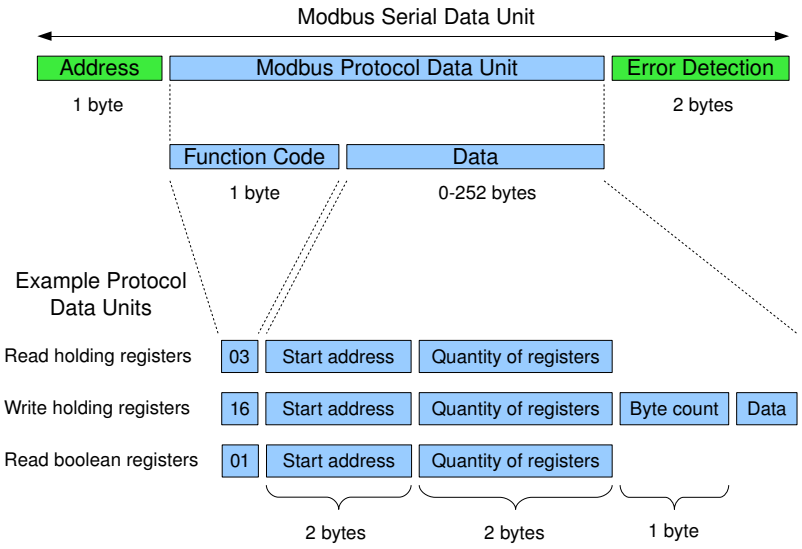


Figure 7.9: The Modbus serial data unit

central controller to errors that require immediate action, as they would have to wait to be polled for information. This issue, and the fact that the protocol must be implemented in software mean that Modbus protocol, using serial communications, would be more suitable for communication with a PC for monitoring purposes.

Controller Area Network (CAN)

CAN is a network protocol designed for automotive use, but also popular in factory automation, and is often implemented in hardware on some of the more powerful microcontrollers. CAN is implemented on a differential bus, which can have two states: dominant, representing 0, and recessive, representing 1. A recessive bit transmitted by one node on the network is overridden by a dominant bit transmitted by another node. Speeds of up to 1MBit/s are supported, and the data frame is small, giving low latency.

The basic CAN message frame is shown in Figure 7.10 [55]. The arbitration field of the message contains a message identifier, which can be 11 or 29 bits long. The control field contains the data length and other information, while the data field contains 0-8 bytes of information. Finally the CRC field contains the cyclic redundancy check, for detecting errors.

While a node on the network is transmitting, it is also checking the network state. If two nodes start transmitting simultaneously, then they will continue transmitting until there is a difference between the data transmitted by each node. At this point

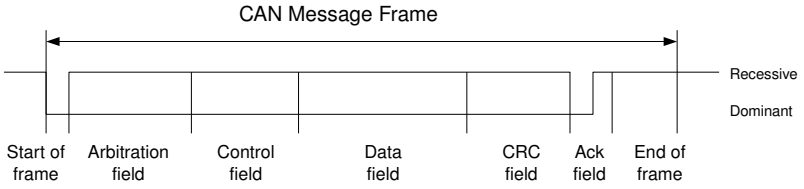


Figure 7.10: CAN standard message frame

the dominant bit from one node will override the recessive bit from the other one, and the node transmitting the recessive bit will notice this and cease transmission while the other node continues. This is likely to occur while the message identifier field is being transmitted, and means that messages with a lower message identifier are prioritised.

The message identifier, in the arbitration field, identifies the message frame as a particular unit of information, and the CAN controllers can be programmed to react differently to messages with different identifiers. For instance, one identifier could be used to identify an inverter synchronisation frame, from the central controller, which all modules will receive, and which will cause an interrupt, running specific code with low latency. Another identifier could be used to request information from a specific module, with the other modules ignoring this message.

The flexibility of CAN and the low latency, as well as the fact that the protocol is mainly implemented in hardware, make it ideal for interfacing the power modules and the central controller. The small data field in the data frame, and the cost of CAN-to-PC interfaces mean that it is less suitable for general monitoring.

Choice of Communication Interfaces

Based on the strengths and limitations of the different systems mentioned above, CAN will be used for synchronisation of the modules and real time control, while Modbus over RS485 will be used for monitoring by a PC. A separate digital synchronisation line is deemed not to be necessary as the CAN interface should be able to synchronise to an accuracy of 1μs, corresponding to 0.018° in a 50Hz cycle. An extra RS485 output will also be provided, connected to a spare PWM output, which will be able to be wired to provide an analogue signal, or a trigger signal for external test equipment. All communication interfaces will need to be galvanically isolated due to the varying potential of the modules relative to the system ground.

7.7.2 Choice of Microcontroller

The most suitable microcontroller for the control board was found to be the recently released TMS320F2808, from Texas Instruments, which is a 32-bit microcontroller designed for power electronic use, and featuring many DSP features. In common with most microcontrollers the program can be run from built in re-writable FLASH memory, and many communication interfaces, including serial and CAN are built in, as is an analogue to digital converter (ADC). There are several other features that make this microcontroller suitable:

- A powerful and flexible PWM system, based around 6 modules providing 2 outputs each. Each module has it's own timebase, and the timebases can be synchronised between modules, with phase shifts. The PWM system can trigger interrupts at specific points to run code, or can trigger ADC conversions.
- An autosequencing ADC, which can take a number of conversions when triggered, and store the results in separate registers, cutting down on the amount of supervision by the processor.
- A high speed of up to 100MHz, and the ability to process one instruction per clock cycle.
- An enhanced CAN controller, providing 16 mailboxes, which can receive or transmit messages with specific identifiers. Each mailbox can cause an interrupt on message reception, or can wait until polled by software. Each mailbox also includes a time stamp, which records when the message was received or transmitted relative to an internal clock.

A disadvantage of this microcontroller is that it requires both 3.3V and 1.8V power supplies, with separate analogue and digital supplies, and connections at various points around the chip. This means that a 4-layer board will be required, increasing complexity.

7.7.3 Other Control Board Components

Power is supplied from the isolated DC-DC converter on the power board at 12V, and a 3.3V supply for the digital section of the control board is derived by a switching

regulator. The 1.8V supplies for the microcontroller digital and analogue cores are derived from the 3.3V digital supplies using linear regulators, while the 3.3V analogue supply is derived from the 12V supply using a linear regulator.

Analogue signals from the current sensors on the power board are in the range of 0-5V, and these are reduced to 0-3V by a potential divider circuit. These signals, along with the DC-link voltage signal, are buffered using an operational amplifier in order to provide a low impedance to the microcontroller ADC, to decrease acquisition time. As the ADC conversions will occur at twice the PWM switching frequency, triggered by the PWM carrier, an anti-aliasing filter is not required, simplifying the board layout.

The RS485 and CAN transceivers are on a section of the control board which is at the system ground potential, and are optically isolated from the rest of the control board. A 3.3V supply for the transceivers is derived from the 12V system supply using a linear regulator.

A 4-pole DIP switch is provided to set the module number, which determines the address for communications, as well as the switching order for the inverter output. Another DIP switch is provided to set the boot method for the microcontroller – the microcontroller is programmed by setting it to boot from the serial IO, and running a programming application on the host PC.

Four LEDs are mounted on the front panel end of the board to provide status information. One is connected to the control board 3.3V digital supply while the others are under the control of the microcontroller. A serial EEPROM is provided on the board to store setup parameters, although this has not been used.

7.7.4 Board Layout

A primary aim with the control board design is to minimise EMC issues. This is achieved by dividing the components among four sections: the digital section, analogue section, power supply and communication section. These sections have their own ground planes, which are connected at single points to avoid ground loops, with the exception of the communication section, which is isolated and at system ground potential. A 4-layer board is used to minimise interference from the power drawn by the microcontroller, and all the microcontroller power pins have decoupling capacitors.

The control board is shown in Figure 7.11, with the different sections of the board indicated. The digital section is connected to the main module ground, via the gate connector, as is the power supply. The communication section shares the ground with the system ground, connected at the communications connection. The analogue section has a separate ground, connected to the digital ground at the power supply. The analogue ground is connected to the analogue ground of the power board at the analogue connection – there is no connection between the analogue and module grounds on the power board in order to avoid ground loops. This is shown in Figure 7.12. Full schematics of the control board are given in appendix B.

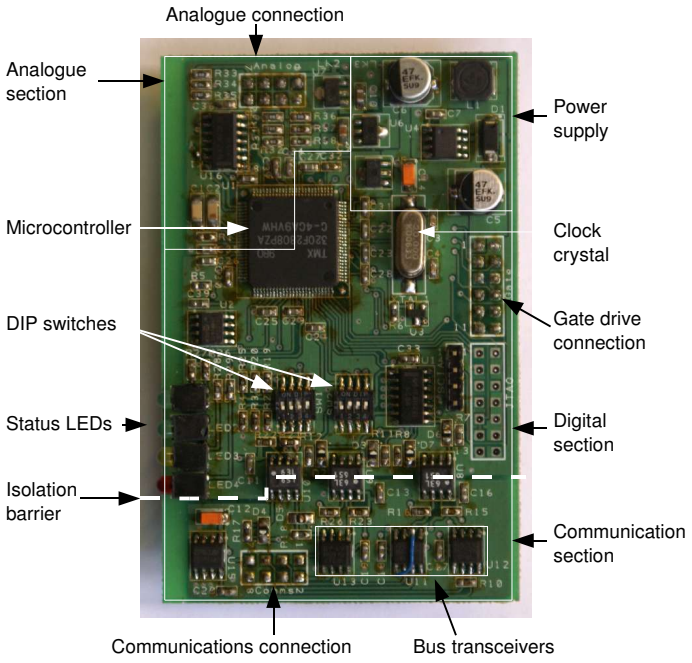


Figure 7.11: Control board layout.

7.8 Test System Hardware Overview

The complete module with control board is shown in Figure 7.13. A diagram of the complete test system is shown in Figure 7.14. From the motor-generator test rig described in Section 7.2, connections to the individual coils are made to two junction boxes. These are then connected to the module rack system.

The rack contains not only the modules, but cards to measure the inverter and grid voltage, and the output current. A grid side inductor is included, as is an overload circuit breaker, to limit the output current. An auxiliary power supply

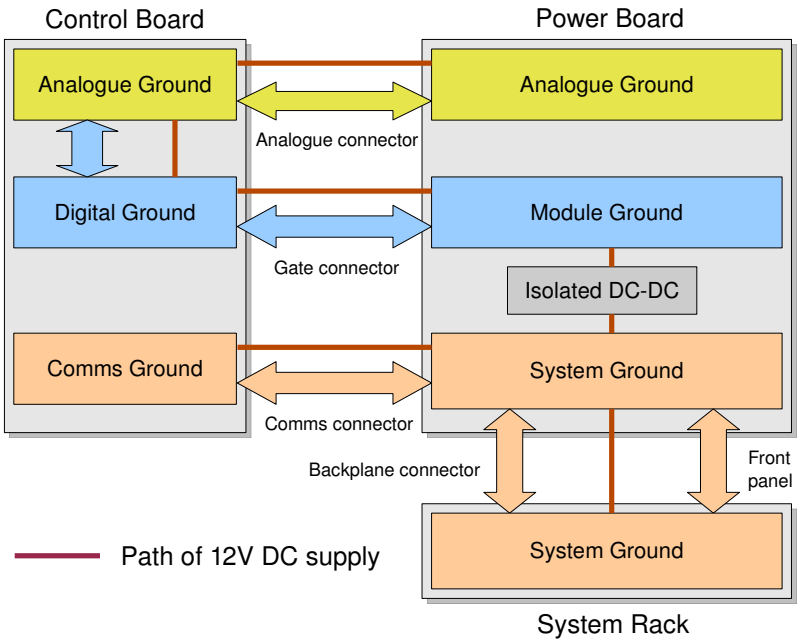


Figure 7.12: Module ground map.

provides 12V DC to the modules and measurement cards. The layout of the rack is shown in Figure 7.15. The output of the inverter is connected to the grid via an isolation transformer and variac.

A DSPACE rapid development system is used as a central controller for the inverter, and measures the analogue voltages from the voltage and current measurement cards. It then synchronises and controls the inverter through the CAN bus. The DSPACE is programmed and monitored using a PC.

A second PC monitors and controls the modules and motor drive via an RS485 interface, using the Modbus protocol. Software implemented in LabView is used for this purpose.

7.9 Central Controller Operation

Operation of the central controller, and the signals sent by it to the modules, has a significant impact on the operation of the inverter controller on the modules, so an overview of the central controller will be given in this section. The central controller is implemented on a DSPACE rapid development system, with the development carried out in Simulink and compiled into code for the DSPACE.

The controller structure is given in Figure 7.16. The grid voltage is sampled and

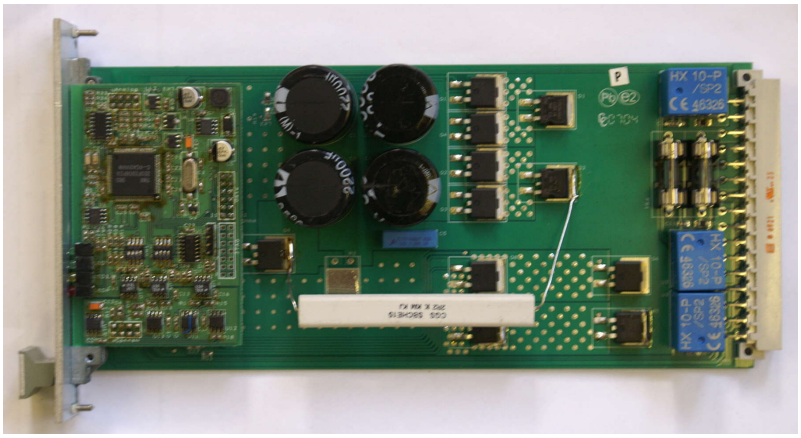


Figure 7.13: Complete module with control board.

fed into a phaselock-loop (PLL), which calculates the grid angle θ and frequency ω. This PLL is similar to the one used on the modules to estimate the machine coil EMF, except that it takes a single phase input. This means that the output of the phase detector will have a large second harmonic component, and the loop bandwidth must be low in order to filter this. A loop bandwidth of around 2Hz was used.

The magnitude $|V^*|$ and angle ϕ of the inverter output voltage required to achieve the desired real and reactive power, are calculated in the same way as in Section 6.3. The desired inverter output voltage magnitude is divided by the number of modules, to obtain the module DC-link voltage demand. This is sent to the modules over the CAN bus. The angle, which is relative to the grid voltage angle, is added to the calculated grid voltage angle to obtain the absolute inverter reference angle θ_{ref}.

The zero-crossing of the inverter reference angle is detected, and used to trigger a synchronisation CAN message frame, to tell the modules to reset their inverter time bases. As the reference angle is incremented at the program sampling frequency of 20kHz, the zero-crossing will be detected a short interval after the zero-crossing has occured. Because of this the reference angle is sent to the modules, and the module time base set accordingly, rather than being set to zero. The grid frequency is also sent to the modules.

The magnitude and angle of the required inverter voltage are used to calculate a real-time value of the required voltage. The measured inverter voltage is subtracted from this and the resulting error voltage is passed into a proportional-integral (PI) controller. The output of the PI controller is an error voltage, which is sent to the

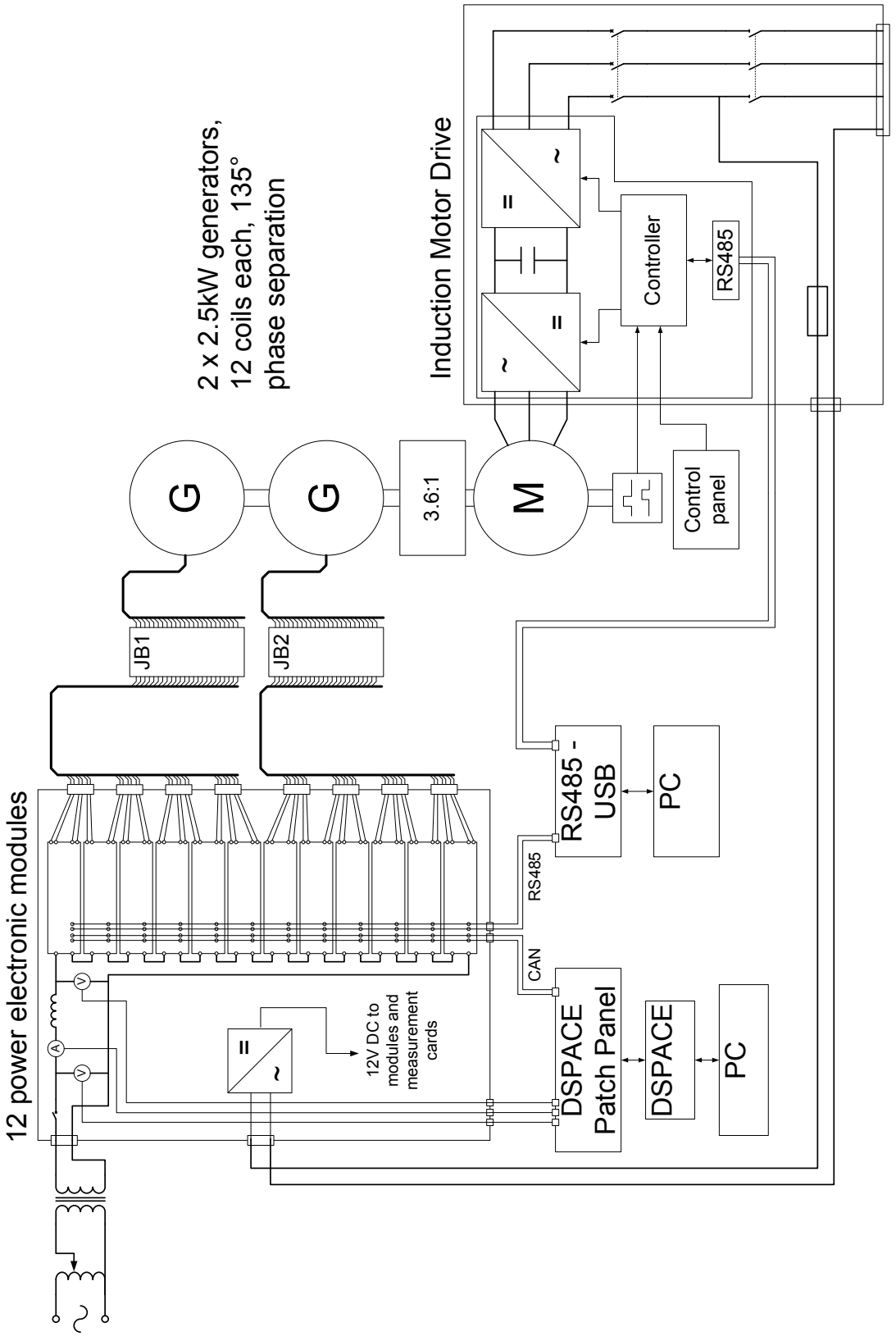


Figure 7.14: Diagram of the complete test system.

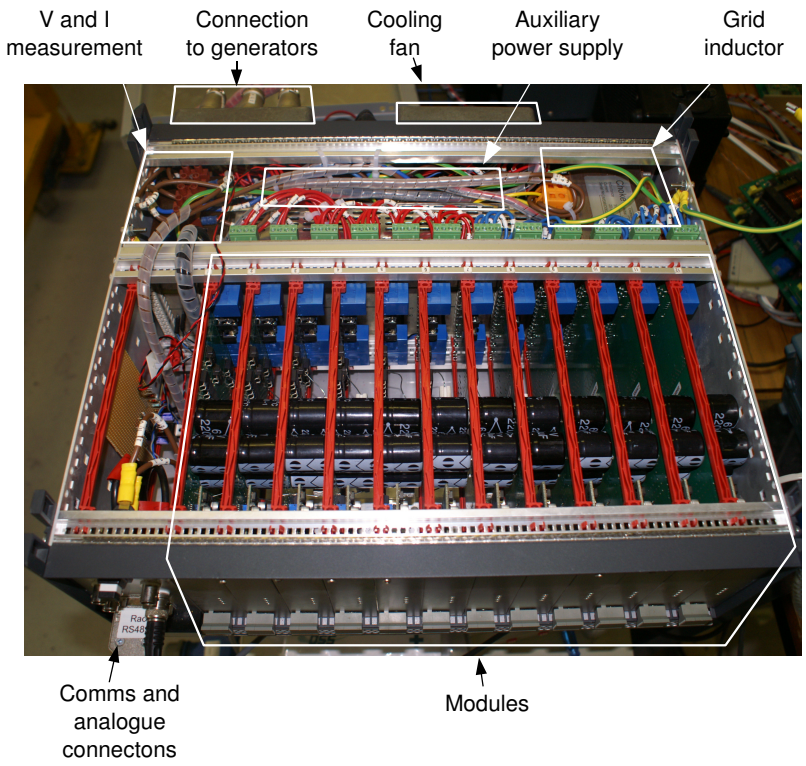


Figure 7.15: Layout of the power electronics rack.

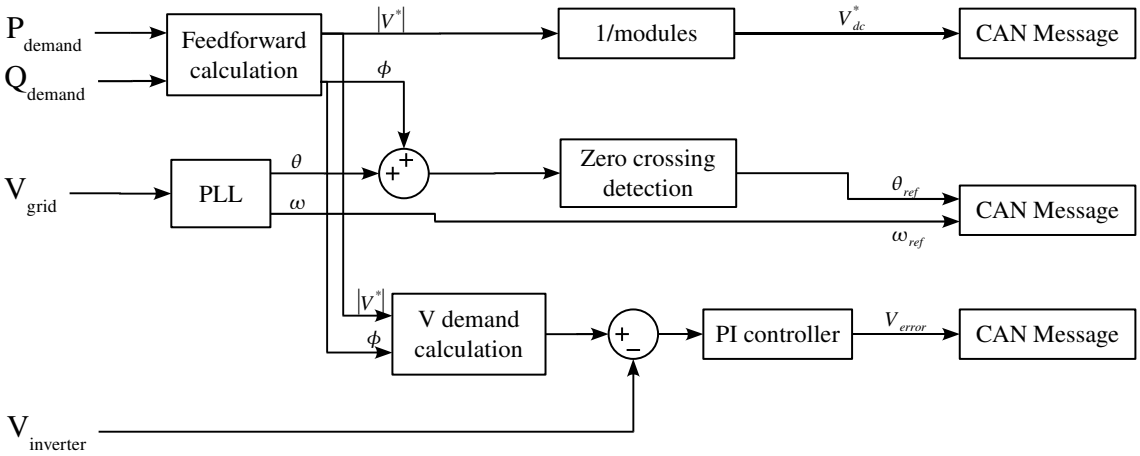


Figure 7.16: Central controller program structure

modules over the CAN bus at a rate of around 10kHz.

7.10 Module Control Software Implementation

Code listings for the most important functions of the microcontroller software are given in appendix C. It should be noted that this code is for the advanced control system described in chapter 9, but the rectifier control code functions identically to that described in this chapter.

Software on the module microcontroller was implemented in the C language, using the DSP/BIOS real time operating system supplied by Texas Instruments, the makers of the microcontroller. This provides an easy system for creating multi-threaded applications. DSP/BIOS provides several different types of thread for running code, with varying levels of priority [56].

- Hardware Interrupts are triggered by hardware events in the microcontroller, and have the highest priority, running code functions as soon as they are triggered. They are generally used for tasks that need to happen with short deadlines. Hardware interrupt functions can prevent other hardware interrupts from running until they finish, so the function code should be short.

- Software Interrupts are triggered by calling specific functions from within the program, and have a lower priority than hardware interrupts. They are used for threads that have time constraints that are not as severe as to require hardware interrupts, and run to completion. A hardware interrupt can trigger a software interrupt to perform additional processing at lower priority. Periodic functions also exist, which are a form of software interrupt run at specific intervals.

- Tasks have a lower priority than software interrupts, and have the ability to pause execution until resources are available, allowing other code to run. Tasks are not used in this project.

- The Idle Loop is a thread that operates continuously at the lowest priority. Each function in the idle loop is called in each iteration of the loop, which is run whenever no other threads are running.

The control system described in chapter 6 can be broken down into a number of processes, which run at different intervals and require different priorities and

deadlines. The arrangement of processes for the rectifier and inverter, as well as communications and miscellaneous functions, will be described separately.

7.10.1 Representation of Control Variables

Most variables are represented as 16-bit signed integers, having a range of -2^{15} to $2^{15} - 1$. Scaling of the variables is kept identical for all variables representing the same quantity, for instance in all voltage variables a value of 10,240 will represent a voltage of 15V. The variable representing the generator speed/frequency is scaled so that it is equal to the RMS EMF produced by the coils at that speed. Angles are represented with the variable range representing the angles $-\pi$ to π, which is determined by the input ranges of the trigonometric functions supplied by Texas Instruments.

Other variables and constants are derived from these quantities and the methods of calculation. For instance, the voltage drop across a resistance is calculated as follows: Voltage=((**long**)Current∗(**long**)Resistance)>>15, where the two 16-bit values are multiplied to produce a 32-bit result, which is then barrel shifted back to a 16-bit quantity. The voltage drop across and inductance is calculated in a similar way, with an extra step to calculate the reactance from the inductance and frequency values. The (**long**) typecasts are necessary for the microcontroller to know that the result is 32-bit, and not discard the upper 16 bits.

Barrel shifting, represented as << or >> is a shifting of a variable the a number of binary digits to the right or left, so a shift of 1 represent a multiplication or division by 2, depending on the direction, and a shift of 15 represents multiplication or division by 32768, or 2^{15}. This method is used anywhere two 16-bit variables are multiplied to give a 16-bit result. The ranges of various quantities are shown in Table 7.3, along with the quantity the real world values must be multiplied by to calculate the microcontroller values.

Quantity	Range	Multiplier
Voltage	±48V	683
Current	±36A	910
Frequency	±68.9Hz	476
Resistance	1.33Ω	24582
Inductance	2.79mH	11744

Table 7.3: Range and calibration of various quantities.

7.10.2 Rectifier Controller

Control of the rectifier can be split into three processes:

- A hardware interrupt service routine (ISR) running at 16kHz, which handles sampling of the coil currents, line current and DC-link voltage, and operation of the current proportional controller. This must run at extremely low latency, so a hardware interrupt is required, and the amount of processing is small so that the ISR can finish quickly and not delay other hardware interrupts. 2-step averaging filters are used on the values passed to the next process, in order to prevent aliasing, as the next process runs at half the frequency. The machine electrical angle estimate is also incremented in this process.

- A software interrupt running at 8kHz, which handles transformation between fixed and rotating reference frames, as well as conversion between duty cycle and voltage. This must be carried out at high speed as the values in the fixed reference frame will be constantly changing, and cannot be processed at a lower speed. 250Hz, 2-pole butterworth low pass filters are used on values passed to the next process, in order to prevent aliasing.

- A software interrupt running at 1kHz, which handles the EMF estimation functions, the EMF position PLL and voltage feedforward calculations.

The distribution of the rectifier control functions between the three processes is shown in Figure 7.17. Operation of the system was described in chapter 6, with the main difference being the presence of the different sampling rates and anti-aliasing filters.

Peripheral Setup and Hardware Interrupt

The microcontroller is set to run at a clock speed of 100MHz, the maximum supported. Two PWM modules, 3 and 4, are used for the rectifier. In both these modules the main clock is divided by 6, and a time period of 520 clock pulses is used in the count up-down mode. This gives a PWM frequency of 16kHz. PWM module 3 will send a synchronisation pulse to module 4 when the timebase reaches zero. This will cause module 4 to set it's timebase to 520, counting down, resulting in the phase relationship shown in Figure 7.18.

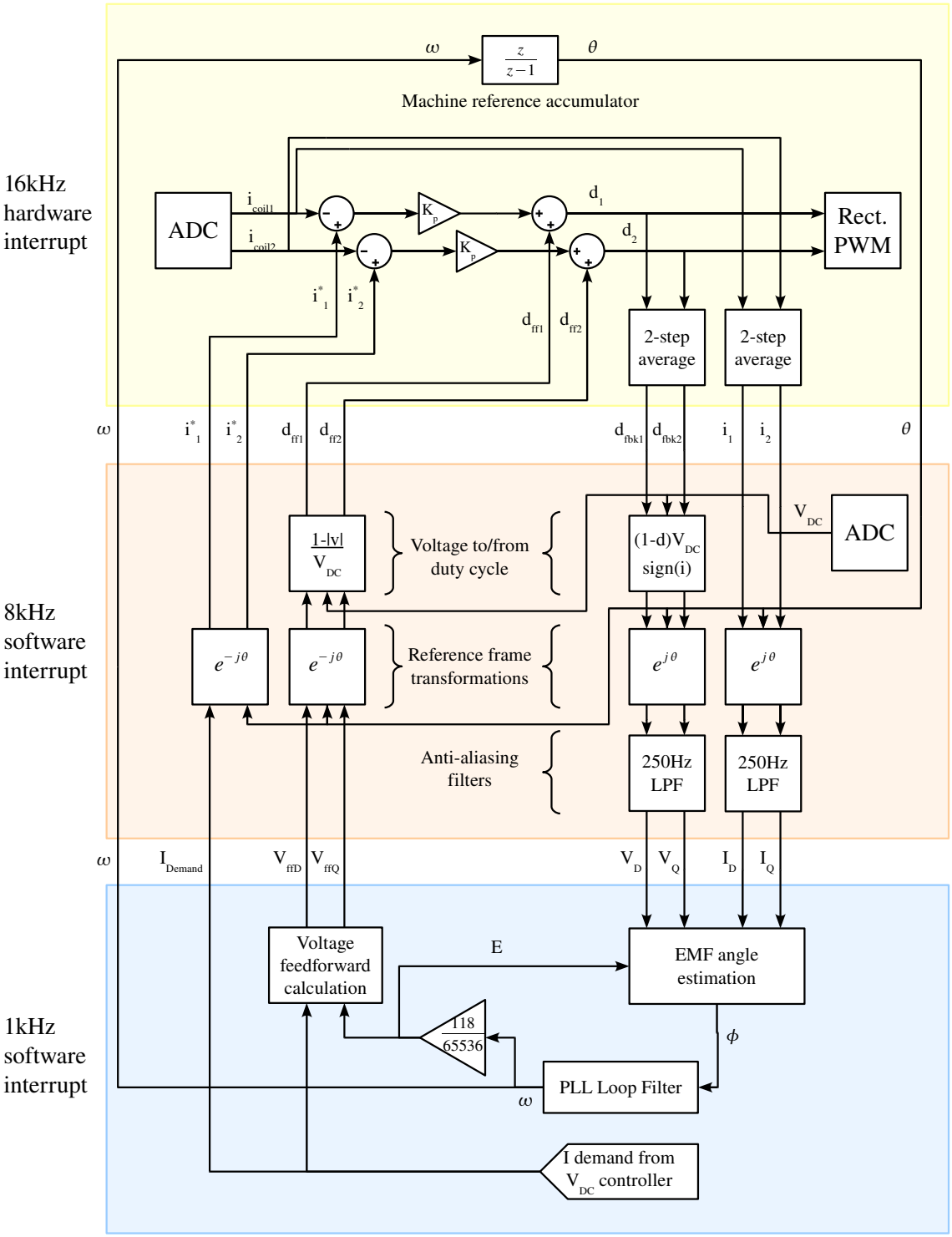


Figure 7.17: Structure of the rectifier controller.

The ADC is triggered to start conversion when the timebase counter of either module reaches zero, and record both coil currents. This happens at a rate of 32kHz. The hardware interrupt is triggered by the ADC after every other conversion, i.e. at 16kHz, which runs the ISR to control the coil current and increment the machine position reference accumulator. This is also shown in Figure 7.18. The ADC is set up to take measurements of each coil current at 32kHz, which are stored in registers. This means that at the time of the ISR there are two values of each variable, and an average is taken.

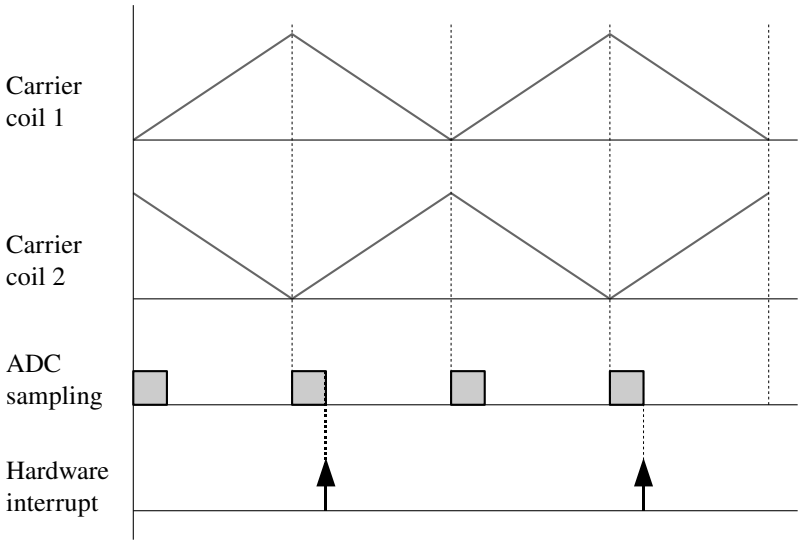


Figure 7.18: Rectifier PWM, ADC and interrupt timing.

PWM module 5 is used to drive the brake resistor, which is used to control the DC-link voltage when the coil current demand is less than zero. The microcontroller clock is not divided, and a time period of 1024 is used in a count-up mode, giving a PWM frequency of around 100kHz.

The ISR decrements the two software interrupt triggers, which run their software interrupts at one half and one sixteenth of the speed. The ISR also starts the ADC sampling the line current and DC-link voltage – this conversion does not trigger another hardware interrupt but the results remain in the ADC registers until required.

Software Interrupts and PLL Parameters

The output of the EMF estimation calculation is a 16-bit integer representing the error between the estimated and actual EMF, which is fed into the loop filter, which

is a PI-controller, as described in chapter 6. The output of the loop is the 32-bit machine reference angle step ω, which is added to the machine reference angle in the hardware ISR. This value is also multiplied by the calibration constant of 118/65536 to obtain the value E representing the machine frequency, which also represents the machine EMF magnitude.

The integrator in the PI controller is a simple backward difference accumulator, with the discrete transfer function $\frac{z}{z-1}$, and implemented as $integral_{k+1} = integral_k + input$, with the output as a 32-bit integer. The same system is used in the machine angle integrator, with the result being barrel shifted back to a 16-bit value. Due to the sampling rates of the different integrators, the PI-controller integrator has a gain of 1000, while the machine angle integrator has a gain of 16000, while the barrel shift represents a gain of 1/65536. This is shown in Figure 7.19, along with the variable types. Based on these gains, the proportional and integral gains of the PLL of 45 and 1000, calculated in chapter 6 for a 5Hz loop bandwidth, become 184 and 4 respectively in the microcontroller.

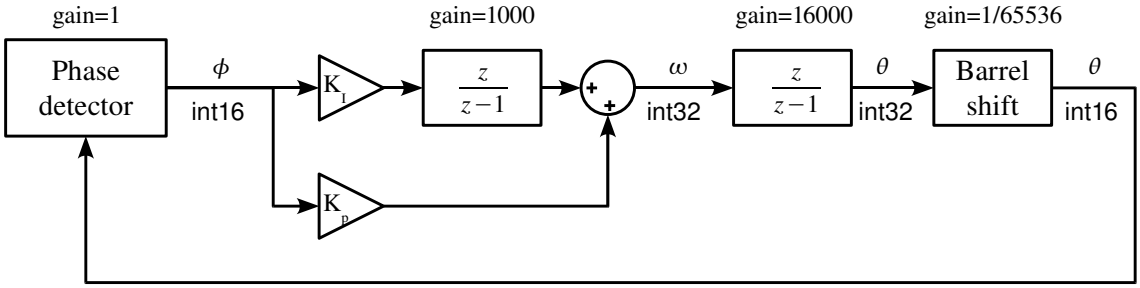


Figure 7.19: Phaselock-loop gains and variable types.

7.10.3 Inverter and DC-link Voltage Controller

Controlling the inverter can be divided into two sections: controlling the switching of the inverter, and synchronising the switching with the signals from the central controller. There is also a DC-link voltage controller, which is included in this section as it is synchronised to the grid frequency.

Inverter Switching

The two inverter legs are connected to PWM modules 1 and 2, which have a timebase frequency of 16 times the fundamental frequency, and govern the PWM component

of the inverter switching. These modules use the main clock divided by 4, in an up-down counting configuration. The fundamental component of the switching is governed by PWM module 6, in which the main clock is divided by 128, and a count-up configuration is used.

The same time period is used for all three PWM modules, which is the grid time period, so PWM modules 1 and 2 switch at 16 times the speed of PWM module 6. The phase relationship between PWM modules 1 and 2 and PWM module 6 is determined by the power module number, in order to achieve the phase relationship between modules described in Section 6.5.2. PWM modules 1 and 2 trigger an interrupt at 32 times the fundamental frequency, which is used to run the DC-link voltage controller routine.

During one grid frequency cycle of 20ms, the inverter controller cycles through four states, which determine how the inverter output is derived from the fundamental and PWM components. The states and transition times between states, as well as the rules determining the inverter output from the error duty cycle d, are given in Table 7.4.

State	Next state	Transition time	Fundamental output	PWM 1 output		PWM 2 output	
				$d \geq 0$	$d < 0$	$d \geq 0$	$d < 0$
0	1	t_1	0	d	0	0	$-d$
1	2	t_2	positive	1	1	0	$-d$
2	3	t_3	0	d	0	0	$-d$
3	0	t_4	negative	d	0	1	1

Table 7.4: Inverter output settings and states.

The state transitions are handled by a hardware ISR which is triggered by an interrupt that occurs when the PWM module 6 timebase hits it's comparator value, with the comparator value determined by the transition time. This ISR advances the inverter state, and loads the PWM module 6 comparator register with the next transition time. It also sets the duty cycles for PWM modules 1 and 2 to the appropriate values. The relationship between the inverter PWM modules and hardware interrupts is shown in Figure 7.20.

An interrupt is triggered when a message is received on the CAN bus containing the harmonic compensation error value. The resulting ISR determines the duty cycles for PWM modules 1 and 2 using the rules in Table 7.4, and applies them to the PWM modules. This ensures a minimum delay in setting the duty cycle.

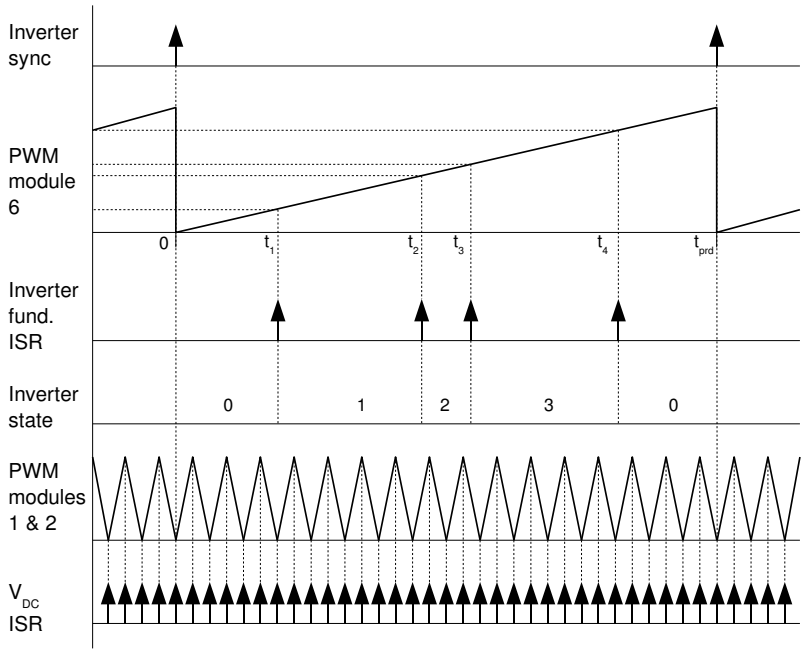


Figure 7.20: Inverter PWM and state transitions.

Inverter Synchronisation

A simple way to synchronise the inverter timebase, i.e. the PWM module 6 timebase, to that of the central controller is to have an ISR which runs whenever a synchronisation pulse is received. This ISR would load the time period value from the central controller into the period registers of PWM modules 1,2 and 6. It would then reset the counter of PWM module 6 to zero, and modules 1 and 2 to their given phase relationships.

This approach leads to a significant level of jitter in the module timebases, of around 100μs, for a number of reasons:

1. The point at which the DSPACE, used for the central controller, detects the zero-crossing of it's reference timebase is different from the actual zero-crossing point, due to the sampling interval of the program. This means that the time of the synchronisation pulse can differ from the actual zero-crossing by up to one sampling interval, which is 50μs for the 20kHz sampling used.

2. There is evidence that the DSPACE sends some CAN message frames twice, suggesting that the DSPACE CAN controller is not properly receiving the acknowledge bit from the modules, and re-sending the message frame. This will occur if the acknowledge bit is received too late, as the DSPACE is sending

the next bit. However, reducing the CAN bit rate to relax the bit timing constraints was found to have no effect. The modules will use the most recent synchronisation message, so the message could be delayed by one message frame, which is 53μs for the message size and bitrate used.

3. The high level of abstraction of the DSPACE hardware means that it is not known exactly when a message is sent, or the hardware and software processes which are involved behind the scenes. By contrast, the CAN controller on the TMS320F2808 microcontroller used in the modules provides a time stamp to show when a given message was transmitted or received.

The solution to problem 1 is to have the DSPACE send the modules the current value of it's timebase, as well as the required time period. The PWM module 6 timebase would then be set to this value rather than reset to zero. This still leaves problems 2 and 3, which are reduced by having the synchronisation ISR average the results of several synchronisation messages.

The timebase synchronisation ISR must also calculate the values of the switching times t_{1-4} for the inverter fundamental switching, as well as re-setting the inverter fundamental switching to state 0 if necessary. The switch-on angles for each module fundamental switching, are stored in an array in the module code, and are shown in Table 7.5. The angle is represented with the 0 to $2^{16}-1$ range of the unsigned 16-bit integer representing 0 to 2π radians.

Module Number	Switch-on angle
1	865
2	2615
3	4385
4	6180
5	8028
6	9942
7	11960
8	14110
9	16465
10	19124
11	22354
12	28482

Table 7.5: Inverter module switch-on times.

The switching angles for the other events are calculated according to Table 7.6,

which shows the switching angles for the asymmetric half-cycle switching scheme, as well as the classic switching scheme, which is also implemented to allow comparison between the schemes. In this table, θ_n is the switch-on angle for inverter module n, from Table 7.5, while N is the total number of modules.

Switching event	Asymmetric half-cycle switching	Classic switching
On positive	θ_n	θ_n
Off positive	θ_{N+1-n}	$2^{15} - \theta_n$
On negative	$2^{15} + \theta_{N+1-n}$	$2^{15} + \theta_n$
Off negative	$2^{16} - \theta_n$	$2^{16} - \theta_n$

Table 7.6: Switching angle calculation.

The comparator value for PWM module 6 is calculated as:

```
t_switch=((long)angle_switch*(long)timebase_period)>>16;
```

An array is also included in the microcontroller code containing the switching angles for an 11-module system, which are used when one inverter module fails.

DC-Link Voltage Control

Control of the DC-link voltage is carried out in an ISR triggered by PWM modules 1 and 2, at 32 times the grid frequency. The measured DC-link voltage is filtered using a 32-step averaging filter, which will remove the grid frequency ripple and higher harmonics. As the PWM modules are synchronised to the grid frequency, the filter will always remove the ripple as required, even if the grid frequency changes.

The DC-link voltage demand, sent over the CAN bus by the central controller, is subtracted from the filtered DC-link voltage and the resulting error used to drive a PI controller. The output of the PI controller is a current demand. If the current demand is positive then it is used to set the rectifier current demand, if it is negative then it is used to set the brake resistor duty cycle, via a gain. The PI controller parameters and the brake resistor gain are both tuned through a trial and error process.

7.10.4 Communications Functions

Modbus communications are handled by a function in the idle loop of the microcontroller, which is run continuously when other functions are not running. The

serial interface of the microcontroller has a 16-byte buffer, and the Modbus function continuously checks for data in the buffer, moving it to an area of memory when it is found. The Modbus function has to store the entire Modbus message frame, of up to 256 bytes, before acting on it. When the end of message character is received, the message frame is interpreted according to the Modbus Serial protocol [53].

The Modbus function implements the Modbus function codes for reading and writing integer data. The tables of data defined in the Modbus specification do not exist physically within the microcontroller memory space, instead they are implemented as an array of pointers to global variables within the memory space. This is shown in Figure 7.21. If a table entry needs to be accessed, the address is looked up from the variable address register.

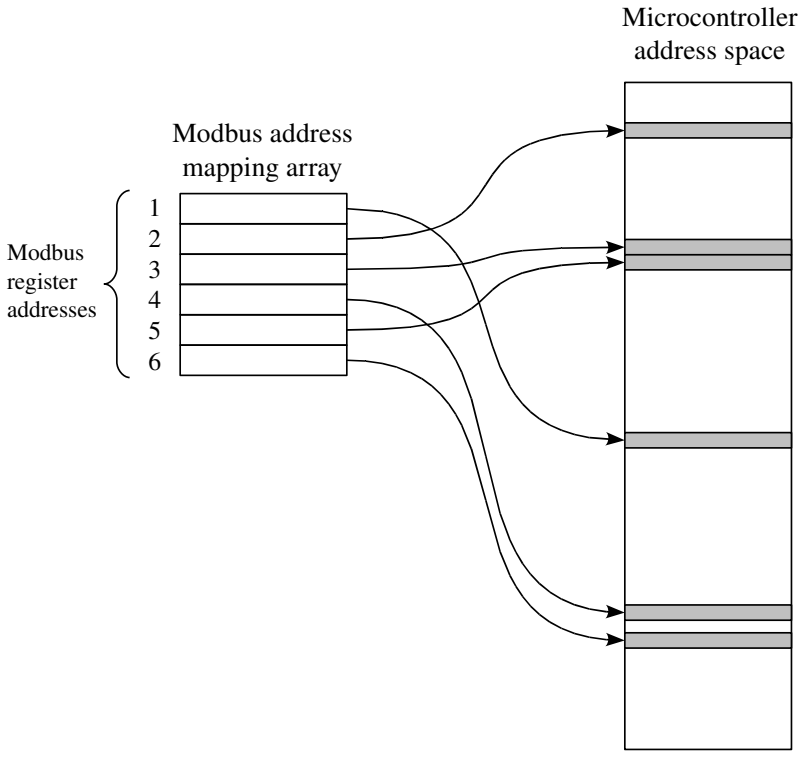


Figure 7.21: Mapping of Modbus table entries to microcontroller memory space.

Separate address registers are implemented for read-write and read-only variables, defined as holding registers and input registers in the Modbus specification. All the variables chosen to be accessible via the Modbus interface are mapped to the input registers table, and the read-write registers are also mapped to the same position in the holding registers table, with the gaps taken up by pointers to an un-used memory location.

A system is also implemented for storing data in a buffer and sending it to the host PC. This is useful where the sampling rate required is faster than that available with the Modbus interface (around 100 data frames/s). A function can be placed anywhere in the microcontroller code, giving two values to be recorded. When recording is activated, by setting a bit in a control register, every time the function is run the values will be recorded. When the buffer is full, the record bit will be unset, and the host PC can download the contents of the buffer using the Modbus file access function.

7.11 Conclusions

A test system has been designed and built to test the concepts outlined in previous chapters. Two 2.5-kW axial flux generators are used in place of a larger lightweight iron cored generator of the type described in previous chapters, and the generators provide 24 coils in total, allowing 12 power modules, each connected to two coils.

Inverter and rectifier control will be tested, along with fault tolerance for module failure. Due to the difference in the test generators and the generator proposed for the application, control issues relating to airgap eccentricity cannot be investigated, nor can issues relating to having a high voltage output and mounting the modules on the generator structure.

The modules are designed to fit into a eurocard subrack, with a length of 220mm and a height of 100mm, which can be easily removed for access. A separate power and control board is used, in order to allow the control board to use a 4-layer PCB, which is necessary to supply power to the microcontroller. The microcontroller used is the TMS320F2808 from Texas Instruments, chosen for the flexibility of the peripheral functions.

The module power boards use surface mount transistors, with the PCB area acting as the transistor heatsink. This was done in order to reduce the system complexity and cost, and allow easy replacement of the transistors. Analysis of a prototype module under full-load conditions using a thermal imaging camera show that the cooling behaves as predicted, although force cooling of the module rack is desirable.

Synchronisation of the modules with the central controller will be carried out

over a CAN bus, a communication bus designed for automotive use but also finding use in factory automation systems. CAN offers a low latency and high speed, as well as a message priority system, and a CAN controller is built into the microcontroller selected for the project. Communication with a host PC will be via the Modbus protocol, over an RS485 serial bus, as the microcontroller features a serial interface, and RS485 interfaces are easily available for PCs. These interfaces are optically isolated on the module control board, between the microcontroller and the bus transceivers.

Central control and synchronisation of the modules is carried out using a DSPACE rapid control system development unit. The grid voltage is measured, and a message frame is sent to the modules a set time delay after the voltage zero-crossing, with the time delay determining the inverter real power output. The modules then synchronise their internal inverter timebases with this message frame.

A DC-link voltage demand is also sent to the modules, which control the rectifier current demand and the brake resistor so that the average DC-link voltage over one cycle tracks the demand. The module DC-link voltage determines the inverter voltage magnitude, determining the inverter reactive power.

The software on the microcontroller modules is written in C, using the DSP/BIOS real time operating system, which allows multi-threading applications to be written. Control of the rectifier and inverter is divided across a number of hardware and software interrupts, running at different rates and with different priorities.

Testing of this system, and the control systems developed, will be described in the next chapter.

Chapter 8

Testing of the Basic Control System

In this chapter, the basic control system is that described in chapter 6, with the addition of the fault tolerance aspect of the loss of a module. Overall turbine control is not considered as it has been studied extensively, but the dynamic aspects of the control system are of interest, particularly the tracking of the changing machine speed.

The loss of a module, and the need to quickly increase the DC-link voltage and change the module switching times, has not been considered so far, and will be investigated in this chapter. Also not considered so far is how the rectifiers will initially lock on to the coil EMF, as they do not have sensors for the coil voltage, only the current.

The following functions of the test system need to be tested:

- Control of the rectifier coil current using the proportional controller and feed-forward arrangement, at a number of machine speeds and coil current demands.
- Estimating and tracking the coil EMF, in a steady state and with a changing machine speed.
- Locking on to the coil EMF, and tracking the EMF when the current demand is zero.
- Controlling the DC-link voltage, including the reaction to step changes in voltage demand and inverter current output, at a number of operating conditions.

- Implementation of the inverter system using the central controller and distributed timebases, and testing with a loadbank output and grid connection.
- Analysis of the power sharing between modules using the classic switching scheme, and the switching scheme designed for equalised power sharing.
- Analysis of the inverter output voltage harmonic distortion due to the fluctuating DC-link voltage, and the correction of this distortion using the active filtering method devised.
- The ability of the system to react to, and compensate for, the loss of a single module, by raising the DC-link voltage of all remaining modules and changing the switching instances of the modules.

8.1 Rectifier Current Control

All rectifier testing involves using a single module connected to the motor-generator test rig, and a resistive load on the DC side. Coil current is measured using an oscilloscope, and the coil voltage is measured for a coil in phase with the coil connected to the module, in order to obtain an estimate of the coil EMF.

The test module is connected to a PC using the RS485 interface, for control and monitoring purposes. The motor drive is also connected to the PC in order to allow the motor speed to be controlled to follow a set speed profile. The test setup is shown in Figure 8.1.

Testing of the rectifier current control system was carried out at several operating conditions, which are listed in Table 8.1. The inverter output of the module was set to output DC into the load resistor, and the DC-link voltage controller was set to maintain the voltage at 27.1V, that being the required voltage for a 230V output with a 12-module inverter. The generator speed was set, and the load resistor adjusted to achieve the desired coil currents.

The coil current and EMF are shown in Figure 8.2a for the 12m/s operating condition, with the zero-crossing region shown in greater detail in Figure 8.2b, and correspond well with the simulated current. A fast Fourier transform of the coil current was calculated using the oscilloscope, and is shown in Figure 8.2c, where small third and fifth harmonics can be seen.

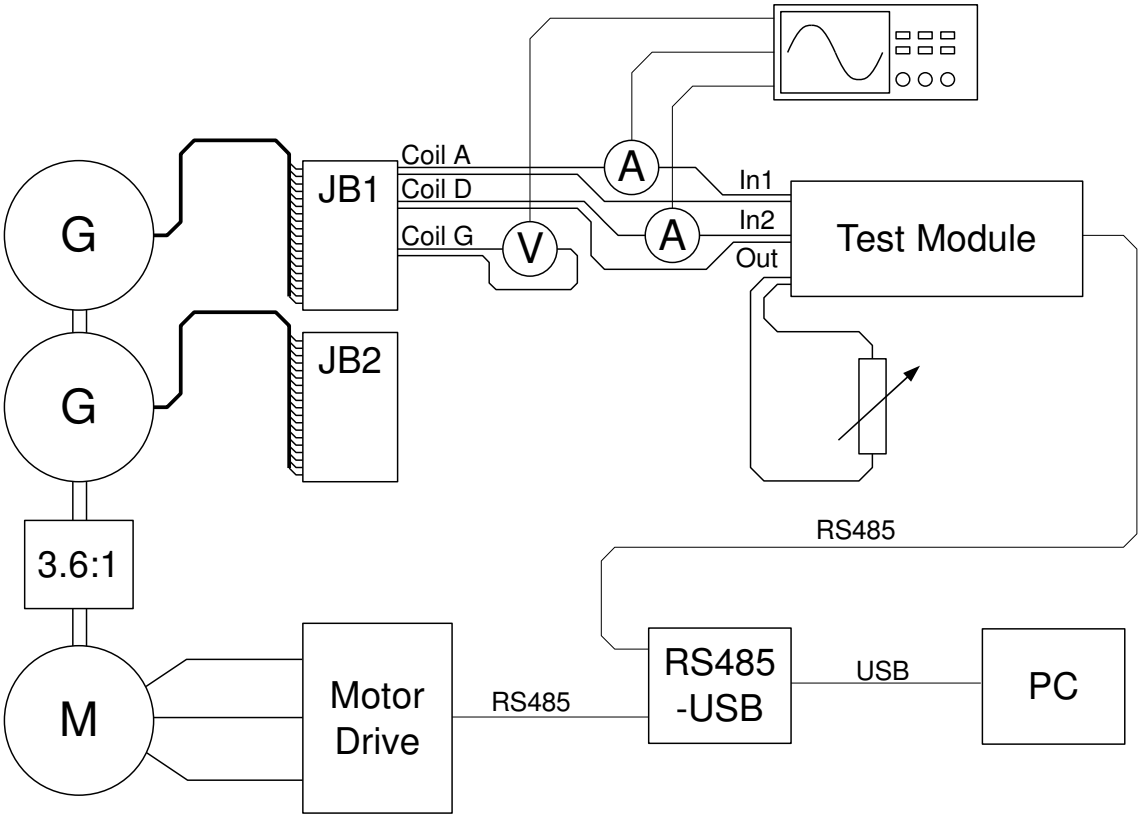


Figure 8.1: Rectifier test arrangement.

Wind Speed (m/s)	Generator Speed (rpm)	Machine EMF (V rms)	Coil Current (A rms)
3 (cut in)	93	5.35	0.25
6	142	8.17	1.5
9	213	12.26	3.4
12 (rated)	290	16.69	6.2

Table 8.1: Turbine operating conditions for rectifier testing.

The coil current and EMF are shown in Figure 8.2d for the minimum power case, with zero crossing shown in greater detail in Figure 8.2e and FFT in Figure 8.2f. Significant third and fifth harmonics are present in the current waveform, which is at the boundary of discontinuous conduction. The coil current is the minimum achievable – a lower current demand will not result in a change in current drawn, and the RMS current is around 500mA, which is higher than that required for the minimum power operating condition.

Coil currents and EMFs along with the FFTs are shown for the 6m/s and 9m/s operating conditions in Figure 8.3. The level of third and fifth harmonics are significantly lower than the 3m/s condition, but higher than the 12m/s condition, and the harmonic levels for all conditions are summarised in Table 8.2.

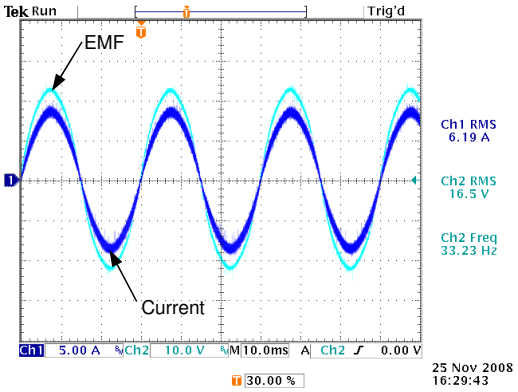
Wind Speed (m/s)	Fundamental Current (A)	Harmonic Current ratio	
		3rd	5th
3	0.392	0.27	0.077
6	1.41	0.085	0.043
9	3.0	0.053	0.040
12	5.76	0.028	0.021

Table 8.2: Coil current harmonic to fundamental ratios.

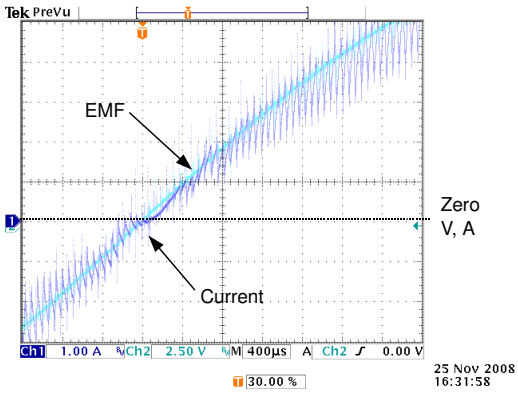
Further measurement of the coil inductance shows that the inductance at higher frequencies is significantly lower than that at lower frequencies. The value of inductance used in all calculations so far is the value at 50Hz, and the value at 10kHz is almost half of that, leading to a greater high frequency ripple current and a higher minimum current. The inductance at 10kHz was also found to vary significantly with the machine rotor position, reaching a minimum when the magnets are aligned with the coil, and a maximum when they are unaligned. This could account for the large harmonic currents at low current demand, where the high frequency ripple current is large compared with the fundamental current. The variation of inductance with magnet alignment is given in Table 8.3.

Frequency (Hz)	Inductance (μH)	
	Aligned	Unaligned
50	452	457
10,000	223	295

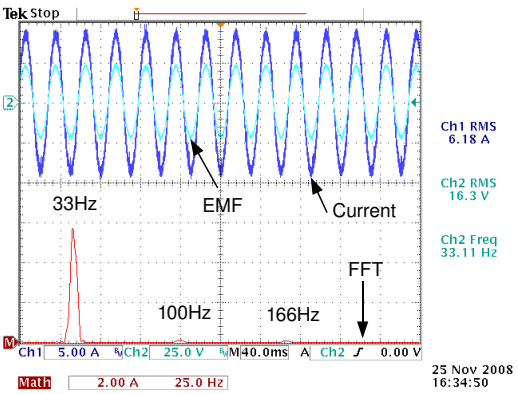
Table 8.3: Coil inductance variation with magnet alignment.



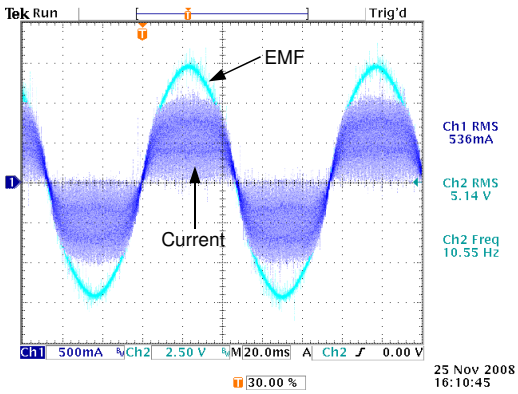
(a) 12m/s coil current and EMF.



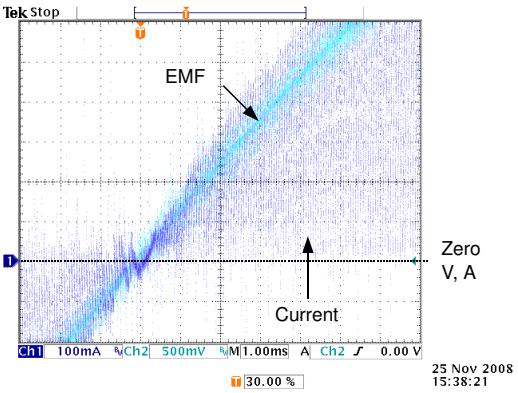
(b) 12m/s coil current and EMF at zero-crossing.



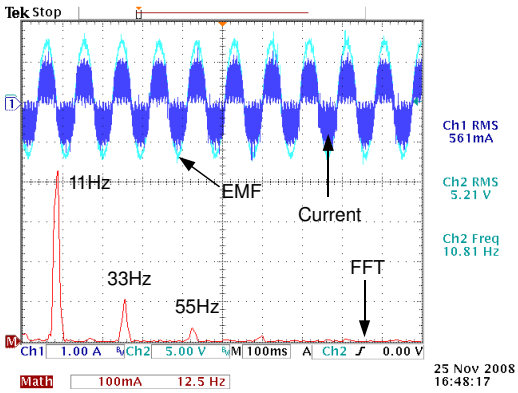
(c) 12m/s coil current FFT.



(d) 3m/s coil current and EMF.

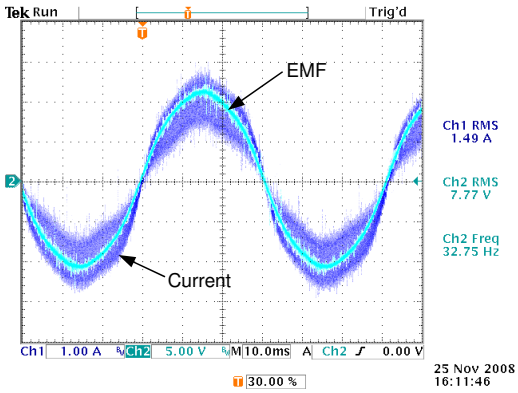


(e) 3m/s coil current and EMF at zero-crossing.

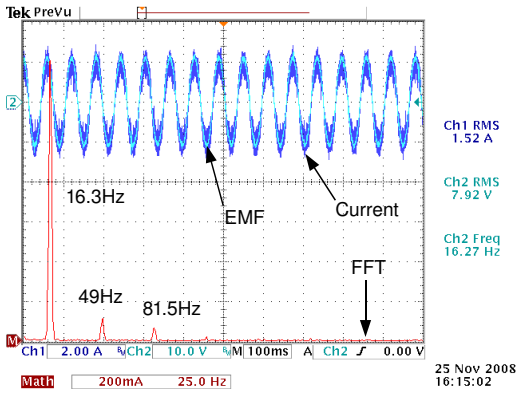


(f) 3m/s coil current FFT.

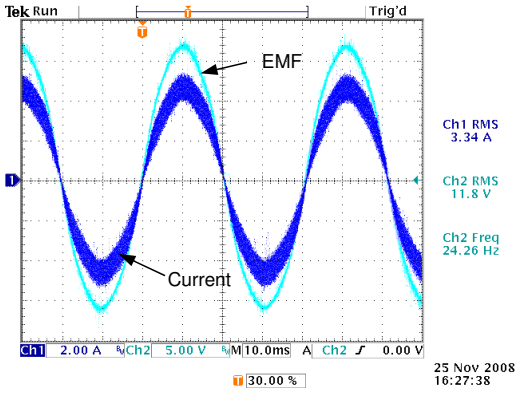
Figure 8.2: Coil current and EMF at 12m/s and 3m/s wind speed conditions.



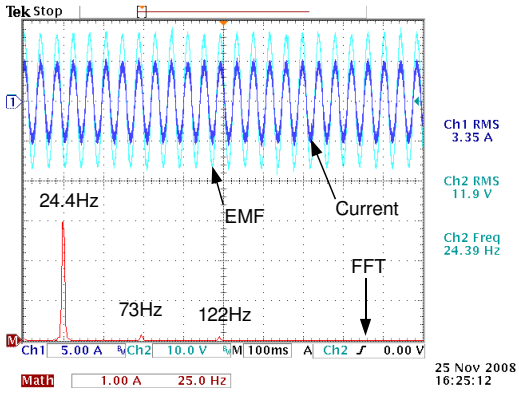
(a) 6m/s coil current and EMF.



(b) 6m/s coil current FFT.



(c) 9m/s coil current and EMF.



(d) 9m/s coil current FFT.

Figure 8.3: Coil current and EMF at 6m/s and 9m/s wind speed conditions.

8.2 Machine EMF Estimation and Tracking

Testing of the steady state EMF tracking performance was carried out at the 12m/s and 3m/s wind conditions. Coil currents were measured on an oscilloscope, while the estimated EMF in the rotating reference frame and estimated speed were obtained from the module under test. Tracking results are shown in Figures 8.4 and 8.5.

The estimated EMF and speed in both cases show a sinusoidal fourth order harmonic ripple, in contrast to the spikes seen in the simulated 12m/s case.

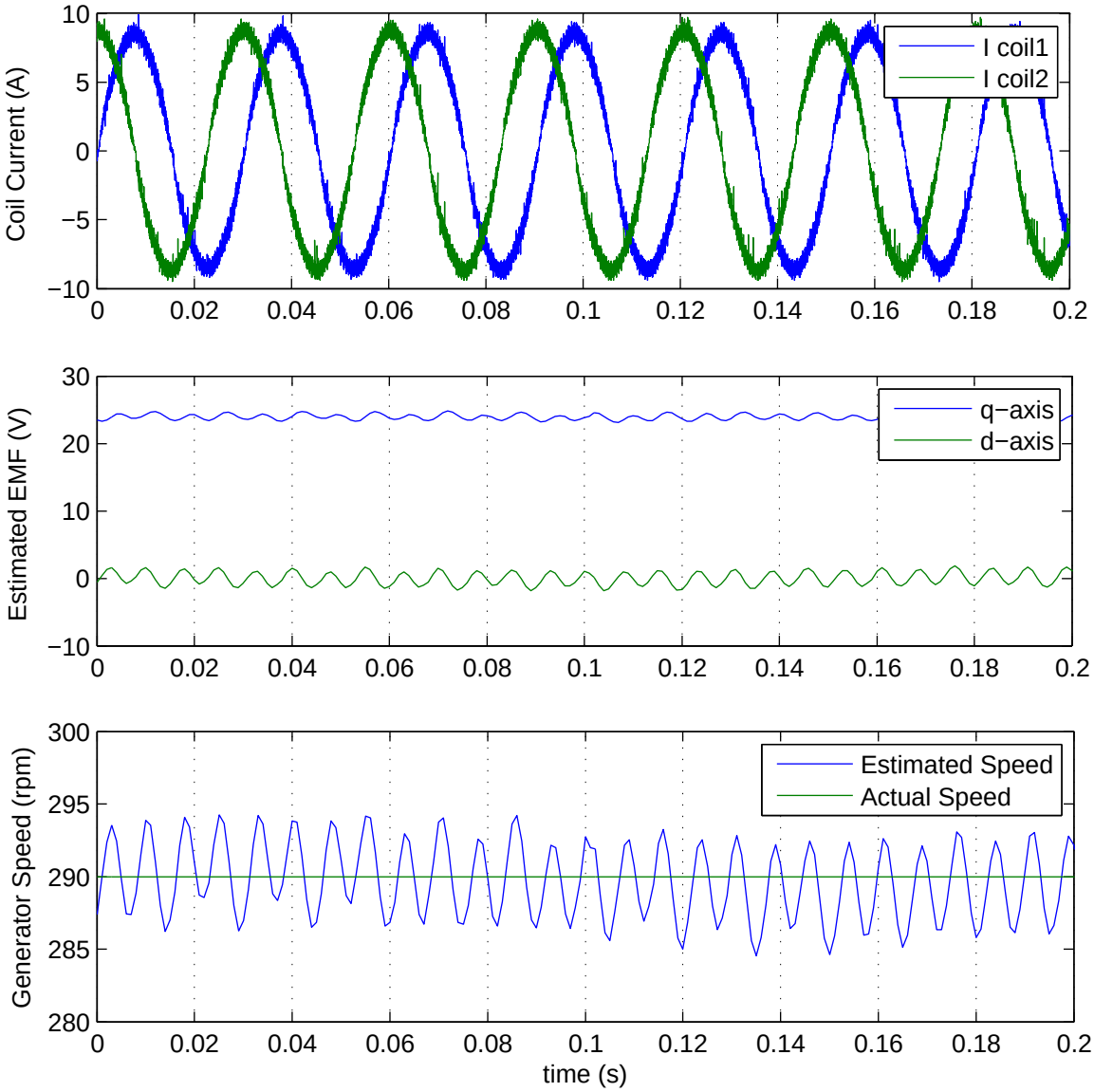


Figure 8.4: Steady state EMF tracking at 12m/s wind condition.

Measurement of the transient performance of the speed estimation during operation is limited by the dynamics of the drive system. A step change in speed demand

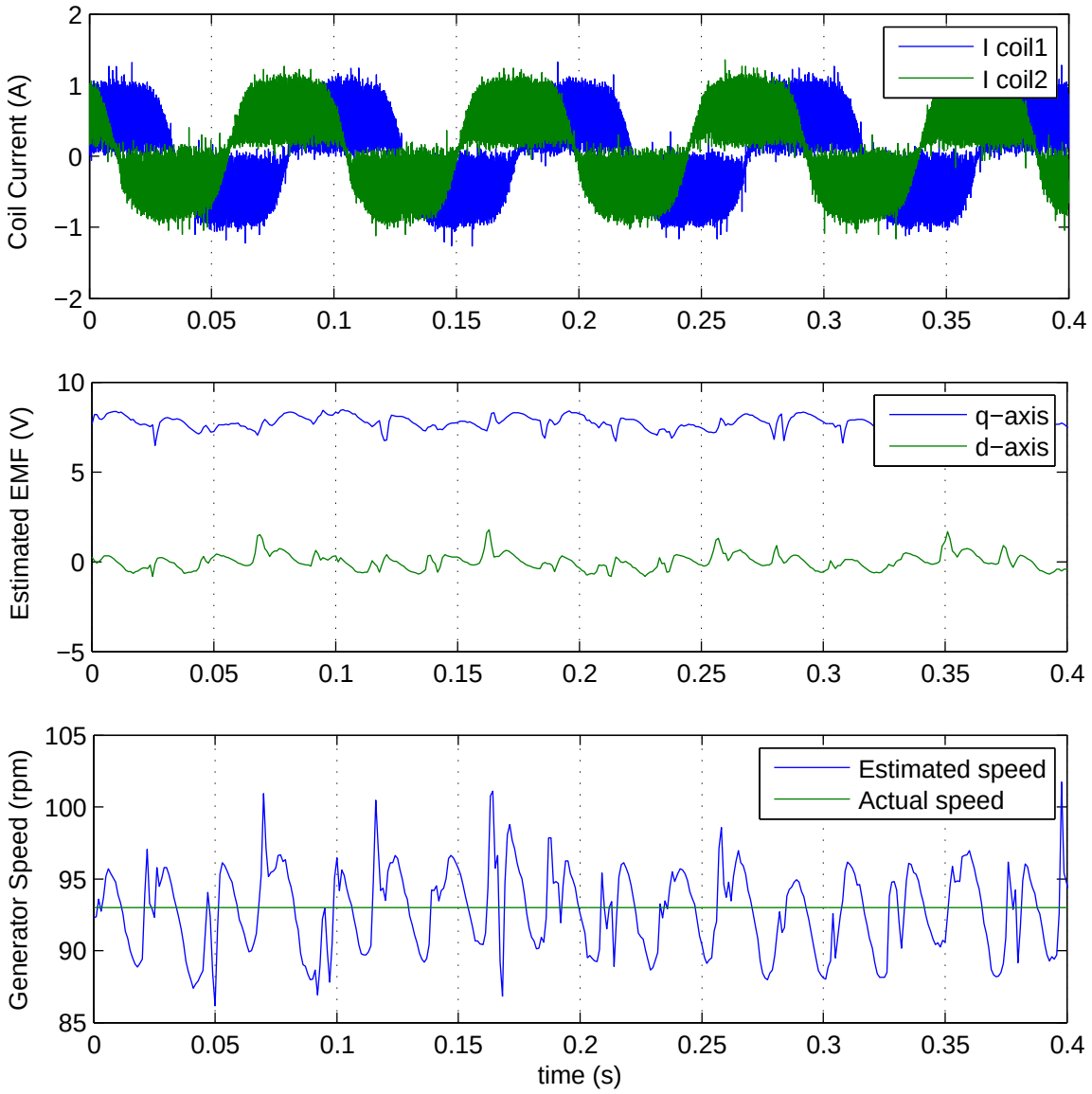


Figure 8.5: Steady state EMF tracking at 3m/s wind condition.

was given to the drive, with the ramp speed set at 5s, and the speed measured by the drive and speed estimated by the EMF tracking loop recorded. Two measurements were taken, at the 3m/s wind condition, with a step from 93rpm to 120rpm speed, and the 12m/s condition, with a step from 250rpm to 290rpm. Results are shown in Figures 8.6 and 8.7. It is clear that the EMF tracking loop is able to track the generator speed at a rate faster than the dynamics of the drive system.

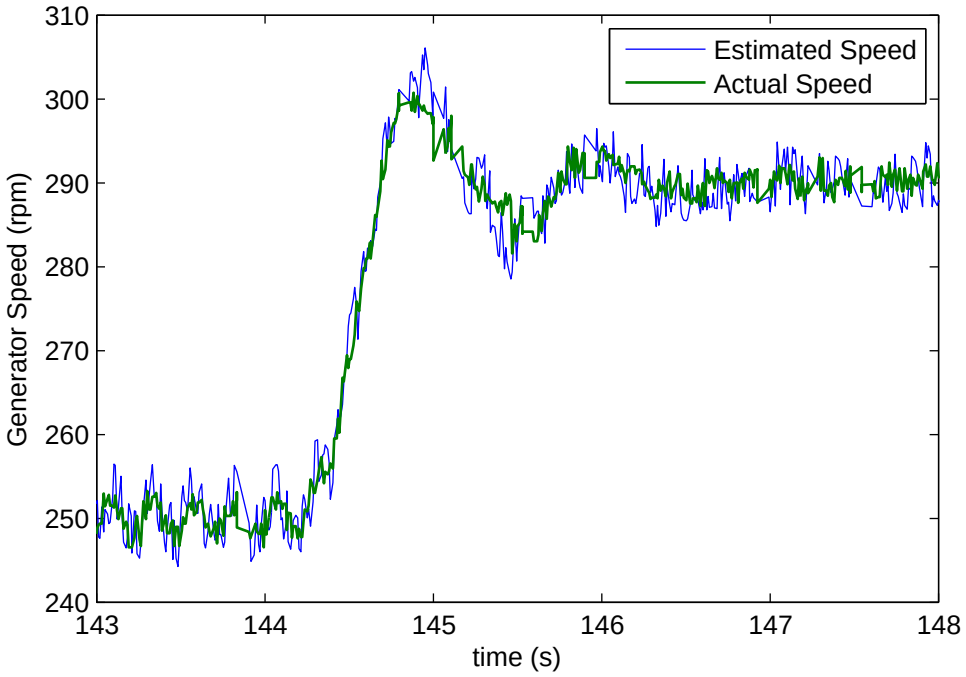


Figure 8.6: Response to a step change in speed demand, 12m/s wind condition.

8.3 Machine EMF Position Acquisition, and Rectifier Startup

EMF position acquisition was not covered in chapter 6, as the simulations assumed that the machine position estimator was already locked, and that current was being drawn. As the module is not equipped with coil voltage sensors, as a cost saving measure, there is no way to measure the coil voltage without drawing a current.

A method to determine the voltage is to provide short pulses of constant length to the rectifier MOSFETs, briefly shorting the coil terminals. While the MOSFETs are switched on the current will be governed by Equation 8.1, and if the coil resistance is ignored then the EMF can be found by finding the rate of change of current [46].

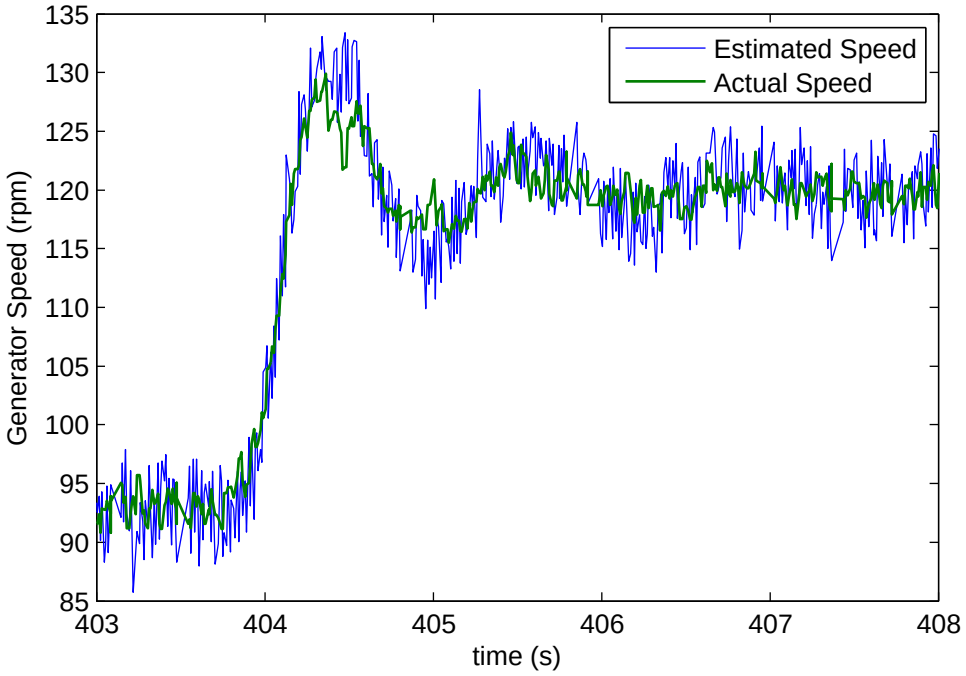


Figure 8.7: Response to a step change in speed demand, 3m/s wind condition.

If the current increases linearly, then the rate of change of current can be found from the final current at the end of the applied pulse.

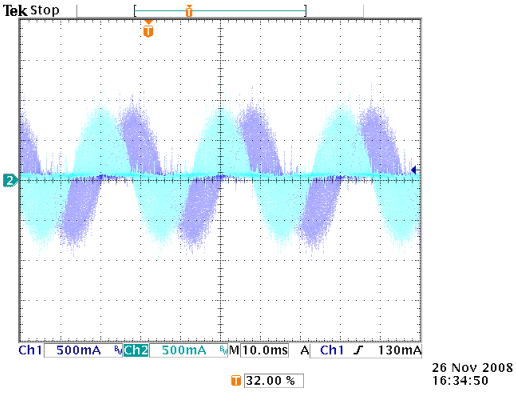
$$e + iR + L\frac{di}{dt} = 0 \tag{8.1}$$

In reality only the position of the EMF is required, so the coil currents at the end of the applied pulses are recorded, and used instead of the estimated EMF as the input to the phaselock loop (PLL). The pulses must be short enough that the current has a chance to reduce back to zero before the next pulse occurs, or continuous conduction will occur and a large current will be drawn. This system is used whenever the rectifier current demand is negative, with the excess power being dissipated in the brake resistor.

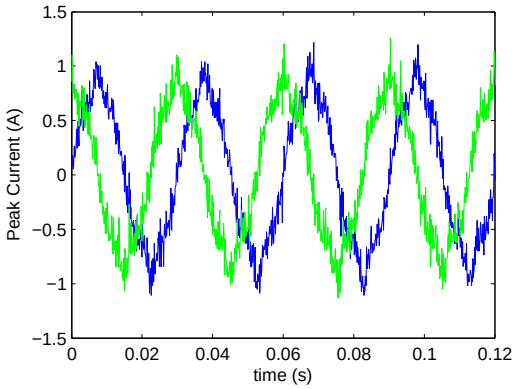
Examples of the currents in both coils, along with the peak currents measured by the microcontroller, are given in Figure 8.8, for the 290rpm rated speed and the 93rpm minimum speed. The measured currents have a high level of noise, especially at low speed, but the machine angle PLL is able to lock on to the signal.

Acquisition of a signal by a PLL can occur in several different ways [57]:

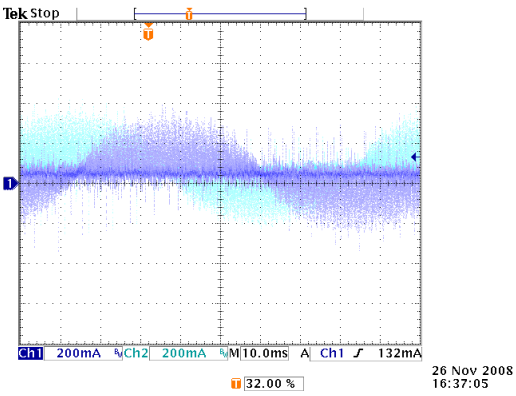
- If the signal is of a similar or smaller bandwidth than the loop bandwidth, then the loop will immediately lock onto the signal within a single cycle.



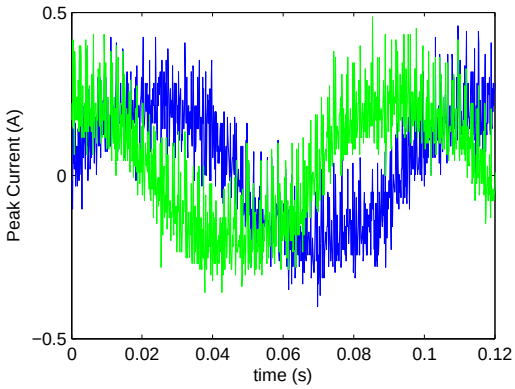
(a) Acquisition coil current, 290rpm.



(b) Measured peak current, 290rpm.



(c) Acquisition coil current, 93rpm.



(d) Measured peak current, 93rpm.

Figure 8.8: EMF acquisition using coil current sensors.

- If the signal is at a higher frequency than the loop bandwidth, the loop will still have a tendency to wander towards the signal frequency until it is close enough for the first method to occur.
- If the signal is at a much higher frequency than the loop bandwidth, the loop will not wander towards the signal frequency. In this case the loop can be programmed to perform a frequency sweep to locate the signal frequency.

It was assumed in development that as the loop has a relatively low bandwidth of around 5Hz, it will not immediately lock on to the machine speed in any of the conditions listed in Table 8.1. However it was found that the loop locked on to the machine speed immediately in all cases apart from the rated speed case, where some slipping occurred. These are shown in Figure 8.9. The theoretical step response from chapter 6 is also given, and the individual step responses show a strong correlation.

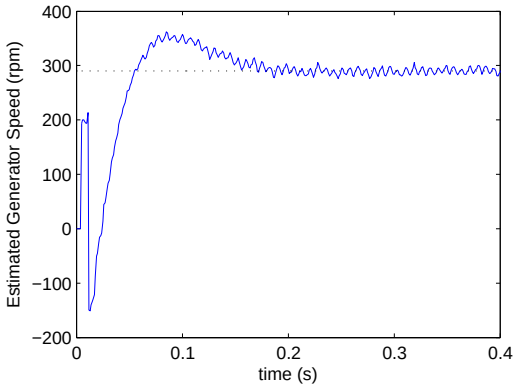
8.4 DC-Link Voltage Control

8.4.1 Steady State Testing

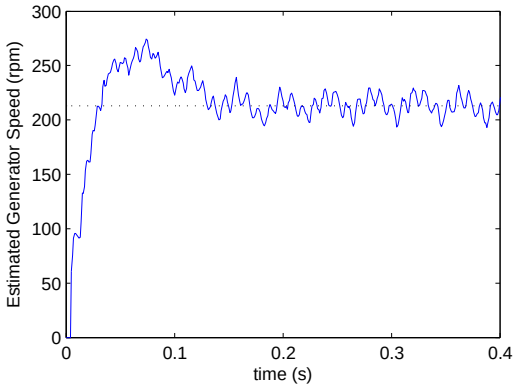
Steady state testing of the DC-link voltage control system was carried out in order to verify the operation of the signal filter, which must prevent the ripple in the DC-link voltage from causing a corresponding ripple in the rectifier current demand. Testing was carried out at the rated power condition, as this gives the largest voltage ripple.

To achieve a sinusoidal current waveform, and thus a DC-link voltage ripple representative of normal usage conditions, the complete inverter of 12 modules was used. The inverter was connected to a loadbank, and the load resistance increased until the rated output current was achieved. The DC-link voltages of modules 2, 4 and 6 were recorded on an oscilloscope, along with the inverter output voltage and current, and an FFT of the DC-link voltage was also calculated.

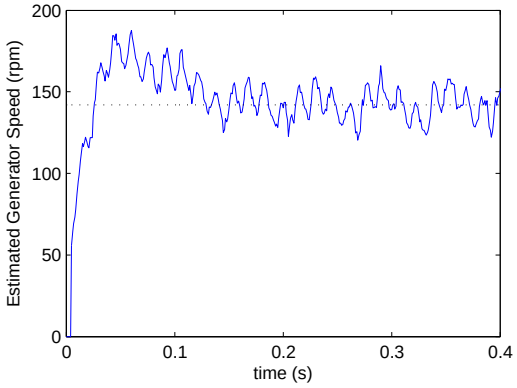
The DC-link voltage recorded by the module controller was obtained, along with the filtered DC-link voltage. These are shown in Figure 8.10. The different modules, each having a different switch timing, produce a DC-link voltage ripple with different harmonic contents, but the harmonic filter in the DC-link voltage controller appears to be effective.



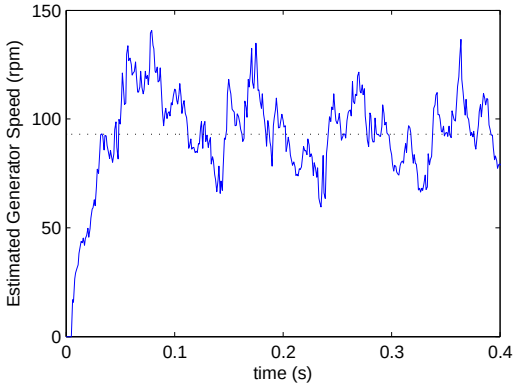
(a) PLL acquisition at 290rpm.



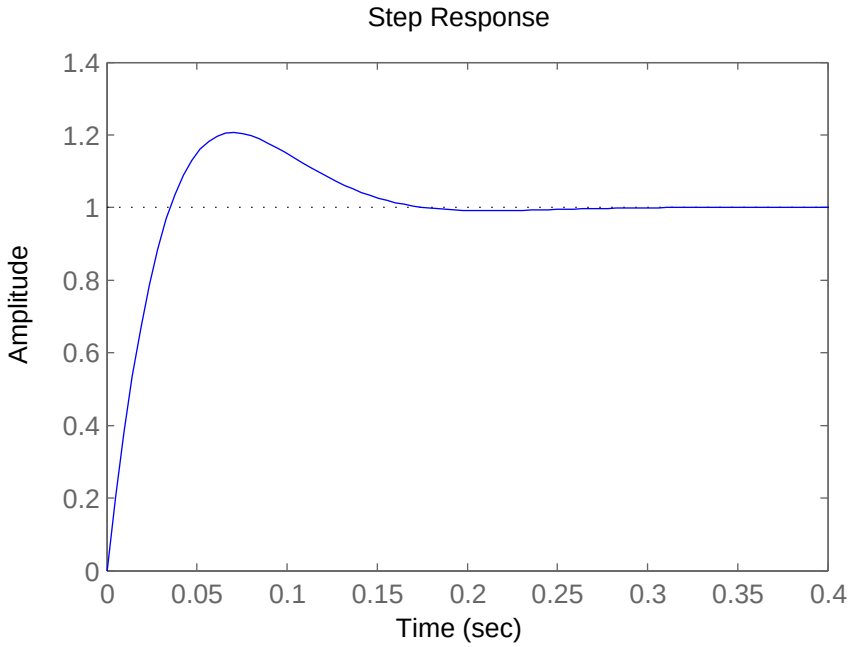
(b) PLL acquisition at 213rpm.



(c) PLL acquisition at 142rpm.

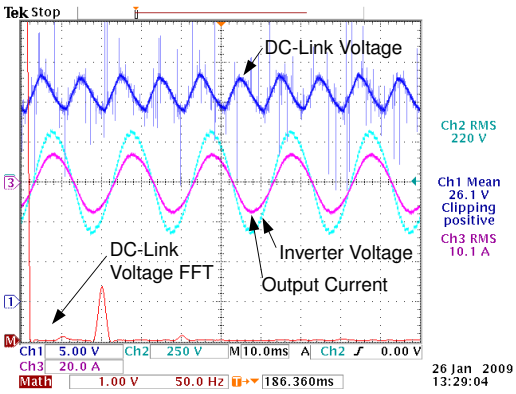


(d) PLL acquisition at 93rpm.

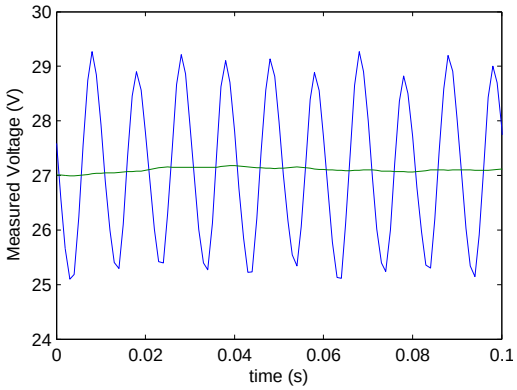


(e) Theoretical step response of PLL system.

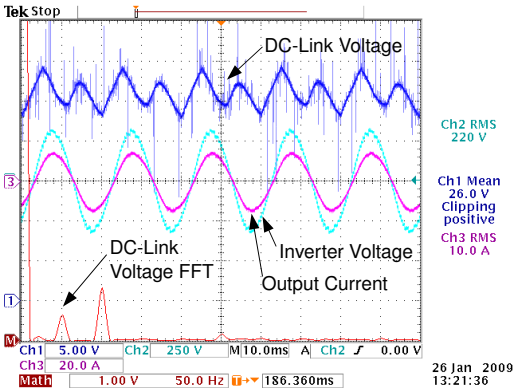
Figure 8.9: PLL acquisition of the generator speed.



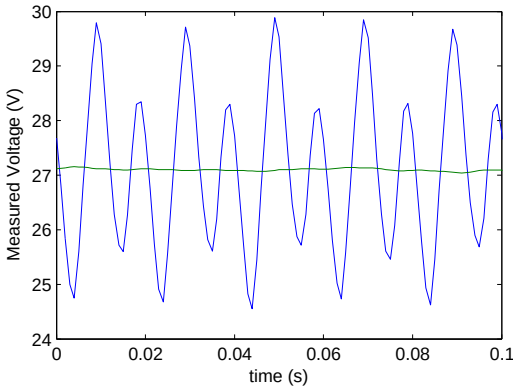
(a) DC-link voltage, module 6



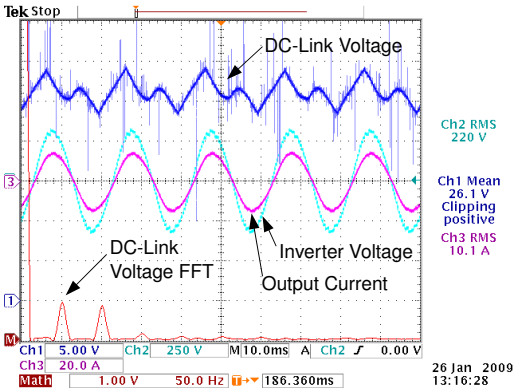
(b) Measured and filtered DC-link voltage, module 6



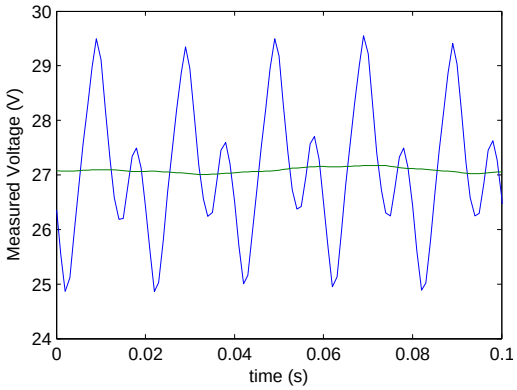
(c) DC-link voltage, module 4



(d) Measured and filtered DC-link voltage, module 4



(e) DC-link voltage, module 2



(f) Measured and filtered DC-link voltage, module 2

Figure 8.10: DC-link voltage controller steady state performance

The levels of the different harmonics of the output frequency in the DC-link voltage are shown in Table 8.4. As significant harmonics other than just the second are present, the use of an averaging filter rather than a simpler 100Hz notch filter is justified. The odd numbered harmonics are due to the inverter switching pattern of the modules being asymmetrical.

The high levels of fundamental frequency ripple in the lower numbered modules could be a cause for concern, as the lower frequency will increase the losses in the DC-link capacitor, leading to a shorter capacitor lifetime than calculated in chapter 4.

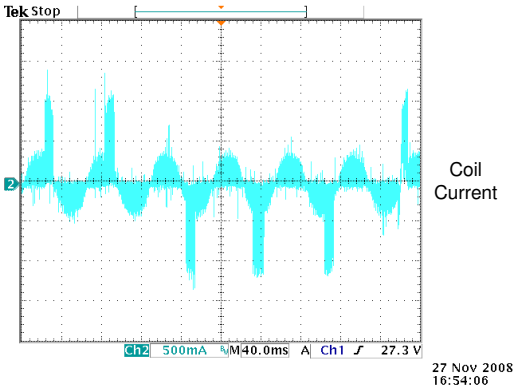
Harmonic number	Harmonic Voltage (V RMS)		
	Module 2	Module 4	Module 6
fund	0.96	0.66	0.12
2	0.88	1.34	1.38
3	0.15	0.06	0
4	0	0	0.14
5	0	0.18	0

Table 8.4: DC-link voltage harmonic content

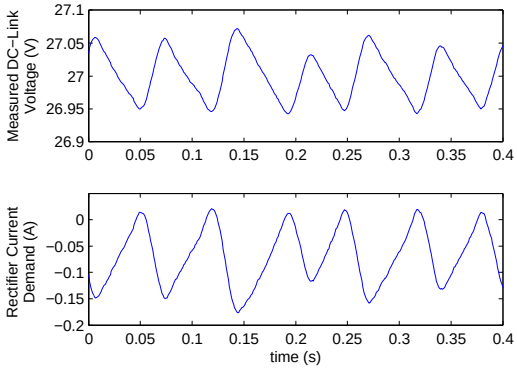
8.4.2 Operation With Low Inverter Output Current

If the rectifier current demand is less than zero then the EMF tracking system of Section 8.3 is used, and the negative demand is sent to the brake resistor to control the DC-link voltage. When the current demand drops below the minimum current, determined by the limits of continuous conduction, it is no longer possible to control the coil currents, which remain at the minimum value until the demand reaches zero, and the rectifiers are set to the EMF tracking mode.

The minimum current means that there is a deadband in the current control system, followed by a discontinuity, which can lead to control issues if the system is operated close to this region. This is shown in Figure 8.11, where the oscilloscope measurement in Figure 8.11a was measured at a different time to the demand in Figure 8.11b. It can be seen that the deadband in the current demand response causes the current demand to oscillate, spending most time in the EMF tracking mode and switching briefly into the full conduction mode when the current demand rises above zero. In full conduction the voltage rises rapidly, causing the current demand to quickly drop below zero again.



(a) Coil current at low current demand



(b) DC-link voltage and current demand at low current demand

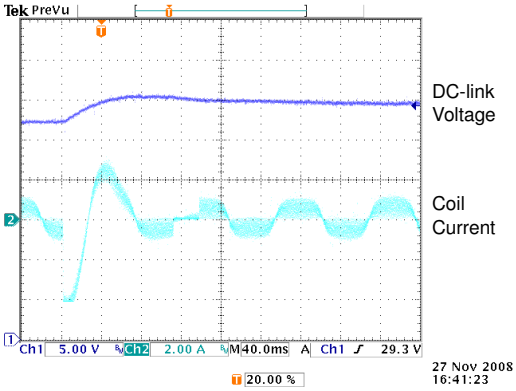
Figure 8.11: Low current demand condition, steady state

This rapid switching between the EMF tracking and full conduction modes can cause trouble with maintaining a lock on the machine EMF. This could be improved by calibrating the EMF measured in the EMF tracking mode so that it is equal to the actual EMF, rather than just proportional to it, which would prevent the discontinuities in the estimated EMF whenever the modes switch.

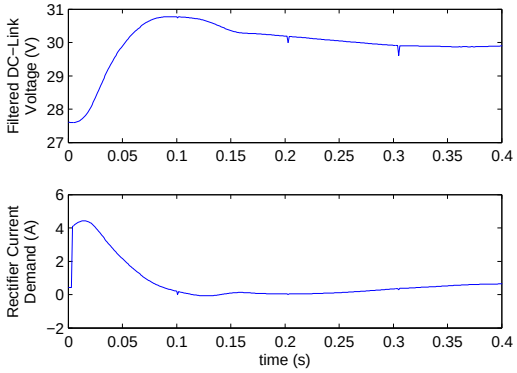
8.4.3 Voltage Demand Step Response

The step response of the DC-link voltage controller was tested using a single module and resistive load, by stepping the voltage demand from 27.1V to 29.6V, this being equivalent to the step required upon the sudden loss of one module. At the same time as the step was initiated, the microcontroller was told to start recording the filtered DC-link voltage and current demand from the voltage controller. The oscilloscope was used to record the DC-link voltage and coil current, and was triggered by the step in voltage.

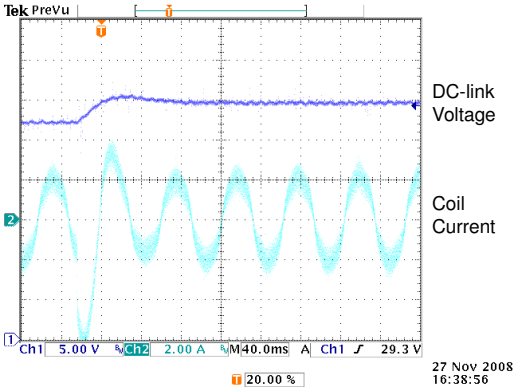
Results are shown in Figures 8.12 and 8.13. The simulated DC-link voltage controller response is also shown in Figure 8.13 for reference, and a strong correlation with the measured responses can be seen. The filtered voltage in the 3m/s wind speed operating condition shows a slightly different response, this is due to the rectifier current demand dropping below the minimum value – at this point the current demand has no effect until it drops below zero.



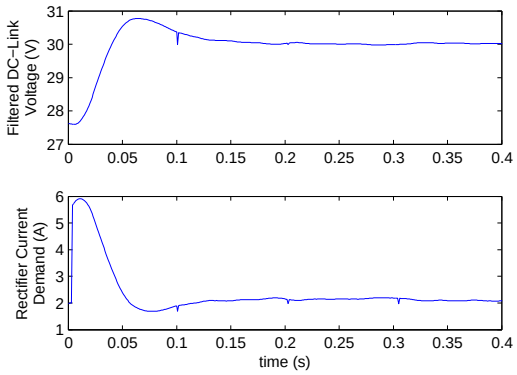
(a) DC-link voltage step, 3m/s condition



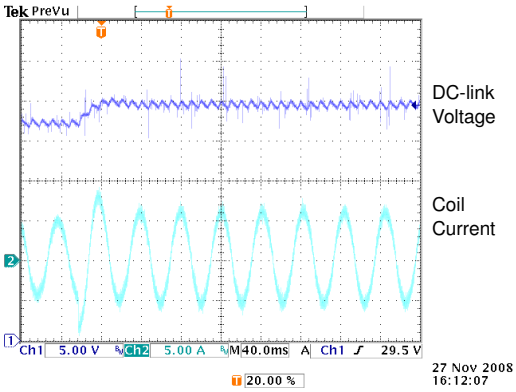
(b) Filtered DC-link voltage and current demand, 3m/s condition



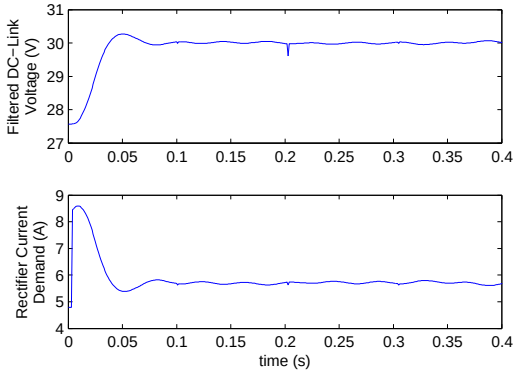
(c) DC-link voltage step, 6m/s condition



(d) Filtered DC-link voltage and current demand, 6m/s condition

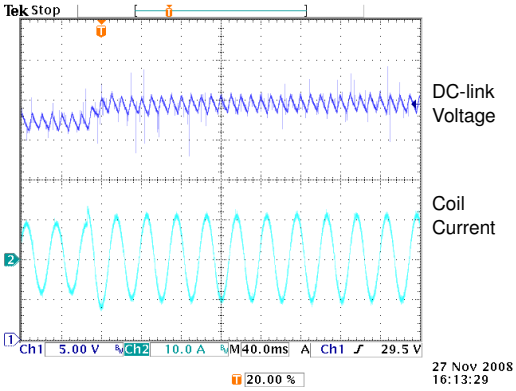


(e) DC-link voltage step, 9m/s condition

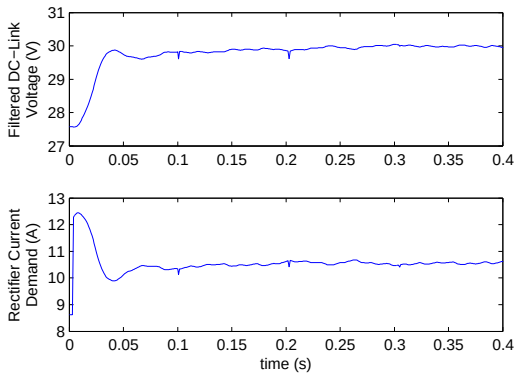


(f) Filtered DC-link voltage and current demand, 9m/s condition

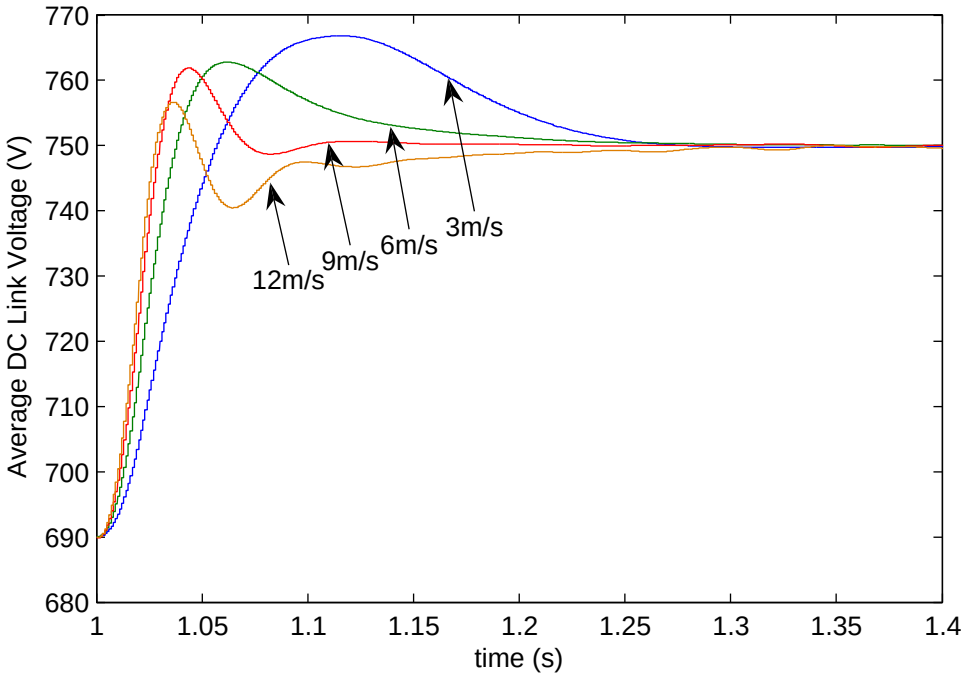
Figure 8.12: DC-link voltage controller step responses



(a) DC-link voltage step, 12m/s condition



(b) Filtered DC-link voltage and current demand, 12m/s condition



(c) Simulated DC-link voltage step response

Figure 8.13: DC-link voltage controller step responses, continued

8.5 Inverter Basic Operation

For testing the inverter, the operating conditions given in Table 8.1 were expanded to include the output power and output current (assuming 230V rms mains voltage). These conditions are given in Table 8.5. For testing the inverter the test system described in Section 7.8 was used, although the DSpace controller was only available when testing the harmonic compensation system and module power sharing. For the other tests, the de-centralised inverter control system described in the next chapter was used. For some tests a resistive loadbank was used as the inverter load in place of the variac and grid connection.

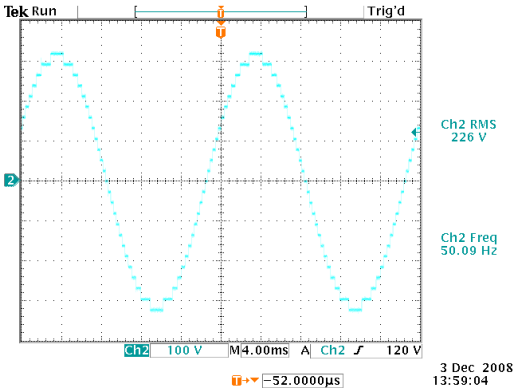
Wind Speed (m/s)	Generator Speed (rpm)	Output Current (A rms)	Output Power (W)
3 (cut in)	93	0.14	32
6	142	1.28	294
9	213	4.32	994
12 (rated)	290	10.9	2500

Table 8.5: Turbine operating conditions for inverter testing.

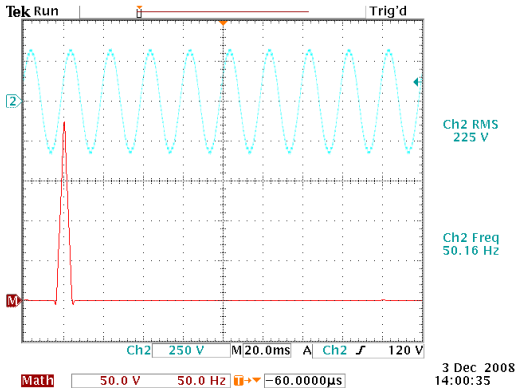
8.5.1 Testing with a Resistive Load

Initial testing of the inverter operation was carried out using a resistive load bank as the inverter load, in order to verify the inverter output waveform without any interactions with the mains voltage waveform. The inverter open circuit voltage, shown in Figure 8.14a shows an accurate sinusoidal waveform. The voltage spectrum, shown in Figure 8.14b, shows minimal harmonic distortion.

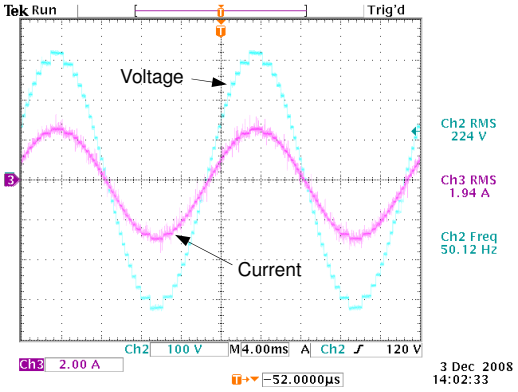
Current outputs were limited by the available resistances of the loadbank, which could step in multiples of around 220W. Because of this the 3m/s operating condition, corresponding to 32W, could not be tested. The voltage and current outputs for the 6m/s, 9m/s and 12m/s operating conditions are shown in Figures 8.14c, 8.14d and 8.14e. In the 12m/s operating condition distortion can be seen on the voltage waveform due to the DC-link voltage ripple of the modules. The voltage spectrum for the 12m/s condition is shown in Figure 8.14f, and around 5V of third harmonic distortion can be seen, representing 2.2% of the fundamental voltage.



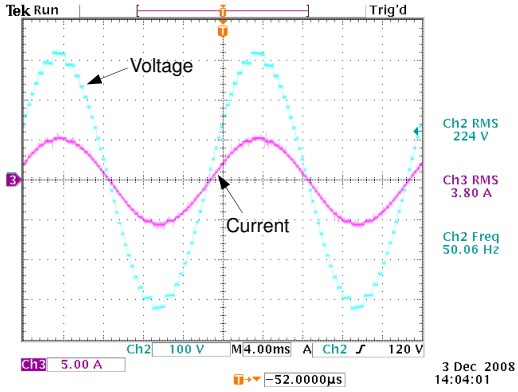
(a) Open circuit output voltage



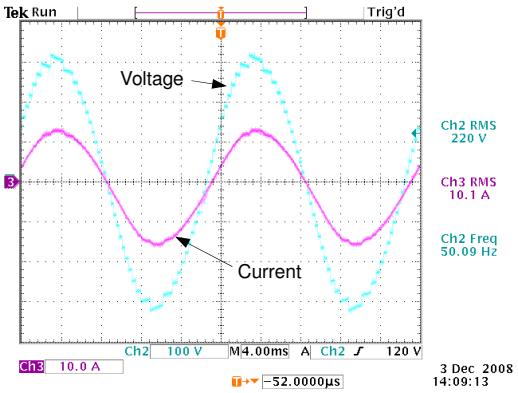
(b) Open circuit output voltage spectrum



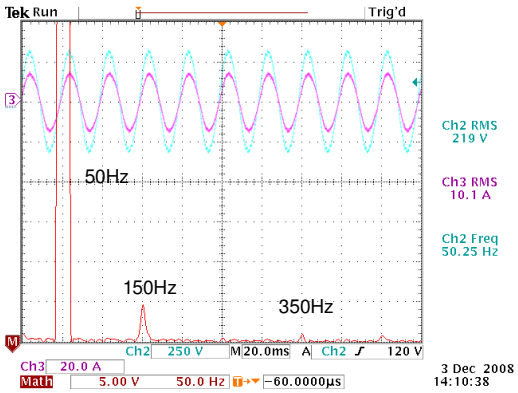
(c) Current and voltage at 6m/s operating condition



(d) Current and voltage at 9m/s operating condition



(e) Current and voltage at 12m/s operating condition



(f) Voltage spectrum at 12m/s operating condition

Figure 8.14: Inverter output current and voltage, resistive load

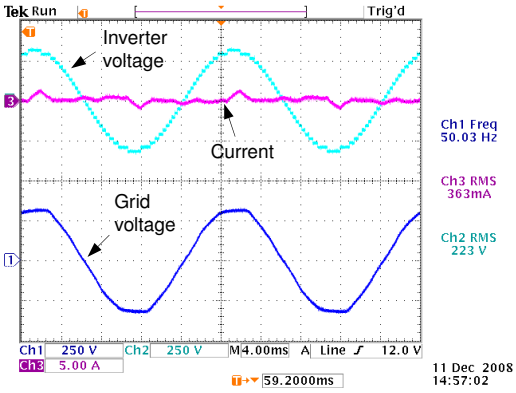
8.5.2 Testing with the Grid Connection

Testing the inverter using the load bank showed that a sinusoidal voltage waveform with low harmonic distortion was produced, meaning that if the grid voltage is also sinusoidal then a sinusoidal current should be produced. Unfortunately it was found that the grid voltage featured significant levels of distortion, leading to distortion in the output current. In an attempt to limit this distortion the inverter grid coupling inductance was increased from 3mH to 9mH, if the rated inverter current and voltage are used as base values this represents an increase from 0.045 PU to 0.137 PU. Unless otherwise stated, this increased inductance is used.

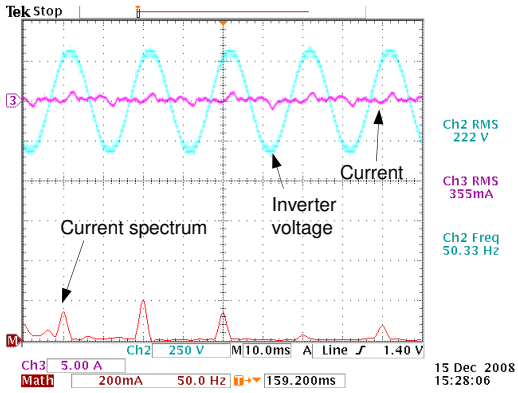
The inverter current and voltage, along with the grid voltage are shown in Figure 8.15a for the case where zero power output demand is set. Even with zero power output demand a small current is flowing, mostly in the form of higher harmonics. The current spectrum is shown for the zero power demand case in Figure 8.15b, and significant odd harmonic currents are present, which is typical for a power system where significant electronic loads are present. For comparison, the current waveform and spectrum are given for the original inductance in Figure 8.15c and show considerably higher distortion currents.

As even the zero current demand case produces a current in excess of that required by the 3m/s operating condition, this condition cannot be used. The inverter current and voltage for the 6m/s, 9m/s and 12m/s conditions with unity power factor output are shown in Figures 8.15d, 8.15e and 8.15f, and show decreasing relative current harmonic distortion with increasing output power.

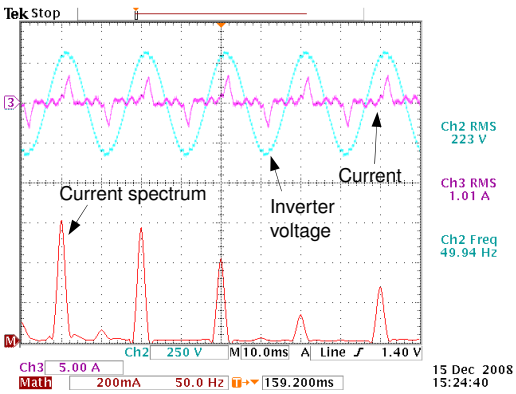
The 9m/s operating condition was also tested with different levels of reactive power flow. The Scottish Hydroelectric wind farm grid code requires a reactive power capability equivalent to 0.95 lagging or 0.85 leading at rated power [28], with the specified reactive power being available at all real power output conditions. Testing was carried out at the 9m/s wind condition, and due to the lower real power output, a lagging power factor of 0.77 and leading power factor of 0.54 were required. The results are shown in Figure 8.16.



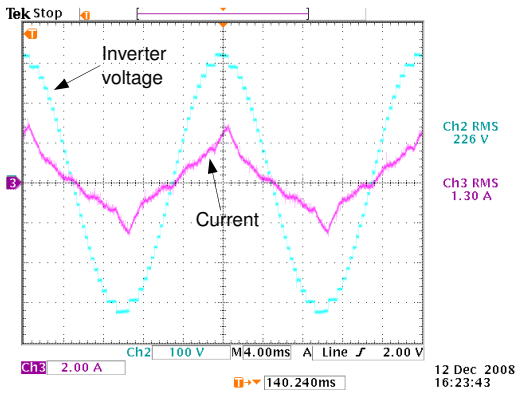
(a) Inverter current and voltage with zero output current demand, 0.134 PU inductance



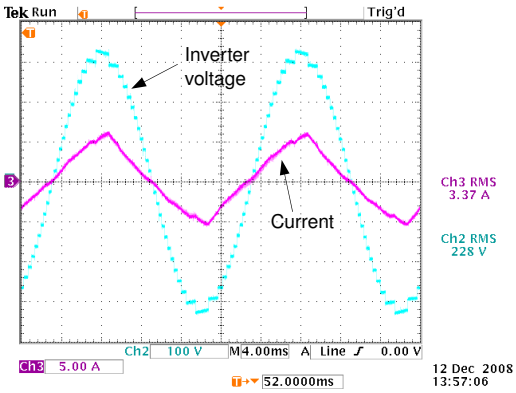
(b) Zero demand inverter current spectrum, 0.134 PU inductance



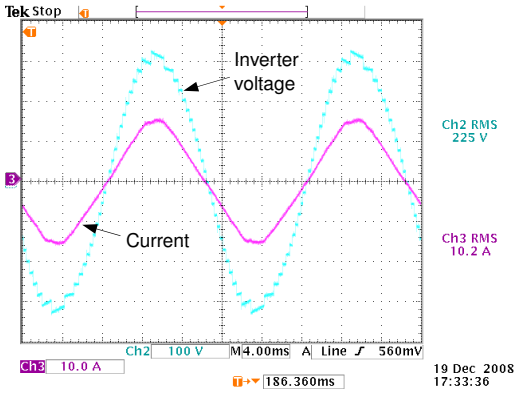
(c) Zero demand inverter current spectrum, 0.045 PU inductance



(d) Current and voltage at 6m/s operating condition, 0.134 PU inductance

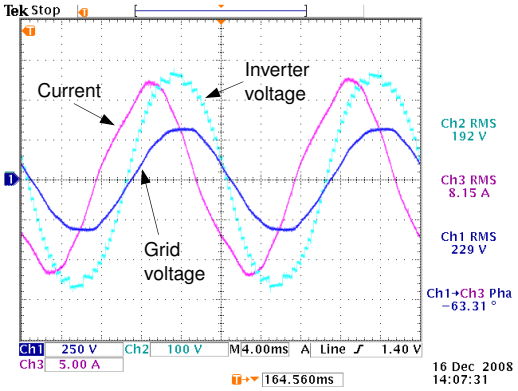


(e) Current and voltage at 9m/s operating condition, 0.134 PU inductance

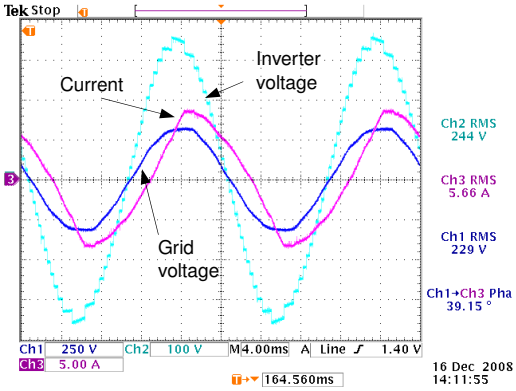


(f) Current and voltage at 12m/s operating condition, 0.134 PU inductance

Figure 8.15: Inverter output current and voltage, grid connection, unity power factor



(a) Current and voltage, leading power factor



(b) Current and voltage, lagging power factor

Figure 8.16: Inverter output current and voltage, 9m/s operating condition with grid connection and reactive power flow

8.6 Inverter Power Sharing

Power sharing between the inverter modules was tested in conjunction with other researchers on the project, and is described more fully in [47]. A resistive load bank was used as the inverter load, in order to obtain a sinusoidal output current, and a power of around 1300W was used. Module power was calculated by recording the input currents for all the modules, and multiplying by the estimated EMF magnitude. Power sharing was tested at several load power factors, by placing inductors in series with the loadbank.

The resulting module power values are shown in Figure 8.17 and show good agreement with the theoretical power sharing shown in Section 6.5.1, with the asymmetrical half-cycle switching resulting in significantly more equalised power sharing than the classic switching scheme. Varying the load power factor has little effect on the power sharing with asymmetrical half-cycle switching, as predicted.

8.7 Inverter Voltage Harmonic Distortion Correction

Design and testing of the inverter voltage harmonic distortion correction system were carried out by C.H.Ng, and are described more fully in [47], from which these results are taken. However the implementation of the distortion correction system

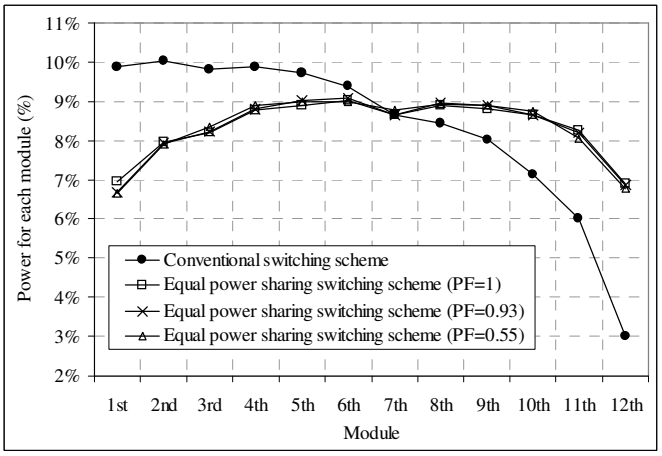


Figure 8.17: Inverter power sharing (image from [47])

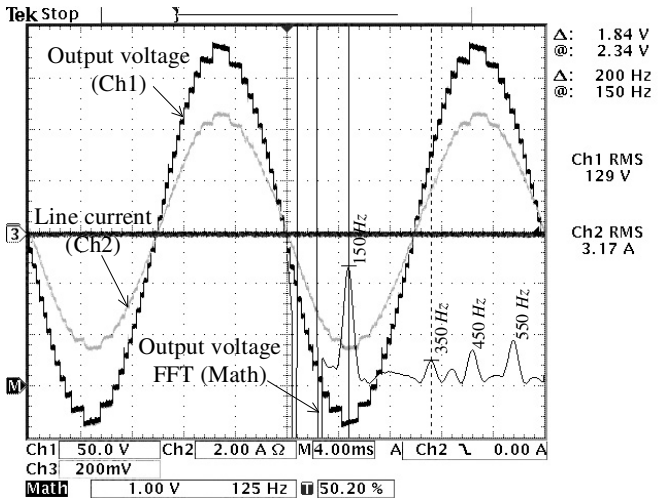
on the module side was carried out as part of this project, so the results will be given here.

The system was tested using a resistive loadbank, to avoid including current distortion due to the distorted grid voltage waveform. The voltage and current without the distortion correction is shown in Figure 8.18b, and significant harmonics can be seen in the inverter voltage spectrum, especially the third harmonic. The voltage and current with distortion correction are shown in Figure 8.18b, and the inverter voltage shows a significantly reduced third harmonic component.

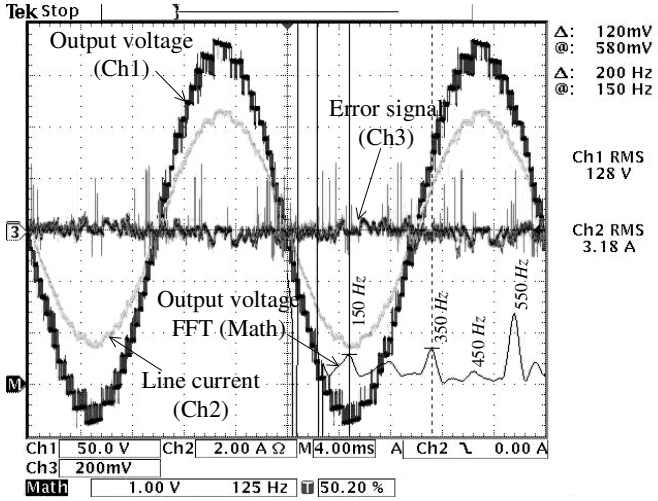
8.8 Inverter Fault Tolerance

Tolerance of single module faults relies on two elements: in the immediate aftermath of the fault, the faulted module will stop providing an output voltage, and the other modules must immediately increase their output voltage in order to compensate. The loss of a module will mean that the inverter output waveform will be distorted, producing a distorted current, so the module switching timings must be changed to compensate for the lost module.

Measurements of the effects of the fault on the inverter voltage and current are shown in Figure 8.19 for the 9m/s wind speed condition with grid connection. The normal operation of the inverter with 12 modules is shown in Figure 8.19a, and the operation with the sixth module in the sequence faulted is shown in Figure 8.19b. The inverter voltage waveform shows slight distortion, with a more pronounced dis-



(a) Uncorrected inverter output voltage



(b) Corrected inverter output voltage

Figure 8.18: Inverter voltage harmonic distortion correction (images from [47])

tortion in the current waveform (ignoring the distortion due to the mains voltage distortion). With the module switch timing changed the voltage and current waveforms are shown in Figure 8.19c, and the current waveform is back to how it was before the fault.

To test the ability of the system to dynamically adjust to a module fault, a fault was simulated on the sixth module, in which the module was set to produce a zero volt output. The inverter output voltage and current were recorded using the oscilloscope, and the DC-link voltage and voltage demand from the controller were recorded for the third module in the sequence using the recording capabilities of the module. The 9m/s operating condition was used and the inverter was grid connected. The results are shown in Figure 8.20, in which the module fault is initiated at a time of 0.04s, and the DC-link voltage is rapidly adjusted to compensate.

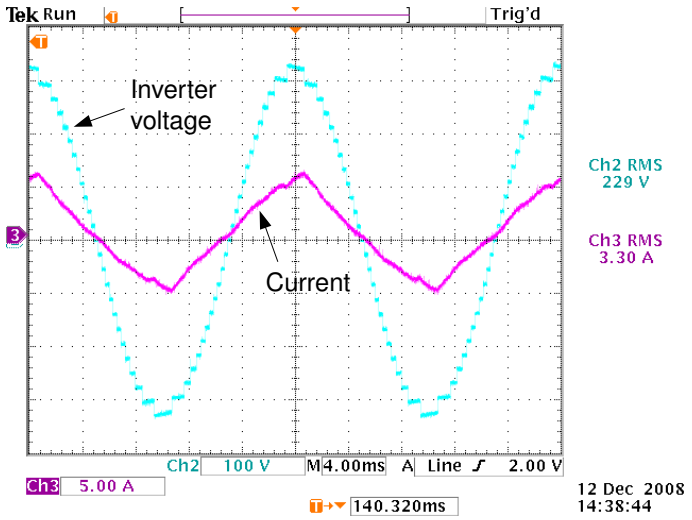
8.9 Conclusion

8.9.1 Rectifier Control

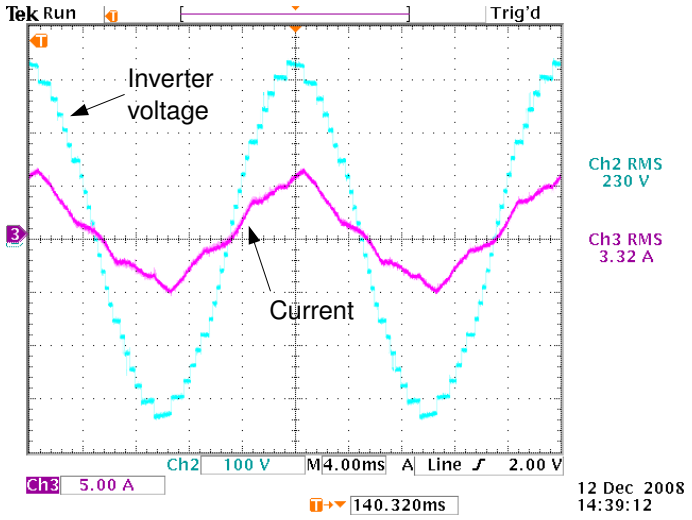
Testing of the rectifier current controller verifies the operation of the controller, and the ability to draw a sinusoidal current in phase with the coil EMF, as simulated in chapter 6. However the coil inductance at high frequencies was found to be lower than the value used in selecting the rectifier switching frequency, leading to a higher current ripple magnitude, and a higher minimum coil current to avoid discontinuous conduction.

This minimum coil current means that the turbine minimum power condition, for a wind speed of 3m/s, cannot be achieved, at least without the rectifier continually oscillating between the active and seeking modes. For continuous operation in the active mode, a wind speed condition of at least 4m/s is required. In any case, when testing the complete inverter with a load bank the minimum power condition could not be reached as the maximum resistance of the load bank was too high. When testing the complete inverter with a grid connection, even with zero output current demand the harmonic power drawn was greater than the desired output power, due to the grid voltage distortion.

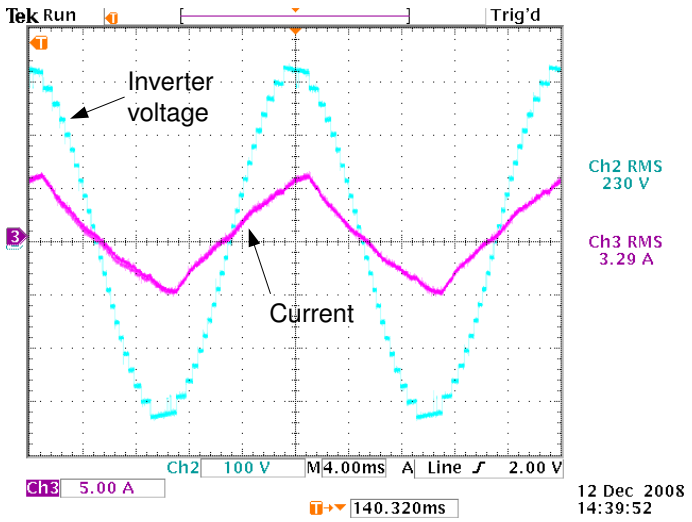
The coil inductance at high frequencies was also found to vary depending on the position of the rotor magnets relative to the coil, which can lead to third harmonic



(a) Inverter normal operation



(b) Single module fault, uncorrected



(c) Single module fault, corrected

Figure 8.19: Inverter V,I, waveforms with and without module faults

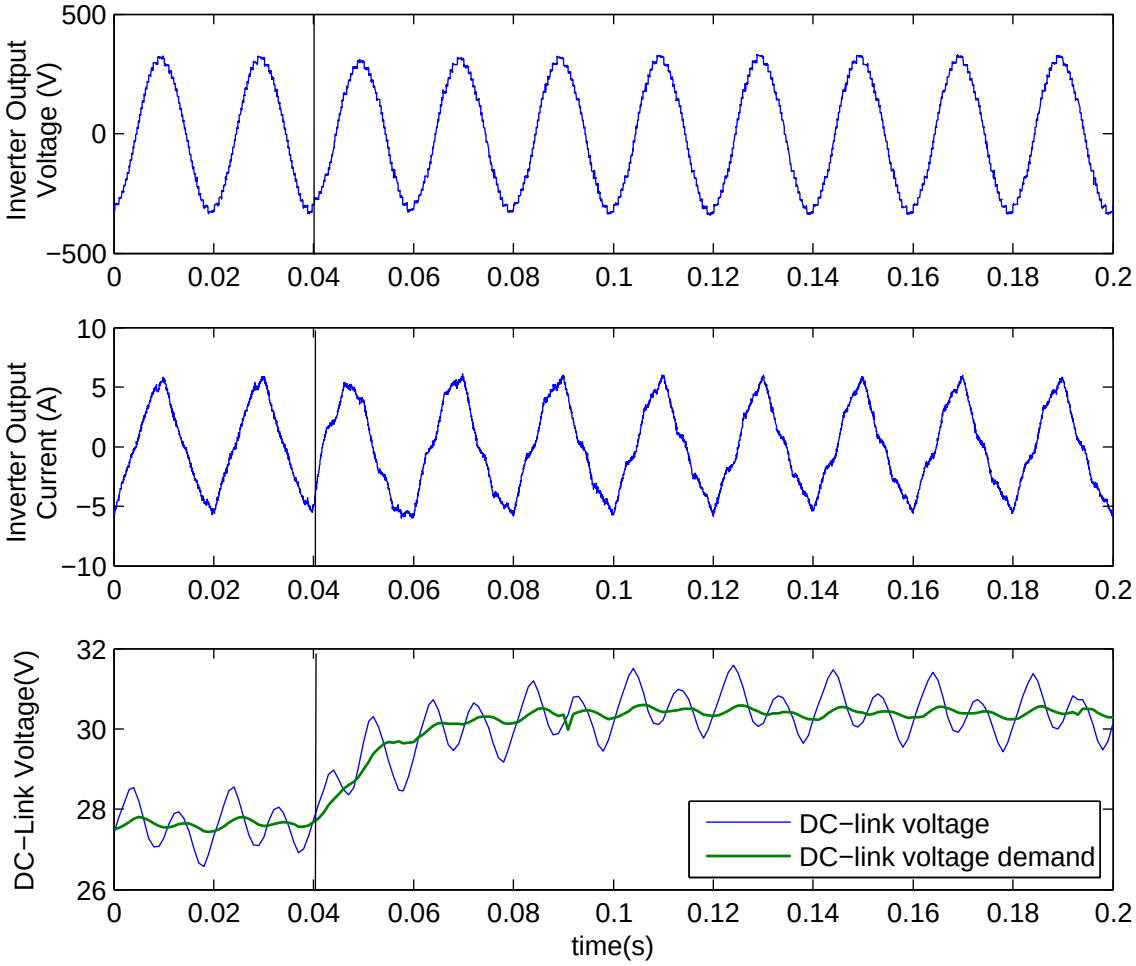


Figure 8.20: Inverter response to a sudden module fault

distortion in the coil current, particularly at low coil current demands.

Estimation and tracking of the coil EMF position was found to behave in a similar way to the simulation in chapter 6. One difference is that the estimated EMF in the rotating reference frame contains a sinusoidal ripple at four times the coil frequency, unlike the simulation which featured discrete spikes at that frequency.

The response of the EMF tracking loop was found to be faster than the dynamic capability of the motor-generator test rig, so it can be expected to be fast enough to track the speed of a wind turbine generator in all operating conditions.

Locking on to the coil EMF is achieved by providing short pulses to the rectifier transistors. This briefly shorts the coils, causing the current to begin to rise. The current at the end of the pulse is measured and will be proportional to the coil EMF if the pulse width is kept constant. This system was found to produce an extremely noisy estimate of the coil EMF, but the EMF tracking loop was able to lock onto the estimated EMF easily. The locking of the estimated speed to the actual speed was found to closely correspond to the theoretical step response of the EMF tracking loop calculated in chapter 6.

8.9.2 DC-Link Voltage Control

Steady state control of the DC-link voltage was carried out for modules with several different positions in the inverter switching order, leading to different DC-link voltage ripple profiles. In all cases the averaging filter was able to completely remove all of the voltage ripple, preventing it from causing a corresponding ripple in the coil current demand.

The response of the DC-link voltage to a step change in voltage demand, at different wind speed conditions, was found to strongly match the step response characteristics of the simulation in chapter 6. The step response rise time and peak overshoot were found to depend strongly on the wind speed operating condition.

8.9.3 Inverter Control

Testing of the complete inverter using a resistive loadbank showed that a good quality sinusoidal output with low harmonic distortion was produced. Some harmonic distortion to the inverter voltage waveform occurs at the rated power condition due to the ripple in the DC-link voltage.

When the inverter was connected to the grid, distortion in the grid voltage and the low inverter grid coupling inductance meant that the current waveform featured significant harmonic distortion. The grid voltage distortion meant that even with zero power demand a significant current is still drawn, mostly in the form of odd harmonics of the grid frequency. This means that the minimum power condition could not be tested.

In order to limit the harmonic currents, the grid coupling inductance was increased from 3mH to 9mH, or from 0.045PU to 0.13PU. The inverter was able to send real power onto the grid in all conditions up to the rated power condition, and also able to produce and absorb reactive power.

Power sharing between modules was tested using a resistive loadbank, at unity power factor and at two different lagging power factors. The asymmetrical half-cycle switching scheme was found to result in significantly better power sharing than the classic switching scheme, with the power sharing being unaffected by the load power factor.

The inverter voltage harmonic distortion correction scheme was tested using a resistive loadbank, and was found to reduce the magnitude of the third harmonic distortion, that being the most significant harmonic in the output AC voltage. However significant higher harmonics are still present in the inverter voltage waveform.

It has been suggested that in a three-phase inverter of this type the third harmonic currents can be eliminated by connecting the generator neutral point to ground through a large resistance, eliminating the conduction path for third harmonics. In this system, protection against a single-phase to ground fault can be proviced by detecting the change of the neutral to ground voltage.

Loss of a single module was found to lead to distortion in the inverter voltage waveform, leading to a distorted output current. This distortion is corrected by changing the switching patterns of the module output H-bridges, which was found to eliminate the voltage distortion, and hence the current distortion. The DC-link voltage of each module must also be increased to compensate for having fewer modules.

The overall controller was found to quickly react to the loss of a module by increasing the DC-link voltage demand, and the modules were able to quickly increase their DC-link voltage, so no current spikes due to the loss of a module were observed.

Chapter 9

Advanced Inverter Control Theory, Implementation, and Testing

A number of disadvantages have been found with the inverter control system described in chapter 6, and tested in chapter 8. Some of these are as follows:

1. There is no provision for ride-through of grid faults and voltage dips. In theory the system of overlaying PWM switching on the fundamental waveform could be used to reduce the inverter voltage during a grid fault, and so limit the current. Unfortunately the grid coupling inductance is very low, so the current is able to change rapidly, and the bandwidth of the PWM system, sending the error signal to the modules over the CAN bus, does not have sufficient bandwidth.

2. The system of overlaying PWM switching on the fundamental waveform, in order to compensate for harmonic distortion caused by the fluctuating DC-link voltage, does reduce distortion, but significant harmonics are still present. Performance is limited by the bandwidth and latency of the CAN bus, and most of the CAN bandwidth is used up in sending the error signals to the modules.

3. The control algorithm relies on measuring the inverter output voltage and the line voltage, requiring line voltage transducers capable of operating at the

11kV voltage output of the inverter, adding to complexity and introducing a source of unreliability. It has also been suggested that the inverter grid coupling inductance be distributed around the generator, as the modules are, and this would make the inverter output voltage impossible to measure.

4. The inverter central controller represents a single point of failure for the system. While it is significantly easier to repair the central controller as it is inside the turbine tower or nacelle, it's failure would still cause turbine downtime while repairs are carried out.

9.1 Proposed Solution

If PWM switching is used on the inverter output, with the PWM carrier signals interleaved as described in Section 6.5.2, then an accurate output waveform can be synthesized, while keeping the individual module inverter switching frequencies low. The PWM duty cycle of each module can then be adjusted to compensate for the fluctuations in the DC-link voltage. Each module will compensate for it's own DC-link voltage fluctuations, requiring no signals to be sent between moudules. This system will eliminate disadvantage 2.

As well as the ability to compensate for the fluctuations in the DC-link voltage, PWM switching should also improve power sharing between the modules and result in fewer low frequency harmonics in the DC-link voltage ripple, leading to longer DC-link capacitor lifetimes. One disadvantage of the PWM approach is the increase in switching losses from operating the switching devices at a higher frequency, so ideally fundamental switching will be used at low power for efficiency, and PWM switching at high power for distortion correction, better power sharing, and reduced DC-link voltage low frequency ripple.

All the power electronic modules in the test system described in chapter 7 feature inverter current transducers, so a proportional controller could be used to limit the current during a fault. This would work in the same way as the rectifier current controller and feature voltage feedforward as well. Theoretically if all the modules are sampling at a similar time then the individual module controllers will respond in the same way, as a single large inverter.

The current proportional controller will limit the inverter current at the moment

of a grid voltage collapse, allowing the grid voltage estimator time to adjust to the reduced voltage and change the inverter feedforward voltage levels, without excessive current flowing during the adjustment time. This will eliminate disadvantage 1. In order for the inverter to be able to supply whatever harmonic loads are present on the grid, a system without a current proportional controller is required, and in this case the output current will be controlled by varying the feedforward voltage signal.

Based on the idea that the modules are all sampling the inverter current simultaneously, and should behave in the same way, a grid position and voltage estimator, of the type described in [46] and used in the rectifier controller, could be incorporated into each module. The grid position and voltage estimate from each module could be synchronised over the CAN bus. This would eliminate disadvantage 4, and as the grid position and voltage estimator under consideration does not use a line voltage sensor, it will eliminate disadvantage 3, although the advantage of eliminating the line voltage sensor could be canceled by the need for each module to have a current transducer on the output.

9.1.1 Design Tasks

Design of the proposed system incorporates a number of design tasks, which are as follows:

- Synchronising the inverter current sampling of all the modules, and synchronising and interleaving the inverter PWM outputs, which will be done using the CAN bus.
- Implementing and testing the inverter current limiting scheme. As well as current limiting, a system using only voltage feedforward should be implemented, as well as a system with fundamental frequency switching.
- Synchronising the grid reference angle and voltage between modules such that a sinusoidal voltage waveform is produced.
- Implementing a system to estimate and track the grid voltage position and magnitude.
- Implementing a method of locking on to the grid voltage.

9.2 Module PWM Interleaving and Sampling Synchronisation

The synthesis of the inverter output waveform using interleaved PWM is shown in Figure 9.1 for 5 modules. The inverter PWM carrier is synchronised to the rectifier carrier, although at 1/48th the frequency, and the inverter current is sampled by the ADC along with the rectifier currents. The inverter PWM duty cycle is updated and current limiting performed in the rectifier interrupt service routine (ISR), at 16kHz. This means that if the module PWM carriers are interleaved properly then all modules will be sampling the current and running the current limiting routine simultaneously.

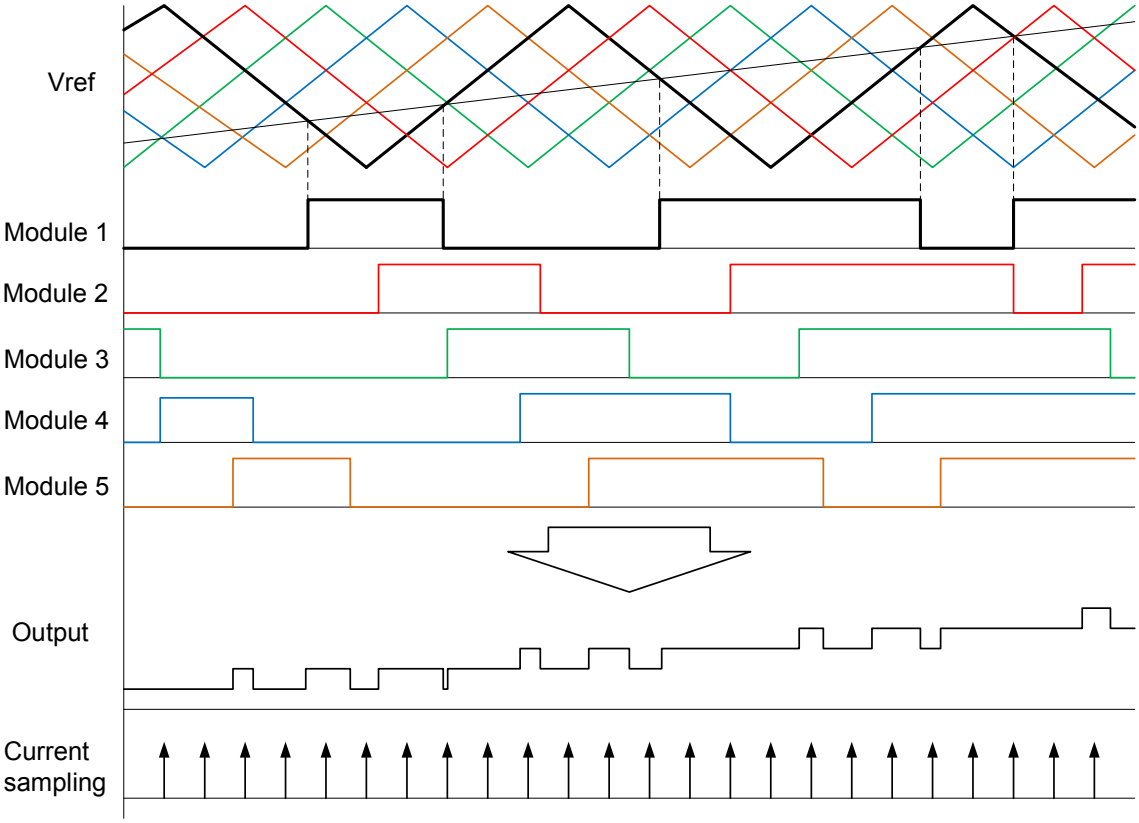


Figure 9.1: Interleaved inverter PWM carrier waveforms

Each module will send a message frame on the CAN bus whenever it's inverter PWM carrier reaches a peak, while also listening out for the synchronisation messages from other modules. Using CAN message timestamps recorded by the CAN controller, each module can calculate the time difference between it's PWM carrier and those of the previous and next modules in the sequence. These time differences is

used to either lengthen or shorten the time period of the inverter and rectifier PWM carriers in order to equalise the time differences, as shown in Figure 9.2 for three adjacent modules. This is similar to a digital implementation of the system used in [52], which uses an analogue synchronisation bus, and a much higher switching frequency.

The modules do not switch in any particular sequence, instead the interleaving system ensures that when the modules are powered up they will automatically interleave their PWM carriers evenly. If a module fault occurs and that module stops transmitting it's synchronisation message, the remaining modules will re-distribute their PWM carriers to compensate.

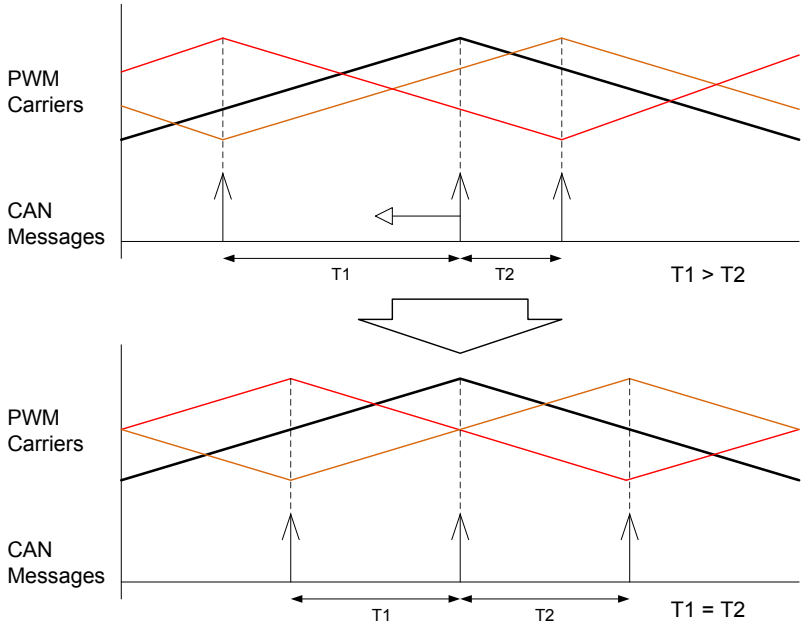


Figure 9.2: Synchronisation and interleaving of PWM carrier waveforms

The system is slightly more complicated than described above. Unipolar voltage switching is used on the inverter output, which means that the output PWM frequency of each module H-bridge is double the switching frequency of the individual inverter legs [58]. This means that the synchronisation message frame must be sent when the inverter PWM carrier reaches a maximum or minimum.

With the rectifier PWM carrier operating at 16kHz and the PWM carrier at 1/48th of this value, each leg of the module H-bridge will switch at 333Hz, giving a frequency of 667Hz for both legs, and 8kHz apparent frequency for the entire inverter. This means that message frames will be sent on the CAN bus at a rate

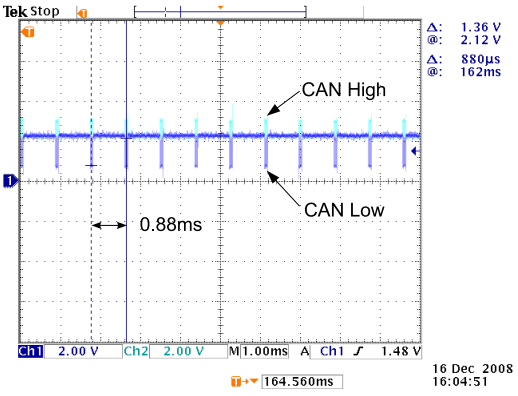
of 8000 per second, and with a message frame length of 44bits (with no data) this will require a bandwidth of 352kbps, over a third of the maximum CAN data rate of 1Mbps. To reduce the bandwidth requirement the synchronisation messages are only sent every seventh carrier maximum or minimum. Seven was chosen as it is not a factor of 12, 11 or 10, which are the potential number of modules in the system, so no modules will end up switching at the same time.

Listings of the microcontroller C code for the most important functions are provided in appendix C, and may aid in explaining the operation of the PWM interleaving system.

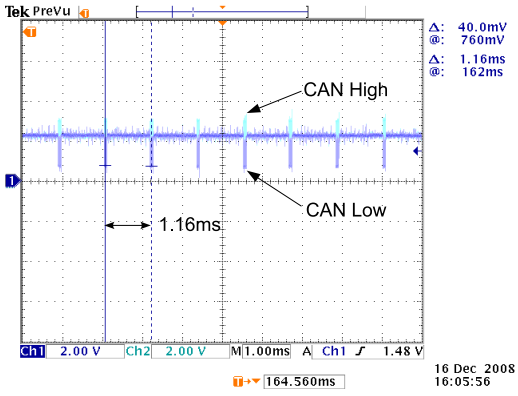
This PWM interleaving system relies heavily on the interaction of the PWM and CAN hardware of the modules, as well as the hardware interrupt timing, making simulation difficult, and as such was tested directly on the laboratory system without simulation.

9.2.1 Verification of Interleaving System Operation

The interleaving system was implemented in the 16kHz hardware ISR of each module. The CAN bus was monitored to verify the operation of the interleaving system, and the results are shown in Figure 9.3a with all 12 modules and in Figure 9.3b with only 9 modules. In both cases the message frames on the CAN bus are spaced evenly, indicating correct interleaving.



(a) CAN activity with 12 modules



(b) CAN activity with 9 modules

Figure 9.3: CAN activity due to PWM interleaving process

The synchronisation error signals of four modules are shown in Figure 9.4, and show a jitter of around $20\mu s$ for all modules. As the synchronisation pulses are only

sent out at 1/7th of the PWM frequency, this results in a jitter in the PWM signal of 2.86μs, which should not cause any significant issues. The jitter appears to be oscillatory in nature, rather than random, and further modeling of the interleaving process could result in a system with much lower jitter.

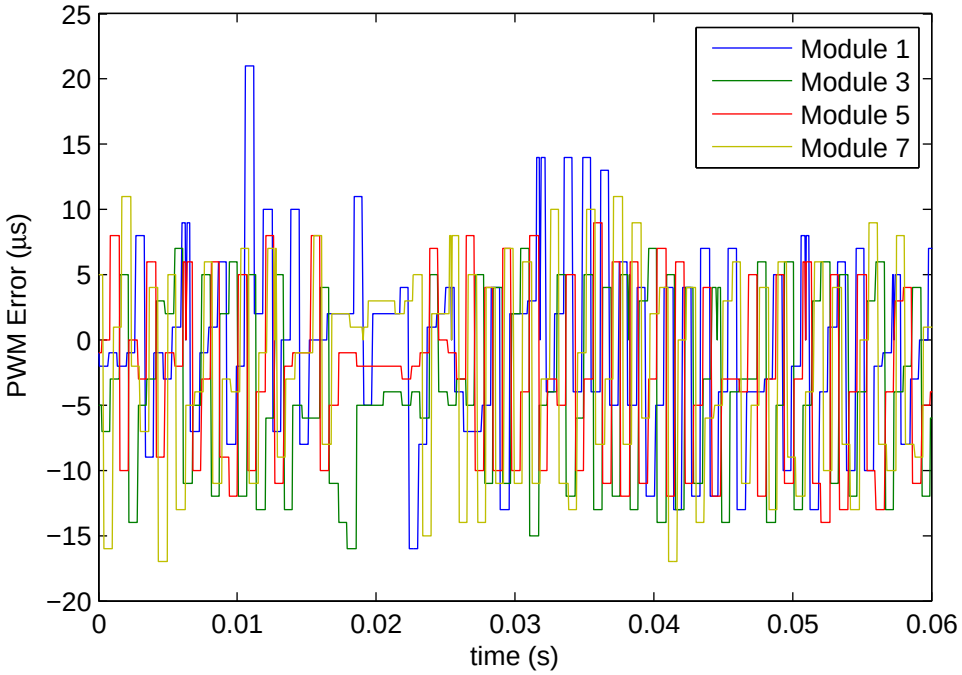


Figure 9.4: PWM synchronisation errors of 4 modules

9.3 Inverter Waveform Synchronisation and Grid Reference Angle PLL

A system based on a grid reference phaselock loop (PLL) and a grid voltage reference, as used in [46] and the rectifier controller, can be used to obtain reference values for the grid voltage angle and magnitude, $\hat{\theta}_g$ and $\hat{V}_g$. These values are required in order to set the output voltage of the inverter to the correct magnitude and phase, to achieve the desired output current.

The angle and magnitude of the grid voltage can be estimated in the controller of one module, and the results used to synchronise the grid references of all the other modules. Alternatively the reference PLL and grid voltage reference can be implemented in every module, which will provide greater redundancy, and resistance to glitches in the grid voltage tracking of one module.

This system requires the grid reference angles to be synchronised between modules, which is similar to the problem of synchronising clocks between multiple nodes in a distributed system [59], especially a system where a relative time is synchronised between nodes rather than an absolute time obtained externally. Both centralised and decentralised algorithms of varying complexity exist.

A simple decentralised method of synchronising the reference angle between modules, described in [59], is for each module to periodically broadcast what reference angle it has, onto the network, with the modules collecting the values from each other and updating their own reference angle with the average. A better algorithm, especially designed for use with the CAN system used on the modules, is described in [60], but for simplicity the simple averaging system will be used.

Each module will send a message frame on the CAN bus for PWM synchronisation and interleaving, as described in Section 9.2, and instead of being empty message frames they can include that module's current grid voltage reference angle and grid voltage magnitude. Each module sends a synchronisation message at a frequency of around 95Hz, so for a system of 12 modules synchronisation messages will be received by each module at a rate of around 1140Hz, and will be evenly spaced in time.

When the CAN controller on a module receives a synchronisation message from another module, the message contents are stored in a mailbox, and the message timestamp is recorded, based on an internal 32-bit counter. Rather than having the message reception trigger a hardware interrupt, the message is ignored until the 16kHz rectifier ISR runs.

In the ISR, the received grid voltage reference angle and magnitude are recorded. The message timestamp is compared with the current value of the timestamp counter, and used to compensate the received reference angle for the delay between the message reception and the occurance of the ISR. The error between the received reference angle and the module's own grid reference angle is calculated and stored.

This error is used in the grid reference angle PLL, which is implemented in the 1kHz ISR. Instead of taking an average of the errors from all the other modules, the most recent error received is simply fed straight into the PLL loop filter, with the syncronisation messages being received slightly faster than 1kHz there is always a new error value. As the time constant of the loop filter is considerably longer than

the rate at which the modules send their synchronisation messages, an averaging function is performed.

The structure of the grid angle reference PLL is shown in Figure 9.5. The error between the module's grid reference angle and those of the other modules is labelled e_1. The error between the grid reference angle and the actual grid angle, estimated from the voltage and current, is labelled e_2. The loop filter takes the form of a PI-controller, as in the machine angle reference PLL, with the difference being that separate proportional and integral gains are used the two errors e_1 and e_2. This allows the controller to be set to prioritise tracking the estimated grid angle or the reference angle of other modules.

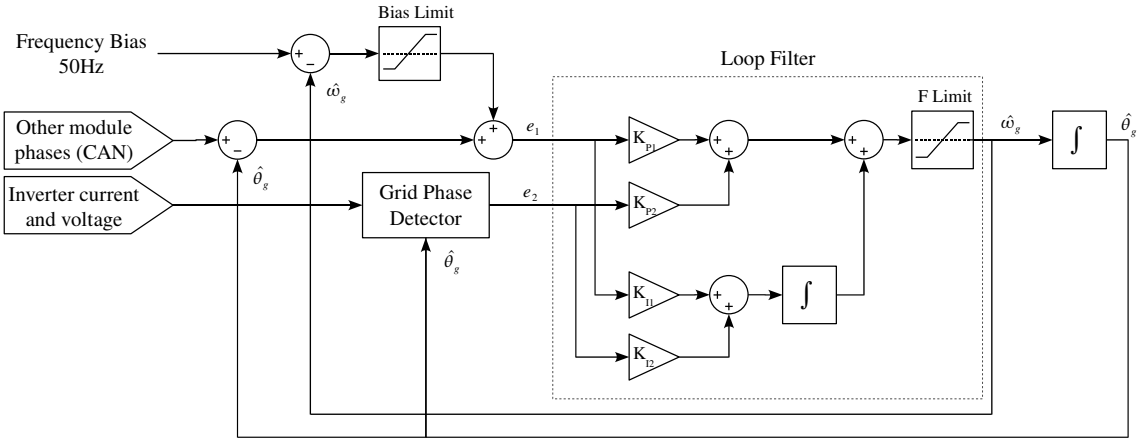


Figure 9.5: Grid angle reference PLL structure

The grid angle reference PLL also includes a control loop which will bias the loop frequency toward a preset value, which is included to keep the estimated frequency at around 50Hz when the inverter is not connected, preventing the frequency from wandering around randomly. The choice of loop filter characteristics will be analysed in Section 9.5 as these depend heavily on the characteristics of the grid voltage estimation method.

In the rectifier machine EMF reference system, the EMF magnitude was assumed to be proportional to the frequency, due to the permanent magnet generator, but this is not the case in the grid voltage reference system, and a grid voltage magnitude reference is required. The grid voltage can be estimated, as described in [46], and this can then be filtered and used as a grid voltage reference for calculating voltage feedforward values for the inverter. In this system, the voltage reference must also be synchronised between modules.

The grid voltage reference takes the form of an integral controller, shown in Figure 9.6. The use of an integrator allows the voltage to be biased toward a specific value when there is no input to the grid voltage detector, and separate integral gains are used for the synchronisation to the estimated voltage vs. voltage of other modules. The integral gains will be analysed in Section 9.5.

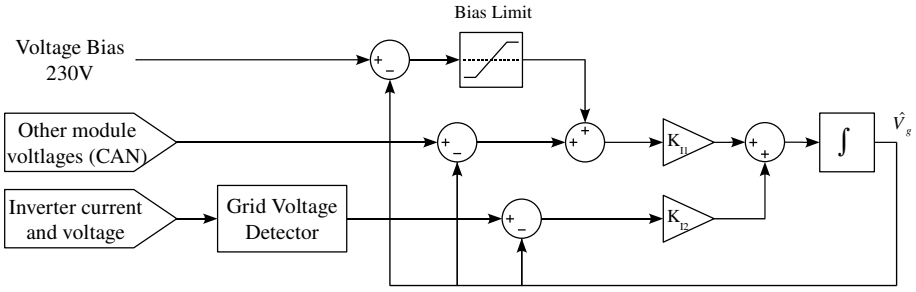


Figure 9.6: Grid voltage reference filter structure

9.3.1 Verification of Module Grid Reference Synchronisation

Synchronisation of the inverter grid reference between modules is shown in Figure 9.7 for four modules, in a steady state situation. In this test the grid angle and voltage estimator was disabled, leaving only the synchronisation between modules and the 50Hz and 230V default values of frequency and voltage.

The grid frequency reference shows mostly white noise when zoomed in, while the voltage reference shows a distinct ripple at 50Hz, which could be caused by some sort of interaction with the grid voltage estimation system, although the ripple is small enough not to be a problem.

9.3.2 Verification of Inverter Output Waveform

The inverter voltage waveform, with an open circuit output and PWM switching, is shown in Figure 9.8a, and shows a good sinusoidal waveform. The spectrum of the voltage waveform is shown in Figure 9.8b, and shows no low frequency harmonics. Switching ripple is spread between 6kHz and 10kHz, without any frequencies having an excessive ripple, which should lead to low acoustic noise.

Testing with a load bank, at the 12m/s wind condition described in the previous chapter, is shown in Figure 9.8c, and shows no low frequency inverter voltage har-

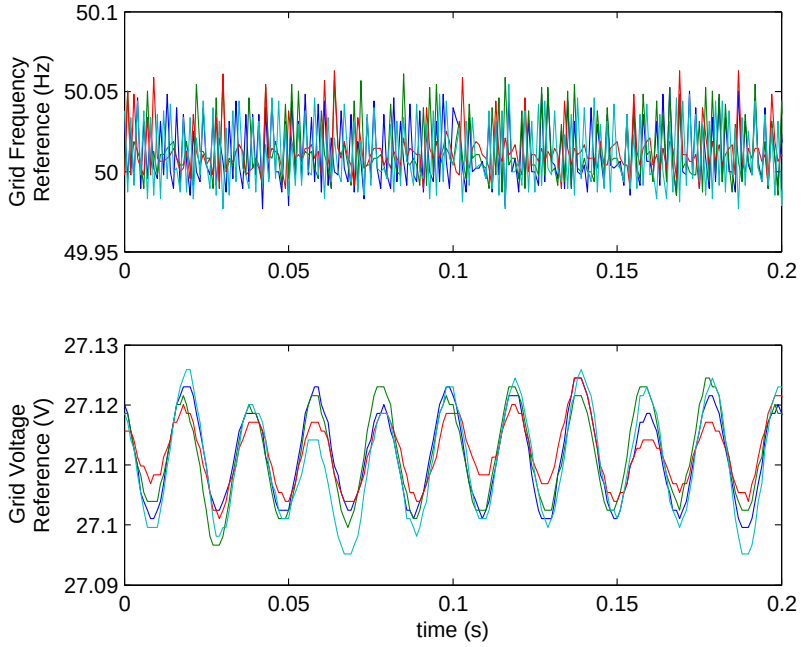


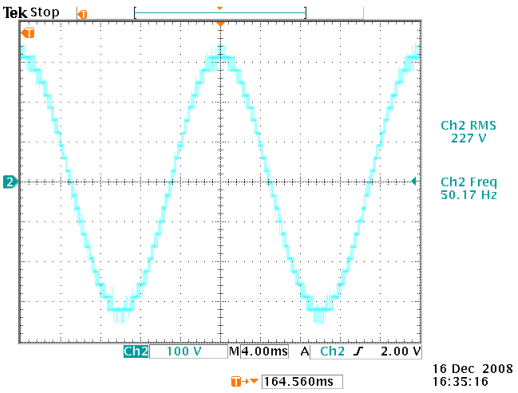
Figure 9.7: Synchronisation of Inverter Grid Reference

monics. This shows that the PWM switching is able to compensate for the ripple in the module DC-link voltages, and can be compared favorably to the same conditions with fundamental switching, shown in Figure 9.8d, where third harmonic distortion is apparent.

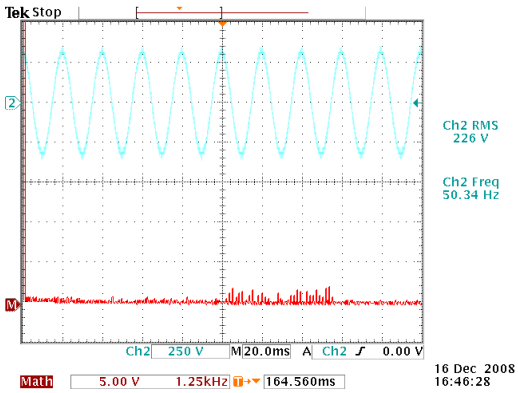
9.4 Inverter Current Controller and Current Limiting

During normal operation of the inverter, the inverter output voltage position and magnitude are set based on the reference grid voltage magnitude and position $\hat{V}_g$ and $\hat{\theta}_g$, and the d- and q-axis current demands I_d^* and I_q^*, which are used to set the feedforward voltage applied to the inverter. The control structure is shown in Figure 9.10a, and the feedforward voltages V_d and V_q are calculated in a similar way to the rectifier feedforward voltage calculation described in Section 6.3, and shown in Figure 9.9 and Equation 9.1.

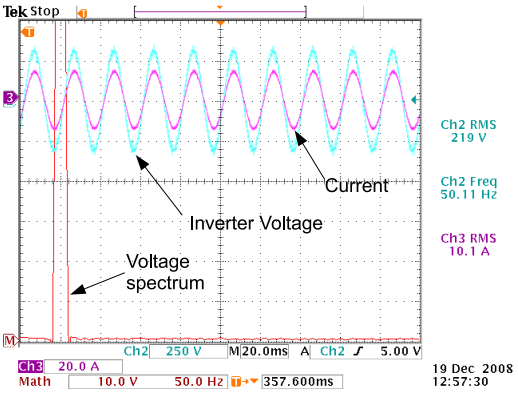
$$\begin{bmatrix} V_d \\ V_q \end{bmatrix} = \begin{bmatrix} 0 \\ \hat{V}_g \end{bmatrix} + \begin{bmatrix} R & 0 \\ 0 & R \end{bmatrix} \begin{bmatrix} I_d^* \\ I_q^* \end{bmatrix} + \begin{bmatrix} 0 & -\omega L \\ \omega L & 0 \end{bmatrix} \begin{bmatrix} I_d^* \\ I_q^* \end{bmatrix} \tag{9.1}$$



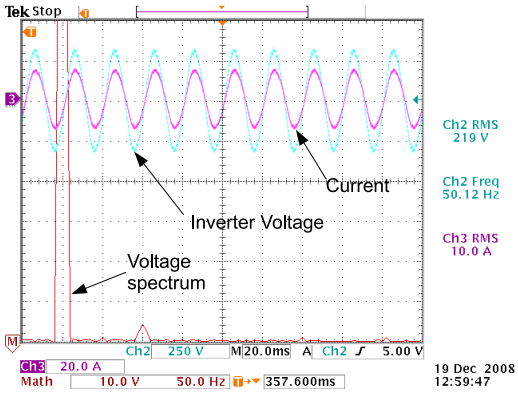
(a) Open circuit output waveform



(b) Open circuit output waveform voltage spectrum



(c) Current and voltage, PWM switching, 12m/s condition



(d) Current and voltage, fundamental switching, 12m/s condition

Figure 9.8: Inverter voltage waveform

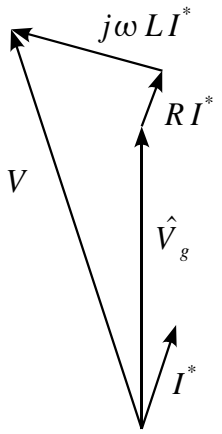
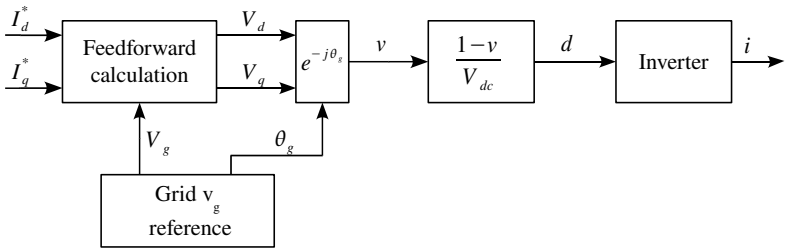


Figure 9.9: Inverter voltage feedforward phasor diagram

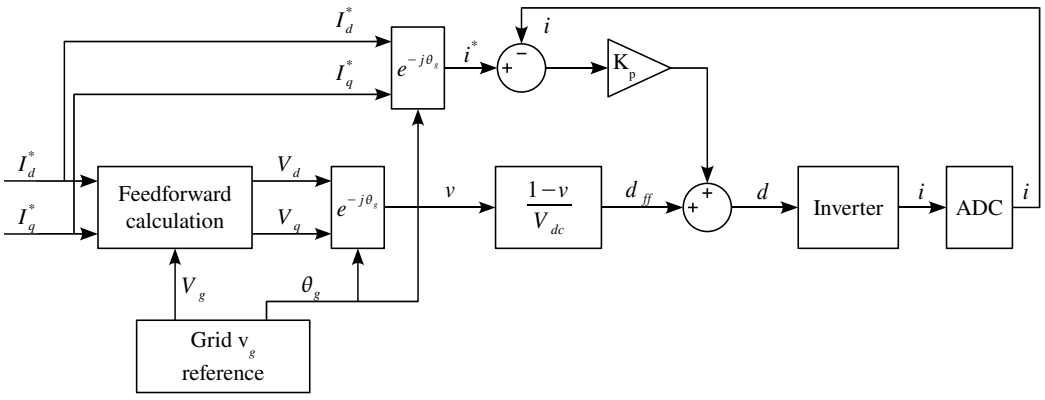
This control structure is implemented on each module, and if the grid angle and magnitude estimates are synchronised between modules the system should behave as an inverter with a single controller. The feedforward system assumes that the inverter grid coupling impedance is large with respect to the grid impedance, which is usually valid.

The inverter current limiter exists to limit the inverter current immediately after a sudden drop in grid voltage, caused by a grid fault. This is required as the grid voltage estimator will take several grid cycles to adjust to the new grid voltage, during which the current would rise to a value which would destroy the inverter.

Current limiting of the inverter output is similar to the proportional controller for the rectifier current, although control is simplified as the inverter is a full four-quadrant inverter, so the current and voltage can take positive and negative values independently, and there is no discontinuous conduction region. The system relies on all the modules in the inverter sampling the grid current at the same time. The inverter current controller is shown in Figure 9.10b with current limiting enabled. The proportional gain K_P is set through experimentation, and is described in more detail in Section 9.4.3 and 9.6.1.



(a) Without current limiting



(b) With current limiting

Figure 9.10: Inverter current controller structure.

In normal operation the inverter will operate without current limiting, in order to provide the current harmonics drawn by the grid. In the event of a grid fault or voltage dip, a sudden increase in current will occur, and the module controller will detect this and switch to the current limiting mode. A message will also be sent on the CAN bus telling the other modules to switch to the current limiting mode if they have not done so already.

Current limiting will be activated when the inverter current exceeds a preset limit value. In theory a system which detects a high rate of change of current, occuring in a grid fault, could be faster at detecting the fault. In practice it was found that the low grid coupling inductance meant that the current rose to a level high enough to trigger the current limiter in only a few cycles of the 16kHz ISR.

The current limiting mode is also required in order to lock the inverter grid angle estimate onto the actual grid angle. The inverter has only current sensors in each module, so cannot directly measure the voltage. The system used in the rectifier for locking on, and described in [46], of applying short pulses to the inverter switches and observing the rate of change of current, would require the module controllers to switch from a mode where all the modules switched at once for locking on, to the interleaved mode for normal operation, and there was insufficent time to develop such a system.

Because the grid voltage cannot be estimated without connecting the inverter, the inverter must be connected without first being synchronised to the grid voltage. When this is done, the current limiting system will limit the current while the grid angle reference PLL locks on to the estimated grid angle.

9.4.1 Simulation of Inverter Current Limiting

The inverter current control and current limiting system was simulated using Simulink, as opposed to the other aspects of the control system which were implemented directly in hardware, as it is the most critical aspect of the new control system. The model of the inverter consists of 12 identical modules.

The simulation model for a single module is shown in Figure 9.11. The Timebase block produces the PWM timebase, which is offset by a phase value given as an input to the block, in order that the PWM outputs of all the modules are interleaved as described in Section 9.2. The exact mechanism of interleaving is not simulated, and

the phase value only sets the initial value of the PWM timebase counter at the start of the simulation. The timebase block also provides a trigger for the PWM interrupt block, which operates at 48 times the module PWM frequency, and corresponding to the 16kHz rectifier hardware interrupt.

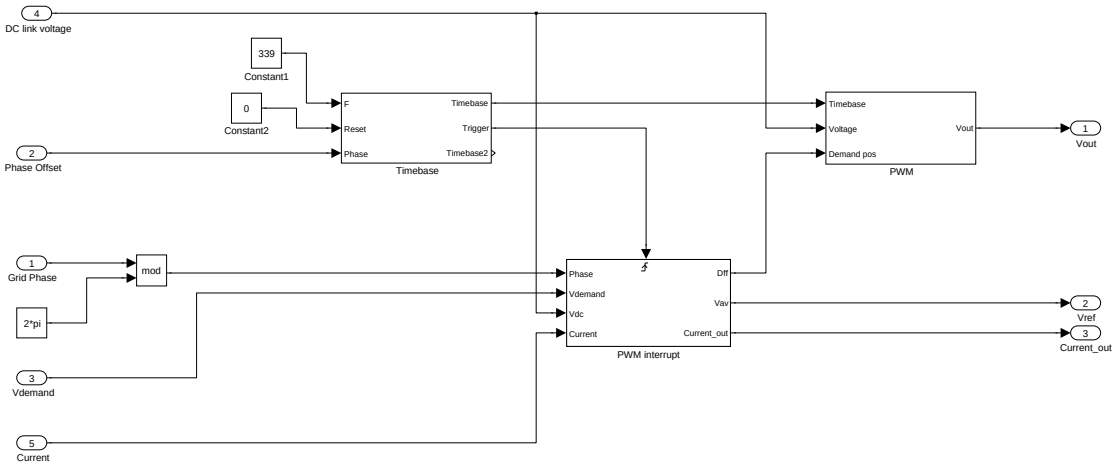


Figure 9.11: Simulation structure of single module

The PWM Interrupt block calculates the PWM duty cycle based on the structures shown in Figure 9.10, and also includes a mechanism to switch from the feed-forward system, in normal operation, to the current limiting system, in fault conditions. The changeover occurs when the measured grid current exceeds a trigger value. The PWM Interrupt block uses as an input the desired output voltage angle and magnitude, from a central controller, and does not model any synchronisation process between modules.

The PWM block takes the PWM duty cycle, DC-link voltage and timebase, and calculates the output voltage of the module H-bridge. The module model assumes that the DC-link voltage is constant, and the DC-link voltage controller was not simulated.

The simulation structure of the complete inverter and grid connection is shown in Figure 9.12, in which a single phase inverter, based on the prototype system described in chapter 7, is simulated. The grid electrical angle is calculated using a self-resetting integrator, based on a constant frequency, and the grid voltage waveform found by taking the sine of this angle and multiplying by the desired grid voltage amplitude. A step function is used for the output voltage, allowing the voltage to be stepped to a lower value to simulate a grid fault or voltage dip.

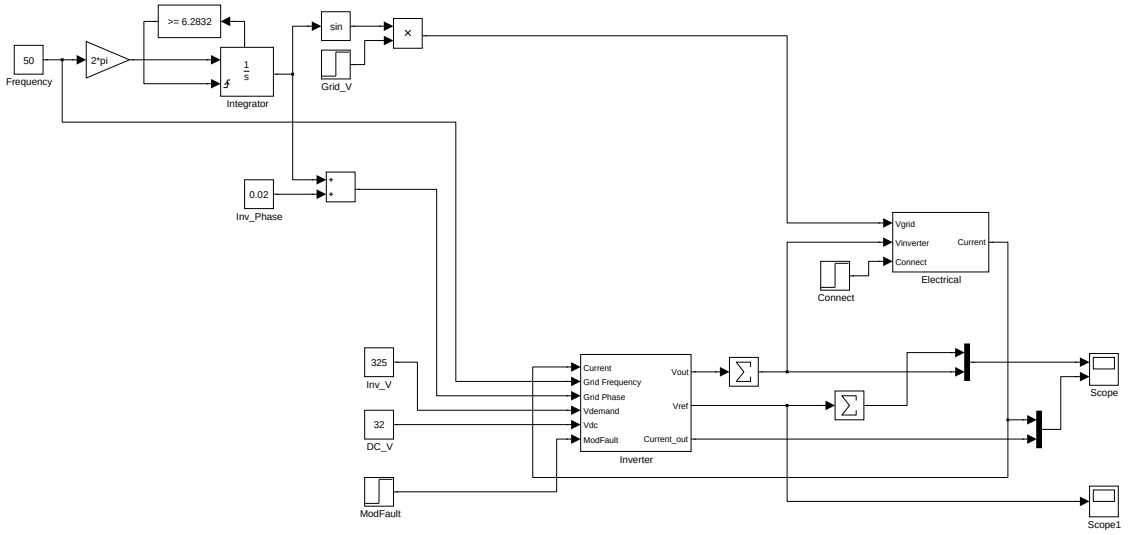


Figure 9.12: Inverter simulation structure

The Inverter block contains 12 of the module blocks, set with the appropriate PWM phase relationships. The desired output voltage reference angle is calculated by adding a constant phase difference to the calculated grid angle, with the phase difference determining the real power output. The desired voltage output magnitude is a constant, as is the DC-link voltage. A module fault input is provided, which will cause the DC-link voltage of one module to drop to zero, simulating a module fault.

The outputs of each module are summed to obtain the total output voltage, and this is fed into the Electrical block, which determines the inverter current based on the inverter and grid voltages. The inverter current calculation is implemented in Simulink according to Equation 9.2, where I_g is the grid current, V_{inv} and V_g the inverter and grid voltages, and L_g and R_g the inductance and resistance of the coupling inductor. A grid coupling inductance value of 3mH was used.

$$I_g = \frac{1}{L_g} \int (V_{inv} - V_g - I_g R_g) dt \tag{9.2}$$

9.4.2 Current Control Simulation Results

Simulated inverter current and voltage waveforms are shown in Figure 9.13. The inverter output voltage phase and magnitude, relative to the grid voltage, were set manually to achieve a current of around 2.8A rms, with unity power factor on the grid side.

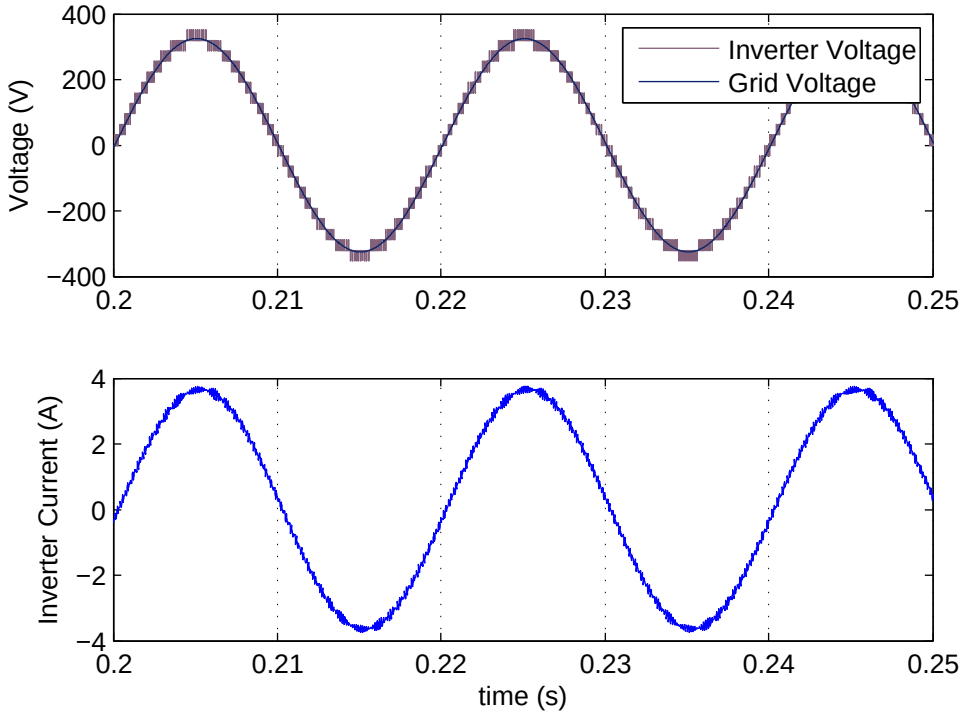


Figure 9.13: Simulated inverter voltage and current, normal operation

The current and voltage waveforms during a grid fault are shown in Figure 9.14. The same initial conditions as the normal operation case were used, with the grid voltage being dropped from 230V to 14V rms 0.205s after the start. The inverter current rises rapidly with the fault, and at a current of 20A the current limiting system is activated. The current limiter tries to force the current to a magnitude of 2.8A rms, but the steady state error of the proportional controller means that a higher current flows.

The steady state error of the proportional controller means that the inverter current during a fault will always be higher than the desired current, but this will only last until the grid voltage estimator is able to register the decrease in voltage, and the feedforward voltage is reduced. The steady state error depends on the value of proportional gain used, and the stable gains depend significantly on the hardware implementation of the inverter.

9.4.3 Testing of Inverter Current Limiting

Current control using only the voltage feedforward method cannot be tested without the grid reference PLL, described in the next section, but the current limiting system

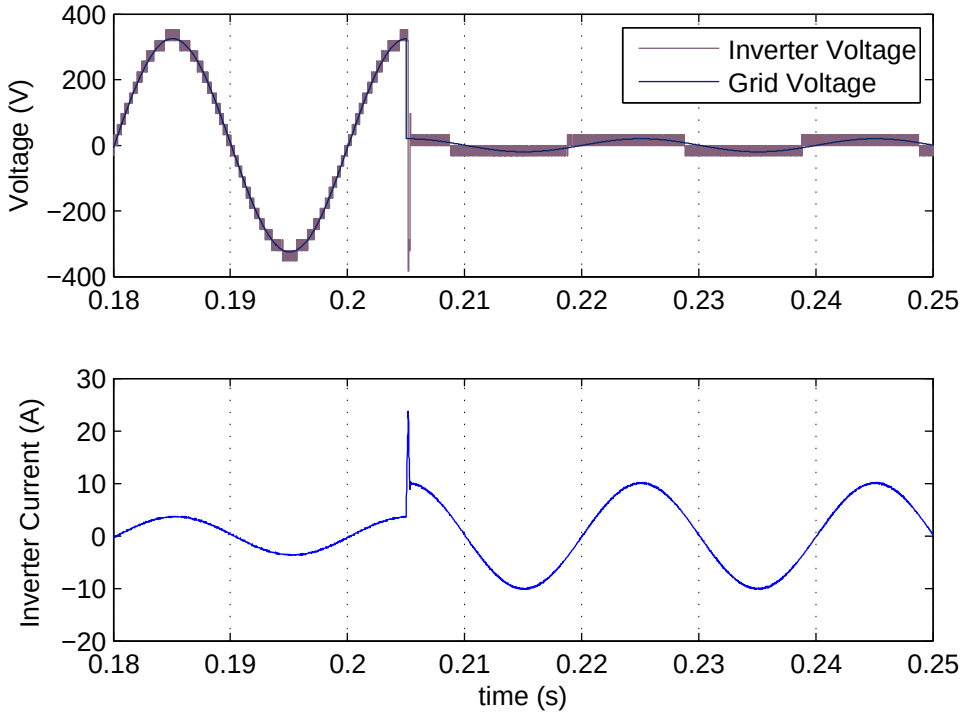


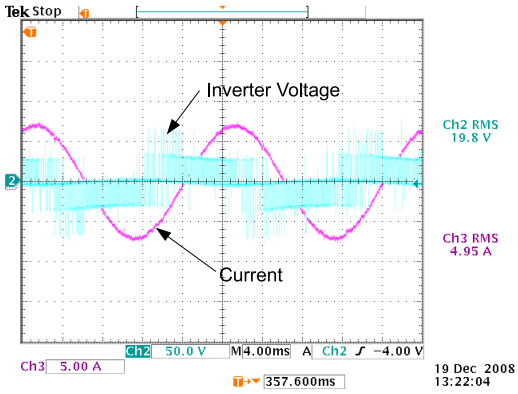
Figure 9.14: Simulated inverter voltage and current, grid fault conditions

can be tested using a loadbank, through a 3mH coupling inductance.

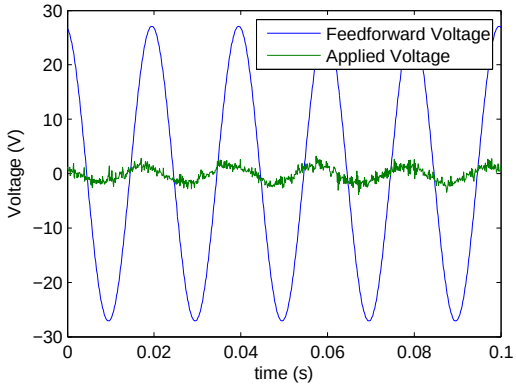
The current limiting system was tested by applying a short circuit to the inverter terminals, setting the inverter current demand to zero, and measuring the resulting current and voltage. The voltage signal fed forward to the inverter of one module was also recorded, along with the actual voltage value used after the actions of the current proportional controller are added. The results are shown in Figure 9.15.

It is clear that a higher proportional gain results in a lower current flowing (the current demand is zero), but a greater level of noise in the applied voltage signal. When a proportional gain of 12 is used, the system occasionally experiences large voltage ripples as stability is temporarily lost.

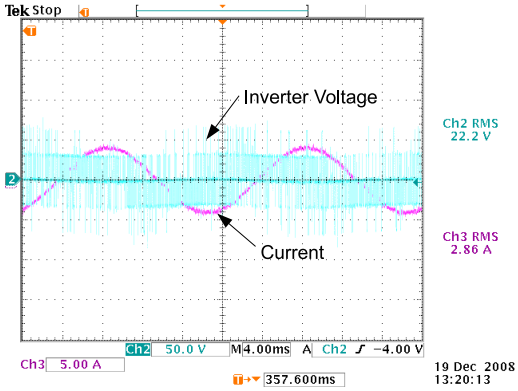
To test the activation of the current limiting controller during fault conditions, the inverter was connected to a loadbank and run in normal operation, and the load adjusted to achieve a current of around 4A rms. The loadbank was then short-circuited, and the current and voltage recorded. The results are shown in Figure 9.16 and show a strong correspondance to the simulated current and voltage in Figure 9.14.



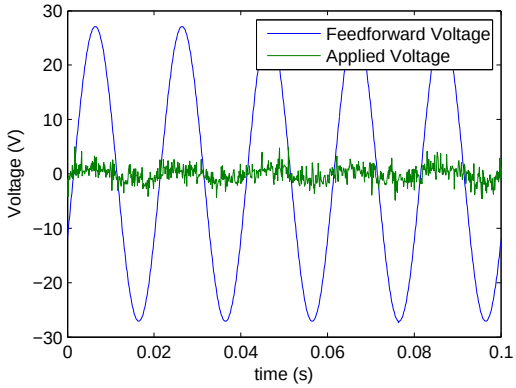
(a) Inverter voltage and current, Kp=4



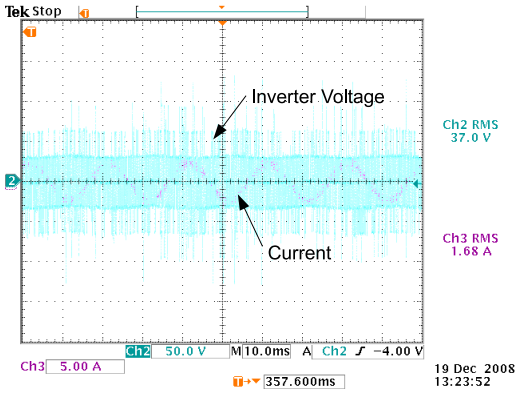
(b) Feedforward and actual voltage signals, Kp=4



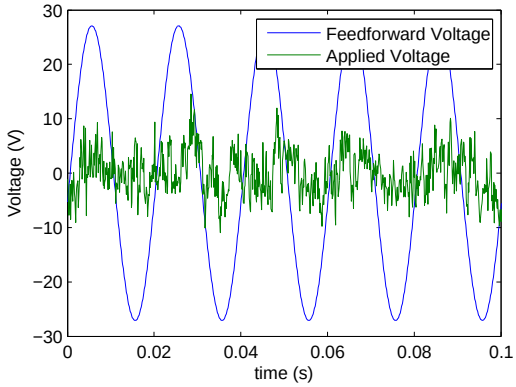
(c) Inverter voltage and current, Kp=7



(d) Feedforward and actual voltage signals, Kp=7



(e) Inverter voltage and current, Kp=12



(f) Feedforward and actual voltage signals, Kp=12

Figure 9.15: Inverter voltage and current with shorted terminals and different proportional gains

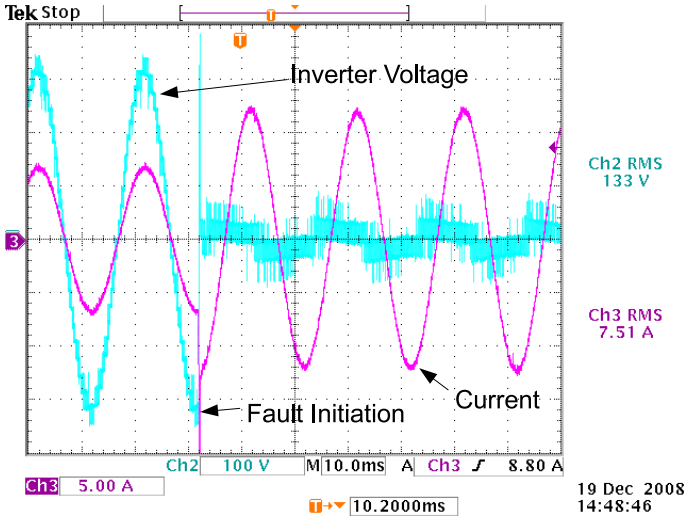


Figure 9.16: Inverter voltage and current, emulated grid fault conditions

9.5 Grid Voltage Estimation and Loop Filter Characteristics

The grid voltage reference loop was introduced in Section 9.3, and maintains reference values for the grid voltage angle and magnitude, $\hat{\theta}_g$ and $\hat{V}_g$, based on the estimated grid voltage and the grid voltage references of the other modules. The operation of the grid voltage angle and magnitude estimator, and the loop filter, are covered in this section.

Estimation of the grid voltage is similar to the system used in [46] and the rectifier controller, which uses the inverter current and voltage to estimate the grid voltage, and relies on converting these quantities to a rotating reference frame based on the module's grid voltage reference angle. The single phase structure of the inverter means that conversion between the fixed and rotating reference frames requires additional filtering.

9.5.1 Reference Frame Transformation and Filtering

Conversion of the single phase quantities, represented as v, to the rotating reference frame quantities V_d and V_q, fixed to the grid voltage reference angle θ_g, is carried out using Equation 9.3, with the reverse transformation given by Equation 9.4. The output of Equation 9.3 will include a significant second harmonic ripple of 100Hz, and this must be filtered so as not to cause interference.

$$\begin{bmatrix} V_d \\ V_q \end{bmatrix} = \begin{bmatrix} \cos\theta_g \\ \sin\theta_g \end{bmatrix} v \tag{9.3}$$

$$v = V_d \cos\theta_g + V_q \sin\theta_g \tag{9.4}$$

The filter must have a high attenuation at the targeted second harmonic frequency, as the second harmonic ripple will be larger than the signal of interest. In order to allow the grid voltage estimation PLL to have a high bandwidth, the filter itself must have a high bandwidth, meaning a high cut-off frequency. However the latency must also be low, meaning that a multi-pole filter is unsuitable. A notch filter is therefore proposed, which will offer an almost infinite attenuation at one frequency, i.e. 100Hz. This system assumes that the grid frequency does not vary significantly, which is a valid assumption.

A suitable notch filter, to be implemented digitally in the 1kHz software interrupt of the microcontroller, is given in Equation 9.5, and the frequency characteristics in Figure 9.17. The filter zeroes were placed to give infinite attenuation at 100Hz, while the poles are those of a 2nd order butterworth low pass filter with a cutoff frequency of 50Hz, to give some extra attenuation above 100Hz.

$$F(z) = \frac{0.2104(z^2 - 1.618z + 1)}{z^2 - 1.561z + 0.6413} \tag{9.5}$$

9.5.2 Grid Voltage Estimation

Estimation of the grid voltage position V_g, relative to the reference position used for feedforward calculation $\hat{V}_g$, is shown in Figure 9.18 and Equation 9.6.

$$\begin{bmatrix} V_{gd} \\ V_{gq} \end{bmatrix} = \begin{bmatrix} V_d \\ V_q \end{bmatrix} - \begin{bmatrix} R & 0 \\ 0 & R \end{bmatrix} \begin{bmatrix} I_d \\ I_q \end{bmatrix} - \begin{bmatrix} 0 & -\hat{\omega}L \\ \hat{\omega}L & 0 \end{bmatrix} \begin{bmatrix} I_d \\ I_q \end{bmatrix} \tag{9.6}$$

The exact structure of the grid angle and voltage reference loop depends on which current controller is being used. If the simple voltage feedforward controller is used, then the reference loop and current controller will have the structure shown in Figure 9.19a, with the CAN bus inter-module synchronisation system not shown. If

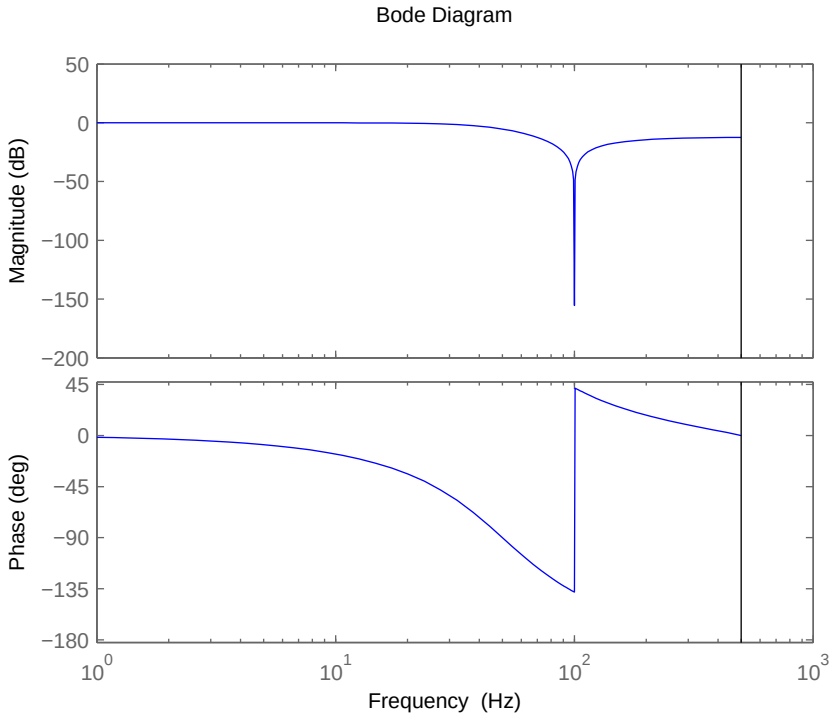


Figure 9.17: 100Hz notch filter frequency characteristics

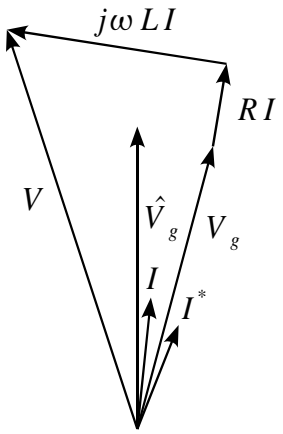


Figure 9.18: Inverter phasor diagram

the current limiting controller is used, then the reference loop and current controller will have the structure shown in Figure 9.19a.

The grid voltage is estimated using Equation 9.6. The grid currents in the rotating reference frame, I_d and I_q, are found by transforming the inverter current i using the transformation described in the previous section. If the feedforward controller is used, then the inverter output voltages V_d and V_q will be the inverter feedforward voltages, in the rotating reference frame, calculated in the previous cycle. If the current limiting controller is used, the inverter output voltage v_{fbk} must be calculated from the applied duty cycle d_{fbk}, and converted to the rotating reference frame. The grid frequency reference, $\hat{\omega}$, is assumed to be constant at 50Hz.

The estimated grid voltages V_{gd} and V_{gq} (not shown in the diagram) are used to calculate the estimated grid voltage magnitude, $\hat{V}$, and phase error e of the module's grid voltage angle reference $\hat{\theta}$ relative to the estimated grid voltage angle. This error is fed into the loop filter, which produces a reference value for the grid frequency $\hat{\omega}$, which is integrated to obtain the grid reference angle $\hat{\theta}_g$.

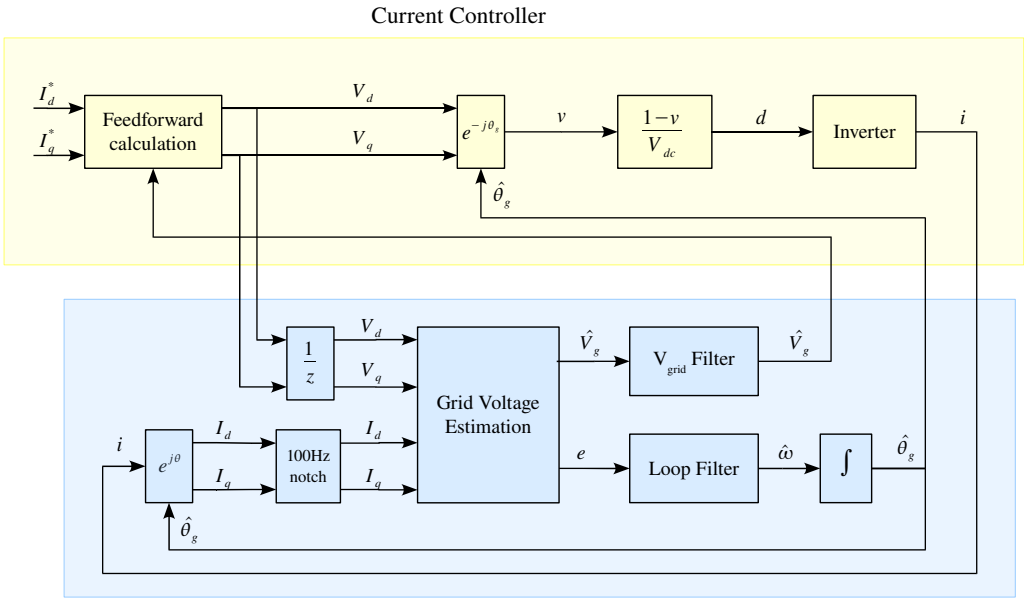
9.5.3 Loop Filter Design

The presence of the notch filters in the phase detector means that their transfer functions must be considered in the design of the PLL loop filter. The loop filter will be based on a PI controller, as with the rectifier PLL, but as the notch filters have a digital implementation the PI controller will be designed in the digital domain for improved performance.

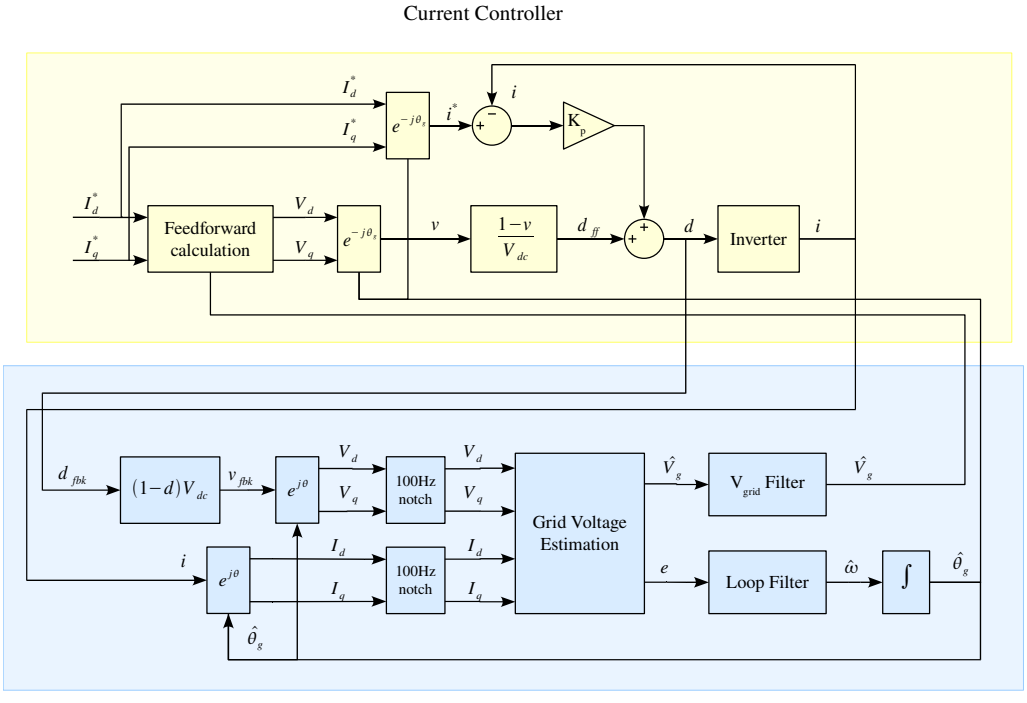
The root locus of the notch filter, PI controller and grid reference integrator are shown in Figure 9.20, with the loop gain varied from 10^{-4} to 10^{2}, and in greater detail in Figure 9.21. A backward-difference integrator is used for the PI controller. The PI controller zero is placed at 0.965, and a loop gain of 0.074 gives a system bandwidth of 30Hz, along with a damping ratio of 0.707, without excessive interactions with the notch filter. The resulting PI controller structure (including gridreference integrator) is given in Equation 9.7. The response of the system to a step in grid angle is shown in Figure 9.22.

$$C(z) = \frac{0.074(z - 0.965)z}{(z-1)^2} \tag{9.7}$$

Conversion of the PLL controller parameters to values used by the microcon-



(a) Control loop, voltage feedforward mode



(b) Control loop, current limiting mode

Figure 9.19: Inverter grid voltage angle and magnitude estimation loop, with current controller

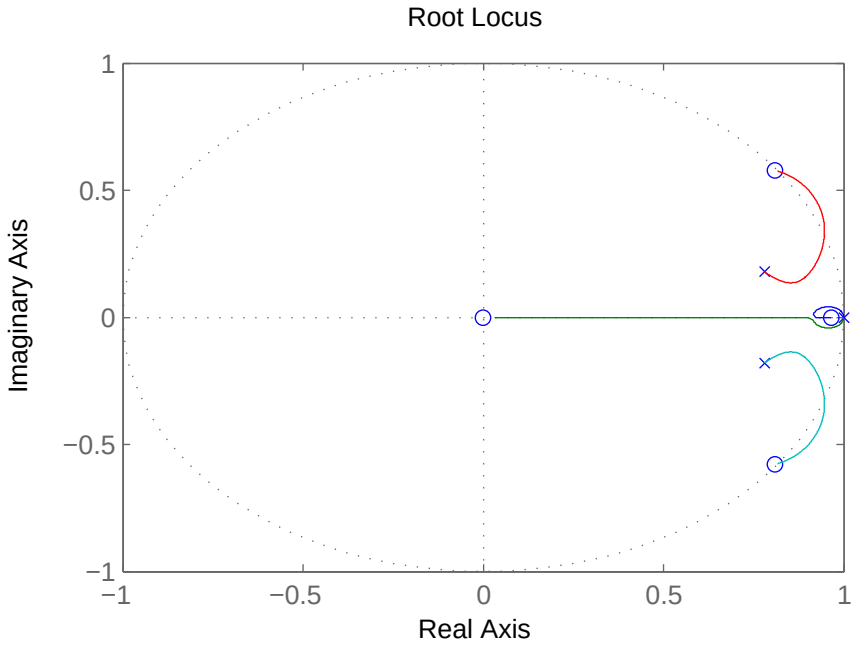


Figure 9.20: Root locus of grid reference PLL

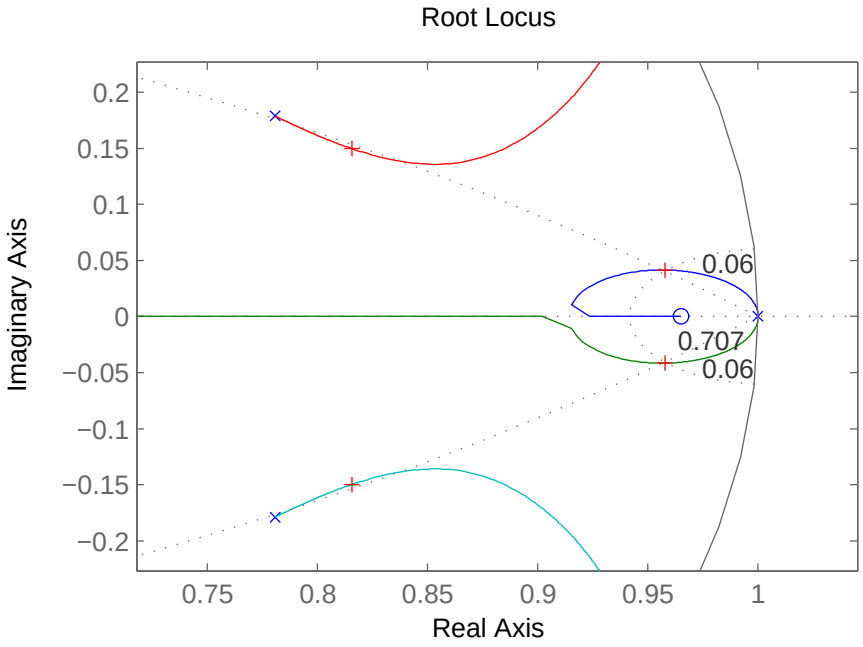


Figure 9.21: Detail of grid reference PLL root locus

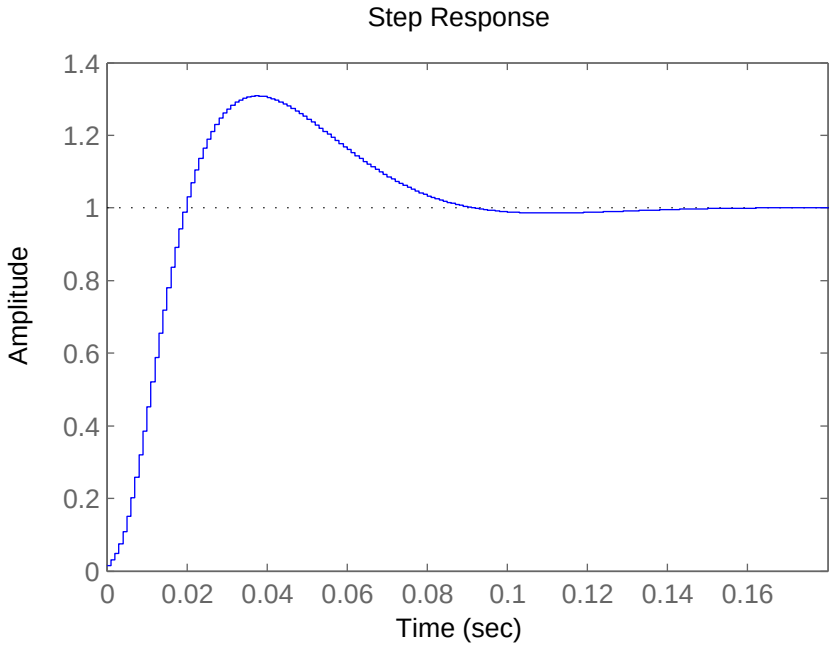


Figure 9.22: Grid PLL step response

troller was carried out in the same way as for the rectifier PLL, as described in Section 7.10.2, and implemented as a difference equation, shown in Equation 9.8. In this equation, x_1 is the phase error from the grid phase detector and x_2 is the phase error relative to other modules, and the output of the controller is y. $x(k)$ represents the current value of variable x, while $x(k-1)$ represents the previous value.The control parameters are the same for both inputs, meaning that the controller is given an equal priority to track the estimated grid angle from it's own estimator and from other modules.

$$y(k) = 298x_1(k) - 288x_1(k-1) + 298x_2(k) - 288x_2(k-1) + y(k-1) \qquad (9.8)$$

9.5.4 Grid Voltage Magnitude Estimation Filter

The grid voltage magnitude estimation filter has the form of an integral controller, as described in Section 9.3, and the controller has the open loop transfer function shown in Equation 9.9. The loop gain was set to give a bandwidth of approximately 50Hz, which leads to the step response shown in Figure 9.23, which also includes the step response with the grid voltage estimator notch filter on the input. The notch filter has a small effect on the step response, but does not introduce any unwanted

oscillations or instability.

$$C(z) = \frac{0.0912z}{z - 1} \tag{9.9}$$

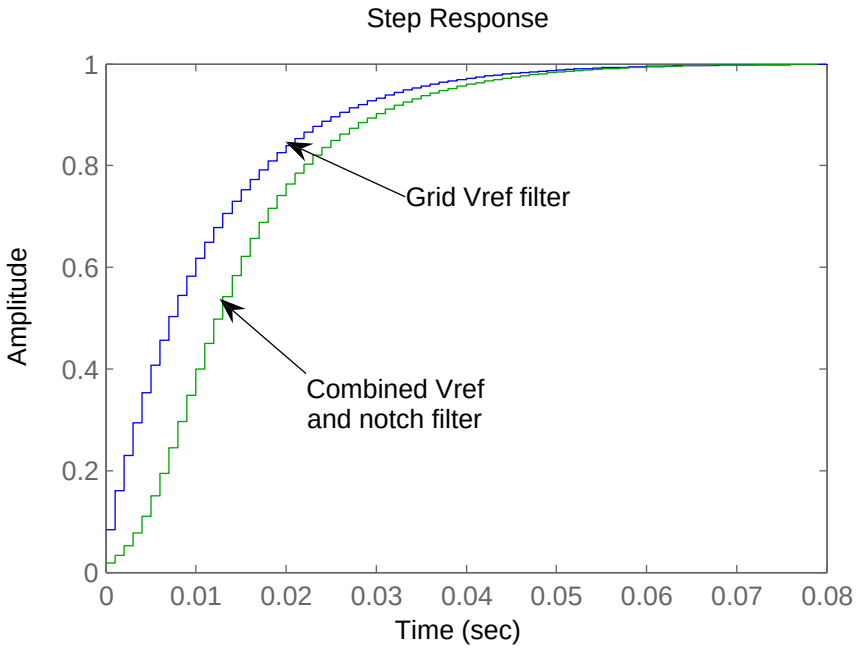


Figure 9.23: Grid voltage reference step response

The difference function of the integral controller is shown in Equation 9.10, where x_1 is the voltage error compared with the estimated voltage, and x_2 the error compared with the estimated voltages from other modules. As with the grid angle reference, the voltage reference uses the same parameter values for the module's voltage estimator and those of the other modules. The control parameter is represented as a fraction of 2^{16}, where the input x is multiplied by the control parameter, then barrel shifted 16 bits to the right, representing a division by 2^{16}.

$$y(k) = \frac{5977}{2^{16}}x_1(k) + \frac{5977}{2^{16}}x_2(k) + y(k-1) \tag{9.10}$$

9.5.5 Testing of Inverter Grid Voltage Tracking

The transient performance of the grid voltage position and magnitude can be gauged when locking the inverter onto the grid voltage. As mentioned in Section 9.4, the inverter locks on to the grid voltage by connecting the inverter to the grid without first synchronising the grid reference with the grid voltage. When this happens,

the current proportional controller must limit the inverter current until the grid reference has locked onto the estimated grid voltage.

In the lock-on test, the inverter and grid voltages and the current were recorded using an oscilloscope. The frequency and voltage as estimated by four modules were recorded by the modules, and the DC-link voltages recorded by three more modules. The results are shown in Figure 9.24.

The grid angle reference takes several cycles to lock onto the grid angle, with the rate limited by the limits placed on the reference frequency range. Increasing the frequency range would result in a faster lock-on performance. During the lock-on process a significant current flows, due to limits of the capacity of the current proportional controller to limit the current. The DC-link voltage rises significantly due to this current, so this synchronisation method would not be suitable for a full-size system with a lower tolerance for overvoltage.

The grid voltage magnitude and angle estimations of the tested modules are the same, so the assumption that all modules will act in the same way, made when the modular grid voltage tracking system was proposed, is validated.

9.6 Additional System Testing

9.6.1 Grid Connection Steady State Operation

Steady state testing of the system with grid connection was carried out using the system described in Section 7.8, without the DSpace controller and using PWM instead of fundamental switching. The operating conditions outlined in Table 8.5 were tested for unity power factor operation. For operation with reactive power, the conditions described in Section 8.5.2 were tested. The system was tested using both the current limiting mode, with the current proportional controller activated, and the normal operation mode, with only feedforward voltage to control the current.

In both operation modes, it was found that even with zero inverter real power demand, the inverter output current was greater than the current for the 3m/s wind condition. This current is mostly in the form of third harmonics, due to the distorted grid voltage. Because of this, the 3m/s wind condition will be ignored in these tests. The 9mH grid coupling inductance, used in the previous chapter, was also used in these tests.

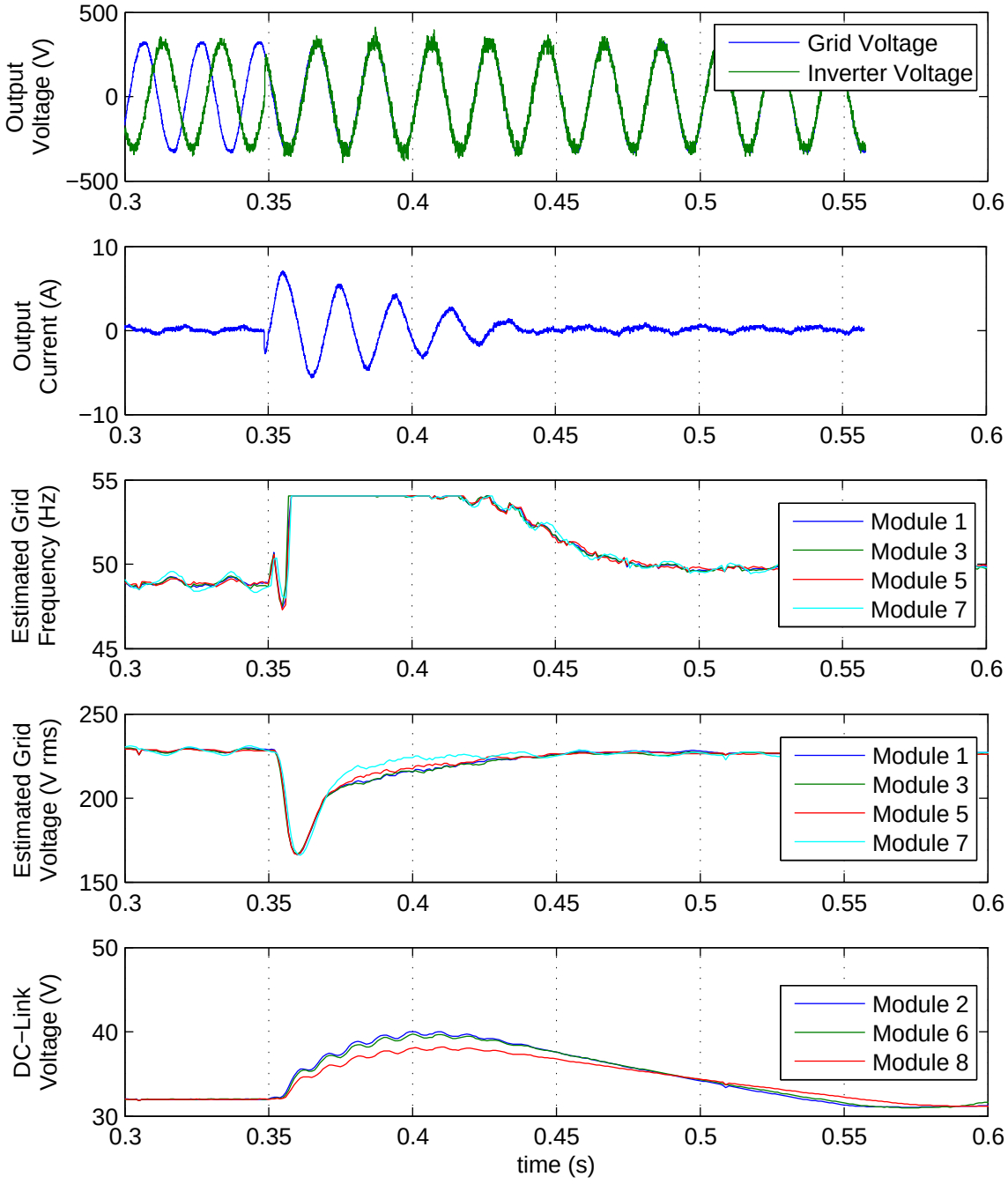


Figure 9.24: Locking of inverter onto grid voltage

Current Limiting Mode

Current and voltage waveforms for the various operating conditions are shown in Figure 9.25. The distorted grid voltage results in a distorted inverter current, as with the fundamental frequency operation tested in the previous chapter, and the current proportional controller is not able to fully control this current to be sinusoidal. The inverter current is much less distorted at higher powers.

For a given proportional gain in the current controller, the inverter current becomes unstable at higher values of current demand. For this reason it is necessary to vary the proportional gain depending on the curent demand. The proportional gains used for the different operating conditions are shown in Table 9.1, and an example of the inverter current with a gain that is too high is shown in Figure 9.26.

As a high proportional gain is required when synchronising the inverter with the grid voltage, in order to limit the current while synchronising, the proportional gain must be varied with the inverter current rather than having a low gain over the entire current range.

Wind Speed Condition	Inverter RMS Current	Proportional Gain
No Load	0 A	7
6m/s	1.28 A	7
9m/s	4.32 A	4
12m/s	10.9 A	1

Table 9.1: Current controller proportional gains used

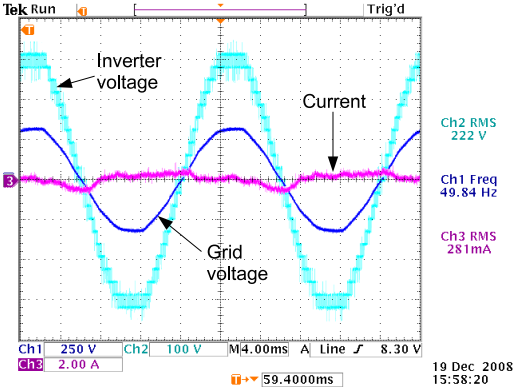
Normal Operation

The inverter voltage and current for normal operation of the inverter is shown in Figure 9.27, and show a slightly lower distortion than with the fundamental frequency switching, particularly around the peaks of the waveform.

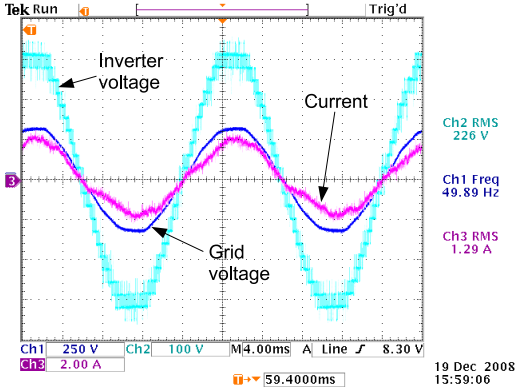
9.6.2 Fault Ridethrough Operation

The ability of the inverter to ride through a grid fault without damage depends on several factors:

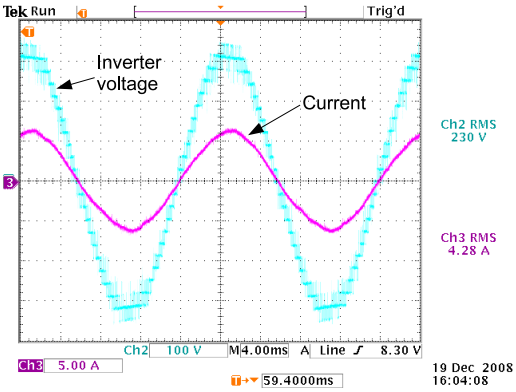
- Limiting the current immediately after the fault. The ability of the current proportional controller, distributed across all 12 modules, to achieve this was



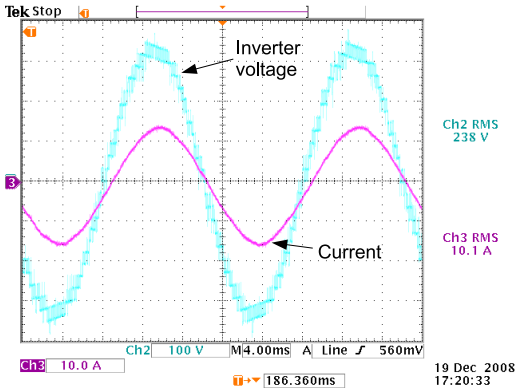
(a) Current and voltage, no load condition



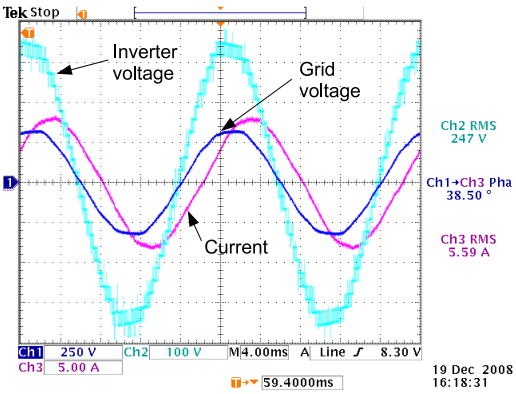
(b) Current and voltage, 6m/s wind condition



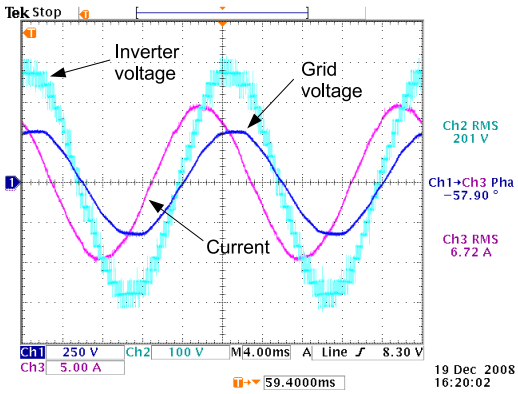
(c) Current and voltage, 9m/s wind condition



(d) Current and voltage, 12m/s wind condition



(e) Current and voltage, 9m/s condition, lagging power factor



(f) Current and voltage, 9m/s condition, leading power factor

Figure 9.25: Inverter voltage and current with grid connection and current-limiting operation

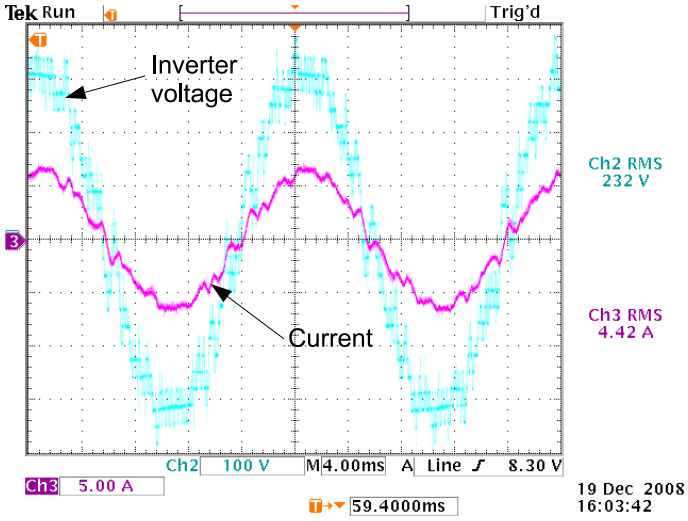


Figure 9.26: Inverter current and voltage, 9m/s wind condition and current-limiting operation, with unstable proportional gain value (Kp=5)

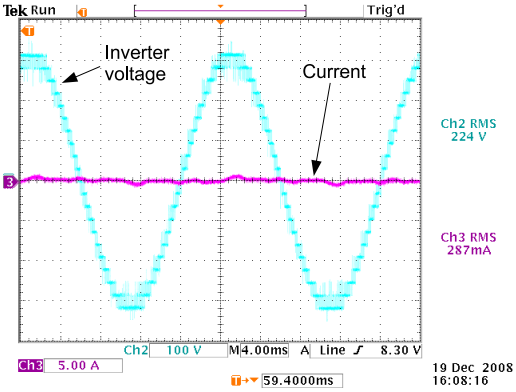
demonstrated in Section 9.4.

- Adjusting the grid voltage magnitude reference to reflect the sudden drop in grid voltage.
- Controlling the DC-link voltage when the drop in grid voltage causes the inverter power to suddenly drop.
- Maintaining synchronisation with the grid with a reduced voltage, or re-synchronising with the grid voltage when the fault is cleared.

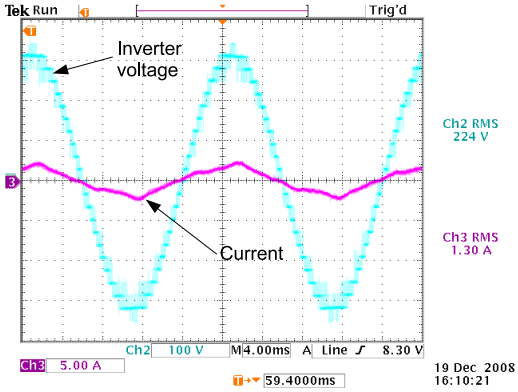
Testing was carried out using a resistive loadbank and 3mH coupling inductance, with the resistance varied to achieve a current of approximately 4A. The grid voltage angle estimator was not used, as there is no grid voltage present, but the voltage magnitude estimator was used. A grid fault was emulated by short-circuiting the loadbank, which appears to the grid voltage magnitude estimator as a drop in the grid voltage.

Maintaining synchronisation and re-synchronising cannot be tested with this arrangement, but the ability of the inverter control system to quickly synchronise with the grid voltage has already been tested. The grid fault performance is shown in Figure 9.28.

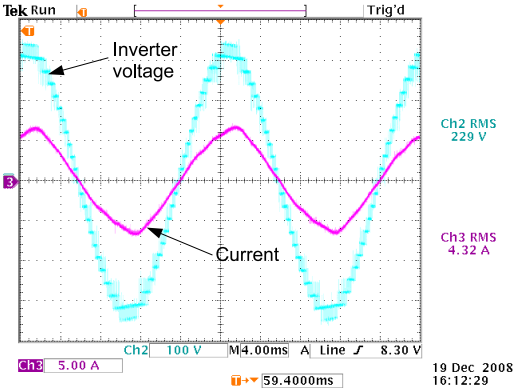
At the start of the fault, the the current rapidly rises to 20A, activating the current limiting mode, which reduces the current. The current is still higher than



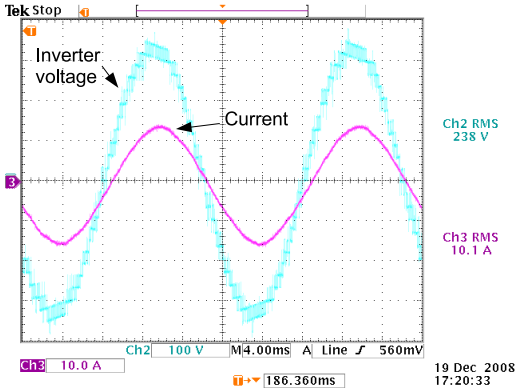
(a) Current and voltage, no load condition



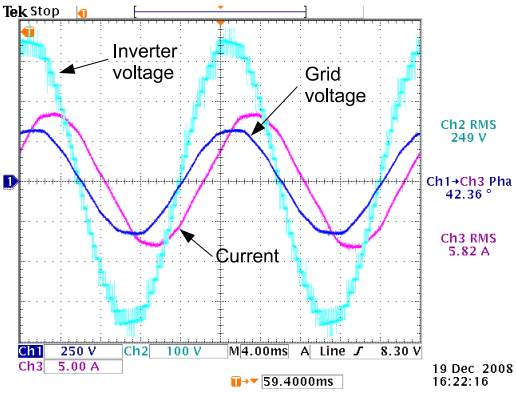
(b) Current and voltage, 6m/s wind condition



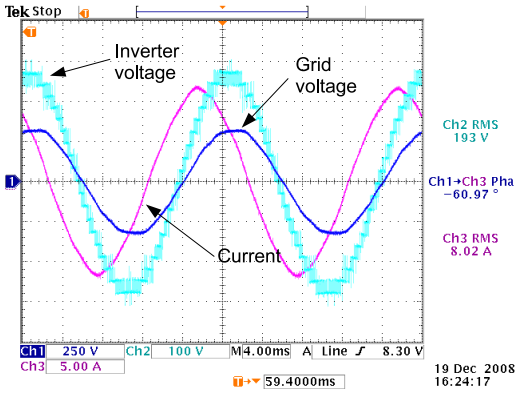
(c) Current and voltage, 9m/s wind condition



(d) Current and voltage, 12m/s wind condition



(e) Current and voltage, 9m/s condition, lagging power factor



(f) Current and voltage, 9m/s condition, leading power factor

Figure 9.27: Inverter voltage and current with grid connection and normal operation

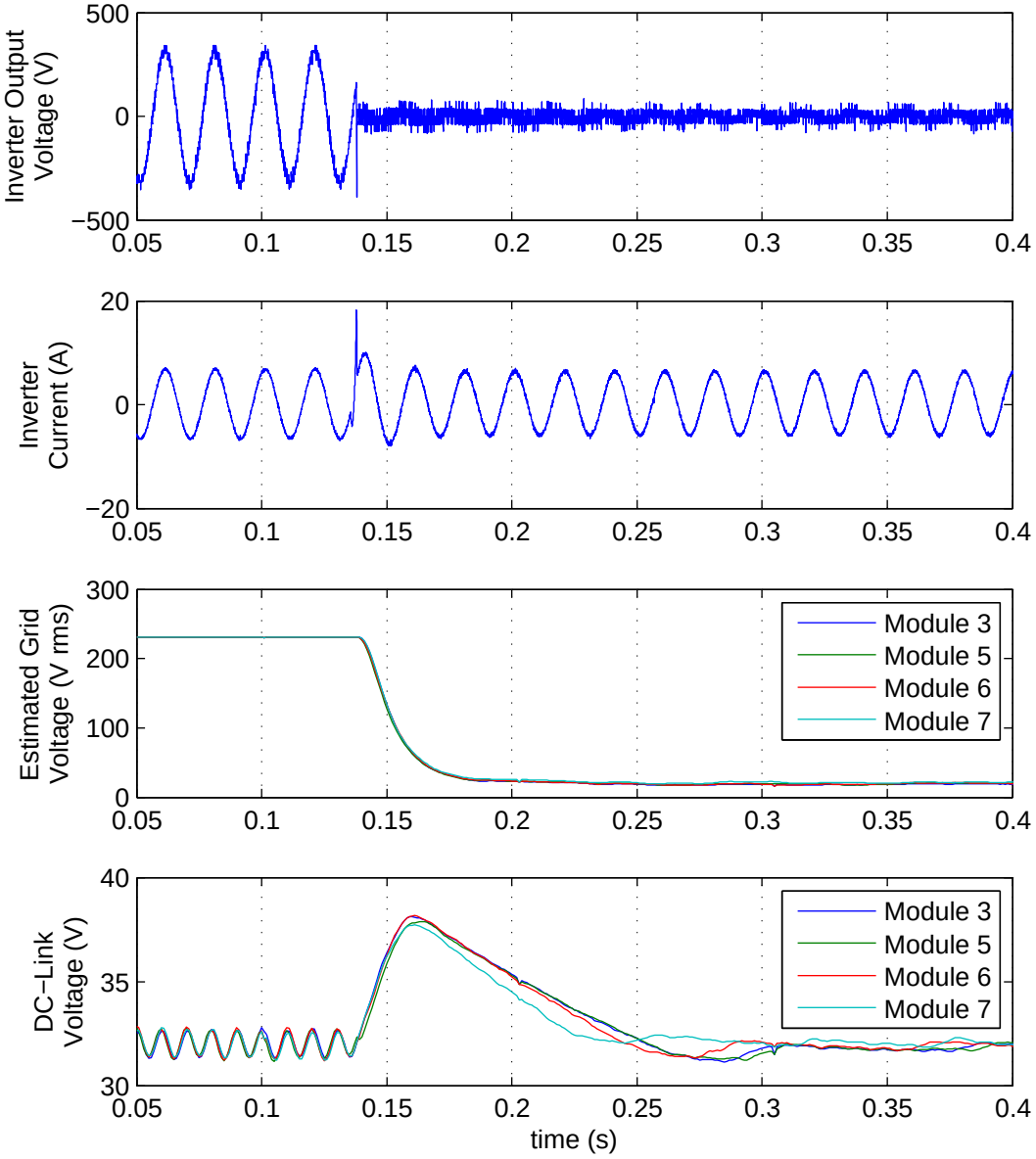


Figure 9.28: Inverter grid fault ridethrough

needed, due to the steady state error of the current controller, but estimated grid voltage drops over several cycles, meaning that the correct feedforward voltage is then applied, and the current reduces back to the desired value.

The DC-link voltage immediately rises due to the lower output power, and is gradually reduced when the DC-link voltage controller reacts. The DC-link voltage still rises by 6V, or 19%, which could damage a full-size system less able to withstand the overvoltage, so a faster controller would be required. The speed of the DC-link voltage controller is limited by requirement to filter out the 100Hz voltage ripple from the inverter. A faster controller could be used when the inverter is in the current limiting mode, which would reduce the voltage rise, but would filter the DC-link voltage ripple less effectively.

An aspect of the control system not implemented is to raise the inverter current to compensate for the drop in grid voltage. This can be done to keep the power flow constant, up to the current limit of the inverter, and will also help to activate any protection systems in the power network.

9.6.3 Power Sharing

Power sharing between modules, for fundamental and PWM switching, is shown in Figure 9.29. While the asymmetrical half-cycle switching scheme used for fundamental switching has improved power sharing, compared with other fundamental switching schemes, the PWM switching scheme offers much better power sharing.

9.6.4 Module Fault Tolerance

Tolerance of a module fault relies on being able to adjust the inverter output voltage to compensate for the lost module, and to change the PWM timing to interleave the PWM switching of the modules. Changing the output voltage with a fundamentally-switched inverter requires the DC-link voltage to be increased, but with a PWM inverter the only requirement is to change the duty cycle of the switching.

The voltage and current waveforms for normal operation, at the 9m/s operating condition, are shown in Figure 9.30a. The voltage and current with an uncorrected module fault are shown in Figure 9.30b, and with a corrected fault in Figure 9.30c.

The dynamic reaction to a module fault is shown in Figure 9.31. The grid voltage magnitude estimation increases quickly, as the loss of a module appears to the

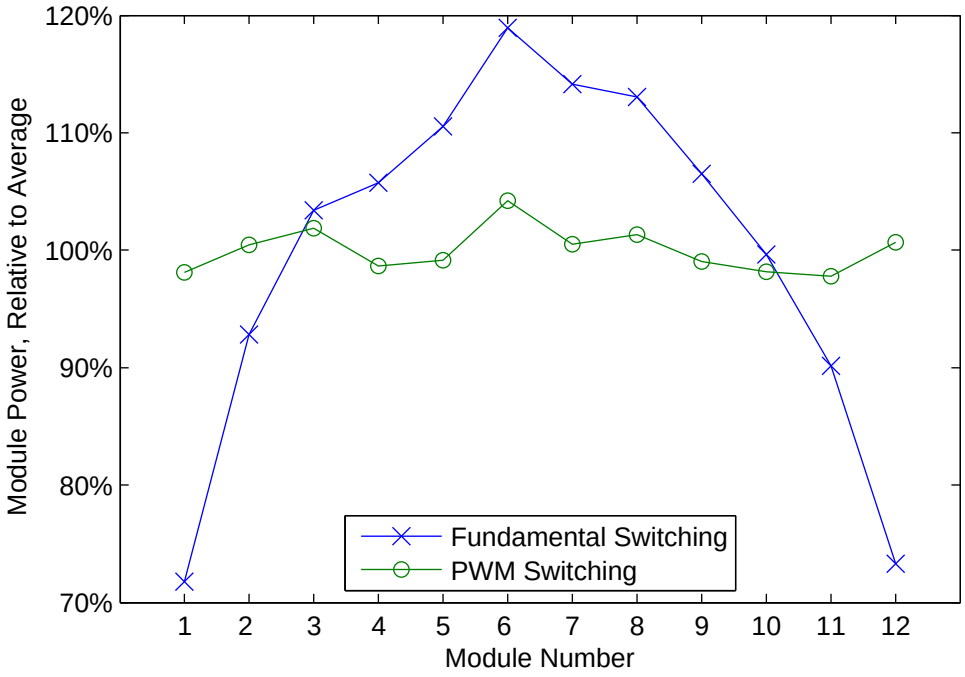
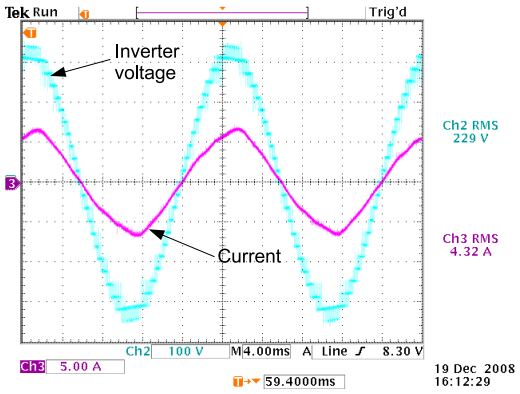
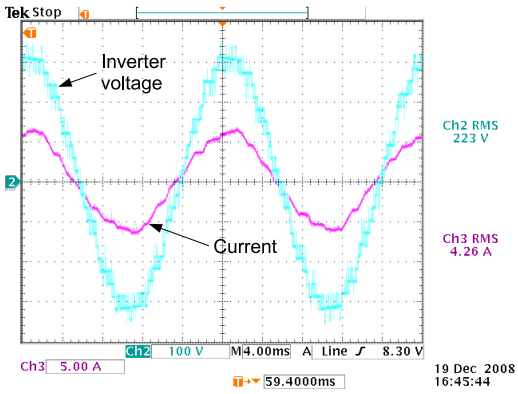


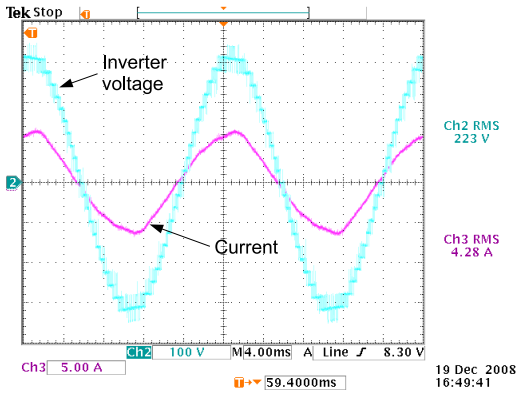
Figure 9.29: Inverter module power sharing



(a) Pre-fault operation



(b) Uncorrected module fault



(c) Corrected module fault

Figure 9.30: Inverter current and voltage waveforms with and without module faults, 9m/s wind condition

remaining modules as an increase in grid voltage. This keeps the current magnitude under control. The interleaving of the module PWM carriers then corrects to compensate for the lost module, which occurs over a period of around 0.3s.

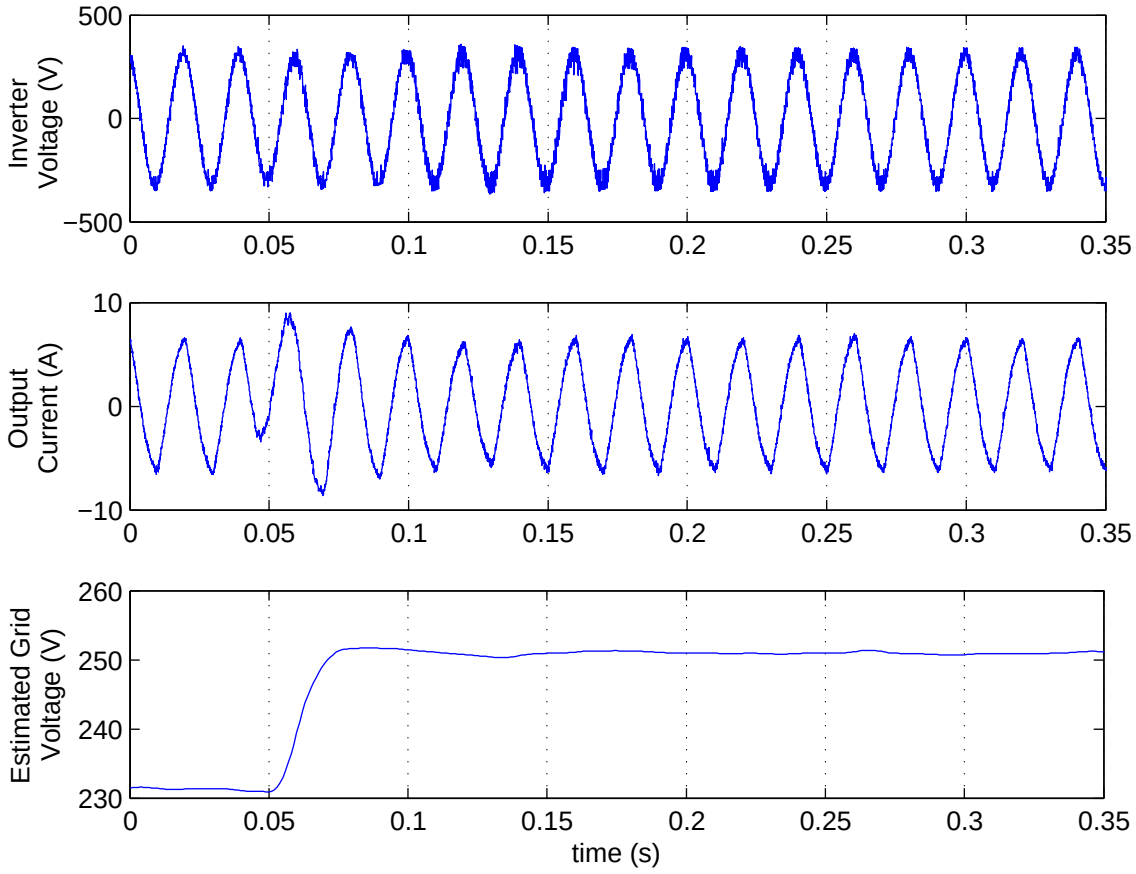


Figure 9.31: Reaction of the inverter to a module fault

9.7 Conclusion

In this chapter, a distributed control system for the prototype system described in chapter 7 has been developed. The system is capable of tracking the grid voltage, and setting the feedforward voltage to achieve the desired current, and the estimated grid voltage angle and magnitude is synchronised between modules using the CAN bus.

The most important aspect of the control system is the distributed current limiting scheme, which is necessary to limit the inverter current in the event of a grid fault. Immediately after a grid fault, the current will rise rapidly due to the low grid coupling inductance of the inverter, and the standard method grid fault ride-

through, where the central controller sees the drop in grid voltage and commands a lowering in inverter voltage, will not be fast enough. A proportional controller is used in each module to vary the inverter PWM duty cycle, to force the current to follow the desired waveform, and limits the current until the grid voltage observer is able to adjust to the new grid voltage.

The current limiting schemme relies on all the modules sampling the inverter current and changing their PWM duty cycle simultaneously, which is tied in to the interleaving of the PWM carrier signals of the different modules. Interleaving of the PWM carrier signals is done using the CAN bus, in a distributed fault-tolerant way, and could potentially be extended to many other modular power electronic applications.

Grid fault ridethrough of the inverter has been achieved, using a loadbank and the distributed grid voltage estimator. The current limiting controller is activated when the grid fault occurs, and successfully limits the current until the grid voltage observer can react to the reduced voltage.

Immediately after the fault, the DC-link voltages of the modules rise rapidly, due to the time taken for the DC-link voltage controller to react to the lower power drawn by the inverter, and this could damage a full size system less able to tolerate overvoltage. A faster DC-link voltage controller could be used while the current limiter is active, but this would not effectively filter the 100Hz DC-link voltage ripple from the rectifier current demand signal.

A distributed method of tracking the grid voltage, and setting the inverter feed-forward voltage appropriately, was also devised. This system uses a known method of tracking the grid voltage without using voltage sensors, which is implemented in all modules, and relies on the modules all behaving in a similar way, which should happen if they are sampling the inverter current simultaneously. The estimated grid voltage angle and voltage are synchronised between modules using the CAN bus.

Testing using the prototype system has verified that the voltage-sensorless grid voltage tracking system works when distributed across the 12 modules of the prototype system. The system quickly reacts to changes in the grid voltage, and can quickly lock on to the grid voltage position when first connected.

The series nature of the inverter means that the method of locking on to the terminal voltage used in the rectifier, where short pulses are applied to the switching

devices and measuring the rate of change of current, cannot be used in the inverter. Because of this the inverter must be connected without first being synchronised with the grid, which relies on the current limiting controller to limit the current until the inverter voltage reference is synchronised with the grid voltage. This can result in significant currents flowing, which could raise the module DC-link voltages to a level that would cause the modules to fail, and this method is less than ideal.

The method of applying short pulses to the switching devices cannot be used as it is not possible to ensure that the switches in each module will switch simultaneously. This means that the last switch to remain open would have the entire grid voltage across it, which would cause it to fail. A zener diode, or similar device, across the module terminals would clamp the voltage, protecting the switching devices, allowing this method of finding the grid voltage position to be used. As mentioned in chapter 5, such voltage clamping devices will be required for lightning strike protection.

The distributed system is also able to handle the sudden fault of a module, with the grid voltage observer raising the voltage output demand of each module, and the PWM carriers re-interleaving automatically to compensate for the lost module.

Distributed current limiting is necessary even if a central controller is used, due to the low grid coupling inductance that is planned for the inverter, and the rapid rates of change of current that this permits. Distributing the grid voltage and current observer system between modules, and thus eliminating the need for a central controller, is less essential, but offers advantages in terms of fault tolerance.

The distributed control scheme described in this chapter has been shown to be viable using the prototype system, but needs to be simulated in a larger system. In particular, the requirements for the sampling speed of the current controller need to be determined, this will relate to the grid coupling inductance used.

The system was tested using a single phase inverter, and relies on treating a full-size three-phase inverter as a set of independent single phase inverters. A more complex system could be implemented which synchronises the PWM waveforms between three phases, and copes with unbalanced grid faults by measuring the positive and negative phase sequence grid voltages using a distributed system. Such a system would have a higher complexity, but would operate on the same principles as described in this chapter.

Chapter 10

Conclusion and Discussion

As well as summarising the findings of the project, this chapter also aims to discuss a number of issues encountered in the course of the project. Chief among these is the question of the viability of the power electronics architecture under investigation, which was based upon the promise of lower cost, increased reliability and fault tolerance, and increased efficiency compared with commonly used systems.

The second issue for discussion is the viability of the entire concept of a modular lightweight direct-drive generator, connected to a modular power conversion scheme, for wind turbine applications. While the viability of the complete system is not the topic of this thesis, it is a question that has been asked often in the course of the project, and the choice of power conversion scheme has an impact on the viability of the system.

Finally the further work that could be carried out based on the findings of this project, and the generator and power conversion system in general, will be discussed.

10.1 Summary of the Project Findings

A lightweight direct drive generator for wind turbine applications has been proposed. The use of an airgap winding, with individually encapsulated modular coils, and permanent magnets, gives significantly lower airgap forces than slotted iron-cored generators, allowing a lighter weight structure, and lower costs.

A modular power conversion scheme has been proposed, based on a number of identical modules, each of which is connected to two generator coils. The outputs of the modules are an H-bridge, and the module outputs are cascaded to form

a cascaded multilevel inverter. This system can produce a high voltage output, of 11kV, while keeping the module voltages low, allowing standard components to be used and eliminating the need for a grid coupling transformer. Having each module in the inverter driven by separate coils allows each DC-link to be individually controlled, eliminating the DC-link balancing problem in multilevel inverters with a large number of levels.

In the second chapter, a power conversion scheme was devised for a small scale wind turbine for battery charging connection. A boost converter is used to increase the speed range of the turbine, which is normally limited by the fixed battery voltage, and results in a significant increase in annual power capture, particularly with a low average wind speed.

The concept of turbine speed range and power extraction was applied to the proposed large-scale power conversion system in chapter 3. Several module topologies were considered, with a system having a boost rectifier input, and an inverter output with each modules switching at the fundamental frequency, was found to have the greatest speed range, and therefore the greatest power extraction. Systems with a passive rectifier input were found to have a much more limited speed range.

A more detailed analysis of the design of the different modules described in chapter 3 was carried out in chapter 4, in order to find the relative costs and efficiencies of the different designs. The systems with the boost rectifier input were found to have a slightly higher cost than those with a passive rectifier input. The boost rectifier systems were found to be more efficient as, although the power electronic losses are higher, the sinusoidal coil current of the boost rectifier systems results in a much lower coil resistive loss. For this reason a system with boost rectifier-based modules was decided upon for further analysis.

Much of the justification for the proposed power conversion scheme, using a modular cascaded multilevel inverter, is based on having a high voltage output, eliminating the need for a grid coupling transformer. This depends on the ability of the generator and power electronics to operate at the required voltage, which was analysed in chapter 5. The casing and heatsinks of the power electronic modules will be at the module's local ground voltage, and the main potential insulation problem is corona discharge between the module heatsinks and the generator structure, which should be minimal. Insulating the generator coils to the amount required, relative

to the stator back iron which will be earthed, will increase the size of the generator airgap as well as reduce the effectiveness of the module cooling, relative to a system operating at a lower voltage.

A control system for the modules was described in chapter 6. The rectifiers are controlled by applying a feedforward voltage to the coils to achieve the desired current, and using a proportional controller to eliminate distortion around the zero-crossings of the coil current. A PLL-based system estimates and tracks the generator EMF position based on the coil currents, to ensure that the correct current is drawn. The coil current demand is controlled to keep the DC-link voltage constant, and the DC-link voltage controller features a filter which eliminates the voltage ripple due to the inverter from the voltage signal, preventing it from being transferred to the coil current demand.

The switching of the inverter is based on having the inverter output of each module switch at a particular time in the grid voltage waveform, such that a sinusoidal output is produced when the modules are cascaded. This reduces the switching losses compared to PWM switching as each module is switching at the fundamental frequency. The inverter is controlled by a central controller, which tracks the grid voltage and sets the inverter voltage and phase accordingly.

Chapter 7 describes a prototype system, built to test the power electronic concepts. The system is based on two 12-coil axial flux generators, driven by an induction machine, through a reduction gearbox. The generators are connected to 12 modules, housed in a separate rack, and built on plug in PCBs, for ease of access. The modules are controlled by a 32-bit microcontroller, and an isolated CAN bus used for synchronisation with the central controller, with an isolated RS485 bus used for monitoring and data acquisition. A DSpace control system is used as the system central controller.

Testing of the prototype system, in chapter 8, shows that the rectifier control system is able to correctly track the machine EMF, and draw a sinusoidal current in phase with that EMF. The DC-link voltage controller was able to filter out the DC-link voltage ripple from the inverter, and show good performance, although the performance varied with the operating conditions used. The inverter was able to produce a good quality sinusoidal output voltage, but distortions in the grid voltage meant that a distorted grid current was produced. The system was able to react to

the loss of a module by raising the DC-link voltage of the remaining modules, and adjusting the switching times of the module inverter outputs to compensate for the lost module.

A decentralised inverter control scheme, based on PWM switching, was developed in chapter 9. The PWM carrier waveforms of all the modules were interleaved using the CAN bus, to give a higher apparent frequency, and a grid voltage estimation and tracking system implemented. The grid voltage tracking system was distributed across all modules, with the angle and voltage references synchronised over the CAN bus. A distributed current proportional controller was implemented in the modules, which allows the current to be controlled immediately after a grid fault, before the grid voltage reference system can react to the drop in grid voltage. The system shows good current control, and maintains a sinusoidal output voltage even at rated power.

10.2 Discussion of the Viability of the Power Conversion Architecture

The concept of a modular multilevel inverter, with each module driven by separate generator coils, and a high voltage output, was proposed based on a number of potential advantages:

- Greater reliability, as the inverter should be able to continue to function even with the failure of several modules. The modular system, where a large number of modules are manufactured from standard components, should also offer greater manufacturing consistency, and greater reliability.
- Greater efficiency, due to the high voltage output and elimination of the grid coupling transformer, as well as the permanent magnet generator.
- Lower cost, compared with other fully-rated inverters, again due to the large number of identical modules manufactured from standard parts.

The system has been shown to be workable on a laboratory prototype, although this system takes no account of the high voltage issues in a full-scale system. A problem encountered is that the ripple in the DC-link voltage of the modules, due

to the single phase inverter output, causes a distorted output voltage when the inverter is switched at the fundamental frequency. This distortion can be reduced by increasing the DC-link capacitance, but this is undesirable as the DC-link capacitors already make up a significant proportion of the module cost.

Distortion can be corrected by superimposing a PWM correction signal on the fundamental signal, based on a voltage error signal from a central controller, but this was found to be difficult to implement and ineffective at removing all distortion harmonics. Using pure PWM switching, with each module compensating for it's own DC-link voltage variation, was found to be effective at eliminating the distortion. A simpler solution is to simply leave the neutral point of the inverter unconnected, or grounded through a large resistor, which would prevent the third harmonic currents from flowing, these making up the majority of the distortion current.

Tolerance to the fault of a single module has been demonstrated, subject to the ability to bypass a faulted module, which justifies the suggested fault tolerance advantages of this system, leading to greater reliability. A fully distributed control system has also been demonstrated, which offers fault tolerance. Tolerance to a module fault is important as the mounting of the modules on the generator makes their replacement difficult, so they will need to last for the lifetime of the turbine.

Grid fault ride through has also been demonstrated, which is important in modern wind turbines. Fault ride through in this system requires PWM switching to be implemented, and a distributed system to limit the initial fault current. This is required because of the low grid coupling inductance leading to a potentially high rate of change of current, and the distributed current limiting system allows fault ride through without needing a large inductance and higher cost.

The high voltage output concept could not be tested using the laboratory prototype, but the use of a high voltage modular power electronic system was found to be viable from an insulation standpoint, with limitations existing mainly in the insulation of the generator coils rather than the power electronics. This conclusion is based on assumptions about the construction of the generator.

In terms of the advantages cited at the start of this section, tolerance to a module fault has been demonstrated, but the reliability of a module is not known. This is important as the modules are difficult to replace, and need to last for the lifetime of the turbine.

The high voltage output of the system is viable, in terms of the power electronics, so the grid coupling transformer can be eliminated, increasing the efficiency of the system. The use of boost rectifiers on the input of the modules has been shown to increase efficiency, and the system was estimated to have an electrical efficiency of around 95% in chapter 4.

No comparison of the power electronics cost with that of a single large converter has been made, as the manufacturing costs of the modules are not known. Using active filtering to eliminate the effects of the DC-link voltage ripple on the output voltage waveform means that a minimal DC-link capacitance, defined by the capacitor lifetime, is required, which reduces the module costs. Distributed current limiting means that a large output inductance is not required to limit the current in a grid fault, also reducing the cost.

10.3 Discussion of the Viability of the Generator System

While this project is not directly concerned with the design of the generator, the power electronic design is linked with the generator used, and has an impact on the viability of the generator concept. Although the modular lightweight iron-cored direct-drive generator with airgap windings does not exist, analysis of the high voltage issues of a potential design were carried out, and assumptions can be made as to the other characteristics of such a generator.

The use of an airgap winding in the generator means that each coil can be individually insulated, and the coils can have a high voltage relative to ground and each other while having a low inter-turn voltage. However it was found that the levels of coil insulation required for 11kV output would increase the airgap size significantly, reducing the airgap flux density and reducing the power output of the generator. Cooling effectiveness would also be reduced, limiting the generator torque capability and power output.

The calculation of insulation thickness was made based on the insulation dielectric strengths used in conventional slotted generators, and the more uniform electric field present in the insulation of a slotless machine could allow a higher dielectric strength to be used. Alternatively a lower voltage output could be used, with a grid

coupling transformer, with other benefits of the modular system still being present.

Having non-overlapping coils in the generator means that the mutual inductance between adjacent coils is low, so each coil can be treated as independent. This allows a modular power electronics approach to be used, providing advantages in terms of cost and reliability, as discussed previously.

A potential problem with lightweight direct-drive generators is that the large generator diameter, and lightweight structure, could mean that the airgap could vary considerably in size around the generator, with effects on the airgap flux density and coil EMF. Modular power electronics allows the current in each coil to be controlled, which eliminates the problems of airgap variation. This allows a lightweight structure, with lower manufacturing tolerance requirements, to be used, which will reduce the generator cost.

Another problem with the proposed generator design is that the coils have an extremely low inductance. When the coils are connected to a passive rectifier, this means that the resulting current waveform has a high crest factor, leading to high losses. Using a boost rectifier means that a sinusoidal current can be drawn, greatly reducing the losses and increasing the generator power capability.

In conclusion, a modular power conversion scheme greatly improves the viability of a lightweight direct-drive generator by eliminating the problems of airgap eccentricity and low coil inductance. Reliability should be improved compared with a conventional direct-drive system, and costs reduced. Even if the full 11kV output voltage cannot be achieved, and a transformer must be used, the other advantages will still remain.

The design of the generator allows the proposed power conversion scheme, with it's advantages, to be used, while the power conversion scheme mitigates many of the disadvantages of the generator design. It is clear that for an unconventional generator design the generator and power electronics must be considered together in order to obtain the maximum advantage from both.

10.4 Further Work

An important issue with this project is that a prototype lightweight iron-cored direct-drive generator with an airgap winding does not exist, and development has

mostly been based on a design spreadsheet for such a generator. This means that many potential issues, such as airgap eccentricity and structural rigidity can only be guessed at. Developing such a generator is therefore important in proving the proposed system to be viable.

A more detailed design for the structure of the generator will allow the insulation issues of the generator system to be analysed in greater detail, and potentially tested. It will also be useful to design and construct a full-size power module, in order to better work out the design issues involved, and to calculate the manufacturing costs. A study into how the module can be designed for the greatest reliability would be important.

A more detailed generator design and high voltage analysis will allow the coil insulation thickness to be calculated, which will allow an analysis of the turbine power handling capability to be determined. A compromise between the inverter output voltage and the generator power handling could then be made.

The control system has been designed based on a single-phase inverter, and must be adapted for use in a three-phase system. In particular, the system of PWM interleaving and current limiting will need adaptation. Grid fault ride-through will also work differently in three phases, involving the calculation of the positive and negative phase sequence voltages. It would also be useful to investigate the splitting of the control functions between the distributed and centralised controllers, based on performance, practicality and cost.

Finally the control system has been tested using simple speed ramps, but needs to be tested under emulated wind turbine response conditions. At present the inverter output current demand is set to be constant, but if wind turbine emulation is used then it will need to be set to track the turbine power curve, and this system could interact with the other control systems.

Bibliography

[1] H. Hansen, L, L. Helle, E. Blaabjerg, S. Ritchie, H. Munk-Nielsen, P. Bindner, P. Sorenson, and B. Bak-Jensen, "Conceptural survey of generators and power electronics for wind turbines," Risø National Laboratory, Roskilde, Denmark, Tech. Rep., 2001.

[2] (2003, Jul.) Wind energy pictures – gedser wind turbine. Danish Wind Energy Association. [Online]. Available: http://www.windpower.org/en/pictures/juul.htm

[3] S. Muller, M. Deicke, and R. W. De Doncker, "Doubly fed induction generator systems for wind turbines," *IEEE Ind. Appl. Mag.*, pp. 26–33, May 2002.

[4] (2009) 3d drawing of the N80/ 2500kW. Nordex AG. [Online]. Available: http://www.nordex-online.com/en/news-press/press-pictures.html

[5] P. J. Tavner, G. J. W. van Bussel, and F. Spinato, "Machine and converter reliabilities in wind turbines," in *IEE 2nd International Conference on Power Electronics, Machines and Drives (PEMD), Dublin*, 2006.

[6] (2009) E-70 wind turbine. Enercon GmbH. [Online]. Available: http://www.enercon.de/en/_home.htm

[7] Z72 wind turbine. Zephyros bv. [Online]. Available: http://www.peeraer.com/zephyros/products/

[8] C. Versteegh, "Design of the Zephyros Z72 wind turbine with emphasis on the direct drive PM generator," in *Nordic Workshop on Power and Industrial Electronics (NORPIE), Trondheim*, 2004.

[9] H. Polinder, F. F. A. van der Pijl, G.-J. de Vilder, and P. J. Tavner, "Comparison of direct-drive and geared generator concepts for wind turbines," *IEEE Trans. Energy Convers.*, vol. 21, no. 3, pp. 725–733, 2006.

[10] J. K. Steinke and O. Apeldoorn, "Applying the experience of industrial high power converter design to windpower conversion," ABB Schweiz AG, Tech. Rep., 2002.

[11] E. Spooner, P. Gordon, J. R. Bumby, and C. D. French, "Lightweight ironless-stator PM generators for direct-drive wind turbines," *IEE Proc. Electr. Power Appl.*, vol. 152, no. 1, pp. 17–26, 2005.

[12] E. Levi, R. Bojoi, F. Profumo, H. Toliyat, and S. Williamson, "Multiphase induction motor drives - a technology status review," *IET Electr. Power. Appl.*, vol. 1, no. 4, pp. 489–516, 2007.

[13] (2009) Converteam - naval electric power and propulsion packages. SPG Media Limited. [Online]. Available: http://www.naval-technology.com/contractors/propulsion/alstom/alstom1.html

[14] B. Mecrow, A. Jack, D. Atkinson, S. Green, G. Atkinson, A. King, and B. Green, "Design and testing of a four-phase fault-tolerant permanent magnet machine for an engine fuel pump," *IEEE Trans. Ind. Appl.*, vol. 19, no. 4, pp. 671–678, 2004.

[15] J. R. Bumby and R. Martin, "Axial-flux permanent-magnet air-cored generator for small-scale wind turbines," *IEE Proc. Electr. Power Appl.*, vol. 152, p. 5, 2005.

[16] H. Polinder, G. J. W. van Bussel, and M. Dubois, "Design of a PM generator for the Turby, a wind turbine for the built environment," in *International Conference ICEM, Kracow, Poland*, Sep. 2004, pp. 432–438.

[17] H. Bonnet, "A comparison between insulation systems available for PWM-inverter-fed motors," *IEEE Trans. Ind. Appl.*, vol. 33, no. 5, pp. 1331–1341, 1997.

[18] T. Burton, D. Sharpe, N. Jenkins, and E. Bossanyi, *Wind Energy Handbook*. WileyBlackwell, 2001, ch. 1, pp. 14–16.

[19] Q. Wang and L. Chang, "An intelligent maximum power extraction algorithm for inverter-based variable speed wind turbine systems," *IEEE Trans. Power Electron.*, vol. 19, no. 5, pp. 1242–1249, 2004.

[20] E. Hau, *Wind Turbines, Fundamentals, Technologies, Applications, Economics.* Springer, 2006, ch. 5, pp. 91–99.

[21] W. E. Leithead and B. Connor, "Control of variable speed wind turbines: Dynamic models," *Int.J. Control*, vol. 73, no. 13, pp. 1173–1188, 2000.

[22] W. E. Leithead and B. Connor, "Control of variable speed wind turbines: Design task," *Int.J. Control*, vol. 73, no. 13, pp. 1189–1212, 2000.

[23] H. Camblong, G. Tapia, and M. Rodriguez, "Robust digital control of a wind turbine for rated-speed and variable-power operation regime," *IEE Proc. Control Theory Appl.*, vol. 153, no. 3, pp. 81–91, 2006.

[24] J. B. Ekanayake, L. Holdsworth, X. Wu, and N. Jenkins, "Dynamic modeling of doubly fed induction generator wind turbines," *IEEE Trans. Power Syst.*, vol. 18, no. 2, pp. 803–809, 2003.

[25] (2007) V80-2.0 MW brochure. Vestas Wind Systems A/S. [Online]. Available: http://www.vestas.com/en/wind-power-solutions/wind-turbines/2.0-mw.aspx

[26] B. M. Weedy and B. J. Cory, *Electric Power Systems.* John Wiley & Sons, Chichester, UK, 1998.

[27] J. S. Lai and F. Z. Peng, "Multilevel converters - a new breed of power converters," *IEEE Trans. Ind. Appl.*, vol. 23, no. 3, pp. 509–517, 1996.

[28] J. L. Dallachy and I. Tait, *Guidance note for the connection of wind farms*, SP Transmission and Distribution, Scottish Hydroelectric Std. 2.2.2, 2002.

[29] Z. Chen and E. Spooner, "Grid interface options for variable-speed permanent-magnet generators," *IEE Proc. Electr. Power Appl.*, vol. 145, no. 4, pp. 273–283, 1998.

[30] N. Mohan, T. M. Undeland, and W. P. Robbins, *Power Electronics: Converters, Applications and Design.* John Wiley & Sons, 2003, ch. 7, pp. 195–196.

[31] J. Rodriguez, J. S. lai, and F. Z. Peng, "Multilevel inverters: A survey of topologies, controls and applications," *IEEE Trans. Ind. Electron.*, vol. 49, no. 4, pp. 724–738, Aug. 2002.

[32] R. Zehringer, A. Stuck, and T. Lang, "Material requirements for high voltage, high power IGBT devices," *Solid State Electron.*, vol. 42, no. 12, pp. 2139–2151, 1998.

[33] N. Mohan, T. M. Undeland, and W. P. Robbins, *Power Electronics: Converters, Applications and Design.* John Wiley & Sons, 2003, ch. 7, pp. 172–178.

[34] *Aluminium Electrolytic Capacitors, Application note TD003*, BHC Components Ltd., Granby Industrial Estate, Weymouth, Dorset DT4 9TE, United Kingdom.

[35] C. H. Ng, M. A. Parker, L. Ran, J. R. Bumby, and E. Spooner, "Analysis of the DC-link capacitance requirement in high level MCVSI," in *Proceedings of the 41st International Universities Power Engineering Conference (UPEC)*, vol. 1, Newcastle upon Tyne, Sep. 2006, pp. 103–107.

[36] G. C. Stone, E. A. Boulter, I. Culbert, and H. Dhirani, *Electrial Insulation for Rotating Machines.* IEEE Press, 2004.

[37] R. W. Sillars, *Electrical Insulating Materials and their Application.* IEE Publishing, 1973, pp. 172–179.

[38] *Semikron Application Manual*, Semikron International GmbH.

[39] L. Alston, *High Voltage Technology.* Oxford University Press, 1968, pp. 49–54.

[40] Y. Yasuda, N. Uno, H. Kobayashi, and T. Funabashi, "Surge analysis on wind farm when winter lightning strikes," *IEEE Trans. Energy Convers.*, vol. 23, no. 1, pp. 257–262, Mar. 2008.

[41] B. Glushakow, "Effective lightning protection for wind turbine generators," *IEEE Trans. Energy Convers.*, vol. 22, no. 1, pp. 214–222, Mar. 2007.

[42] E. Hau, *Wind Turbines: Fundamentals, Technologies, Applications, Economics.* Springer, 2006, ch. 7, p. 250.

[43] C. Hochgraf and R. H. Lasseter, "Statcom controls for operation with unbalanced voltages," *IEEE Trans. Power Del.*, vol. 13, no. 2, pp. 538–544, Apr. 1998.

[44] D. Van de Sype, K. DeGusseme, A. Van de Bossche, and A. Melkebeek, "Duty-ratio feedforward for digitally controlled boost PFC converters," *IEEE Trans. Ind. Electron.*, vol. 52, no. 1, pp. 108–115, 2005.

[45] F. M. Gardner, *Phaselock Techniques*. John Wiley and Sons, 1966, ch. 1, p. 1.

[46] I. Agirman and V. Blasko, "A novel control method of a VSC without AC line voltage sensors," *IEEE Trans. Ind. Appl.*, vol. 39, no. 2, pp. 519–524, Mar. 2003.

[47] C. H. Ng, M. A. Parker, L. Ran, P. J. Tavner, J. R. Bumby, and E. Spooner, "A multilevel modular converter for a large, light weight wind turbine generator," *IEEE Trans. Power Electron.*, vol. 23, no. 3, pp. 1062–1074, May 2008.

[48] N. Mohan, T. M. Undeland, and W. P. Robbins, *Power Electronics: Converters, Applications and Design*. John Wiley & Sons, 2003, ch. 18, pp. 500–502.

[49] T. Williams, *EMC for Product Designers*. Newnes, 1998, ch. 5, pp. 143–164.

[50] T. McDonald and J. Ambrus, "Evaluation of power MOSFET thermal solutions for desktop and mobile processor power," in *PCIM China*. International Rectifier Corporation, Mar. 2002.

[51] P. C. Loh, D. G. Holmes, and T. A. Lipo, "Implementation and control of distributed PWM cascaded multilevel inverters with minimal harmonic distortion and common-mode voltage," *IEEE Trans. Power Electron.*, vol. 20, no. 1, pp. 90–99, Jan. 2005.

[52] D. J. Perreault and J. G. Kassakian, "Distributed interleaving of paralleled power converters," *IEEE Trans. Circuits Syst. I*, vol. 44, no. 8, pp. 728–734, Aug. 1997.

[53] *MODBUS over Serial Line Specification and Implementation Guide V1.02*, Modbus-IDA Std.

[54] *MODBUS Application Protocol Specification V1.1b*, Modbus-IDA Std.

[55] *CAN Specification, Version 2.0*, Robert Bosch GmbH Std., 1991.

[56] *TMS320 DSP/BIOS User's Guide*, Texas Instruments, Apr. 2004.

[57] F. M. Gardner, *Phaselock Techniques*. John Wiley and Sons, 1966, ch. 2, pp. 40–54.

[58] N. Mohan, T. M. Undeland, and W. P. Robbins, *Power Electronics: Converters, Applications and Design*. John Wiley & Sons, 2003, ch. 8, pp. 211–221.

[59] A. S. Tannenbaum and M. van Steen, *Distributed Systems: Principles and Paradigms*. Prentice Hall, 2002, ch. 5, pp. 241–258.

[60] L. Rodruigues, M. Guimaraes, and J. Rufino, "Fault-tolerant clock synchronization in CAN," in *RTSS'98, Madrid, Spain*, Dec. 1998.

Appendix A

Published Work

1. M. A. Parker, P. Tavner, L. Ran, A. Wilson, "A low cost power-tracking controller for a small vertical axis wind turbine" in *Proceedings of the 40th International Universities Power Engineering Conference (UPEC)*, Cork, Sep. 2005.

2. M. A. Parker, C. H. Ng, L. Ran, P. Tavner, E. Spooner, "Power control of a direct drive wind turbine with simplified conversion stage & transformerless grid interface" in *Proceedings of the 41st International Universities Power Engineering Conference (UPEC)*, vol. 1, Newcastle upon Tyne, Sep. 2006, pp. 65–68.

3. C. H. Ng, M. A. Parker, L. Ran, J. R. Bumby, and E. Spooner, "Analysis of the DC-link capacitance requirement in high level MCVSI," in *Proceedings of the 41st International Universities Power Engineering Conference (UPEC)*, vol. 1, Newcastle upon Tyne, Sep. 2006, pp. 103–107.

4. C. H. Ng, M. A. Parker, L. Ran, P. J. Tavner, J. R. Bumby, and E. Spooner, "A multilevel modular converter for a large, light weight wind turbine generator," *IEEE Trans. Power Electron.*, vol. 23, no. 3, pp. 1062–1074, May 2008.

Appendix B

Prototype Module Schematics

B.1 Electrical Board

The electrical board includes all the power electronics associated with the inverter and rectifier. It also includes the gate drivers for the switching MOSFETs, as well as the hall-effect sensors to measure the input and output current, and the potential divider to measure the DC-link voltage. An isolated DC-DC converter is used to isolate the 12V DC supply, which is supplied to all the modules.

B.2 Control Board

The control board includes the microcontroller, isolated communications and op-amp buffers for the current and voltage measurements. The 12V power supply is stepped down to 3.3V using a switchmode circuit, for the microcontroller IO power supply. The 1.8V microcontroller core supply is derrived from the 1.8V supply using a linear regulator, as is the 1.8V analogue core supply. The 3.3V analogue supply is derrived from the 12V supply using a linear regulator.

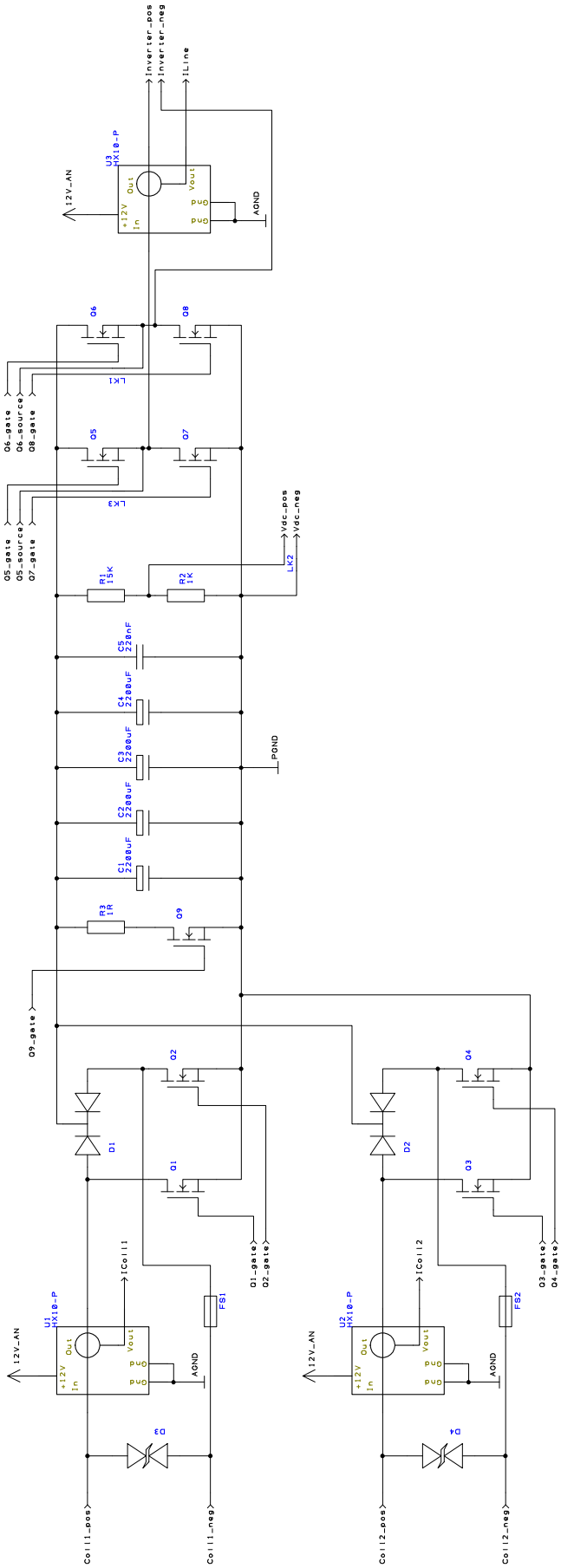


Figure B.1: Power processing part of the electrical board

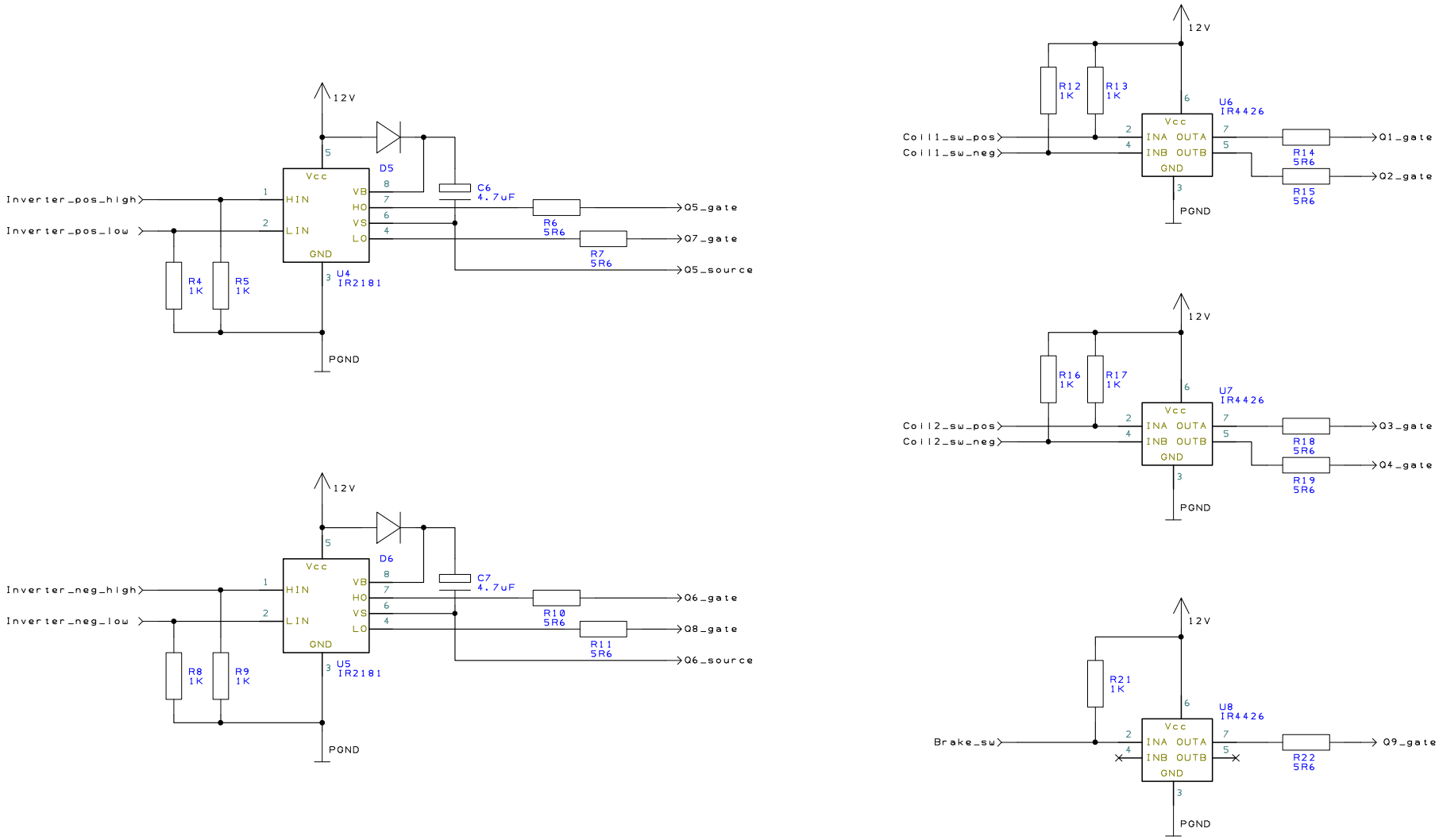


Figure B.2: Electrical board MOSFET gate drivers

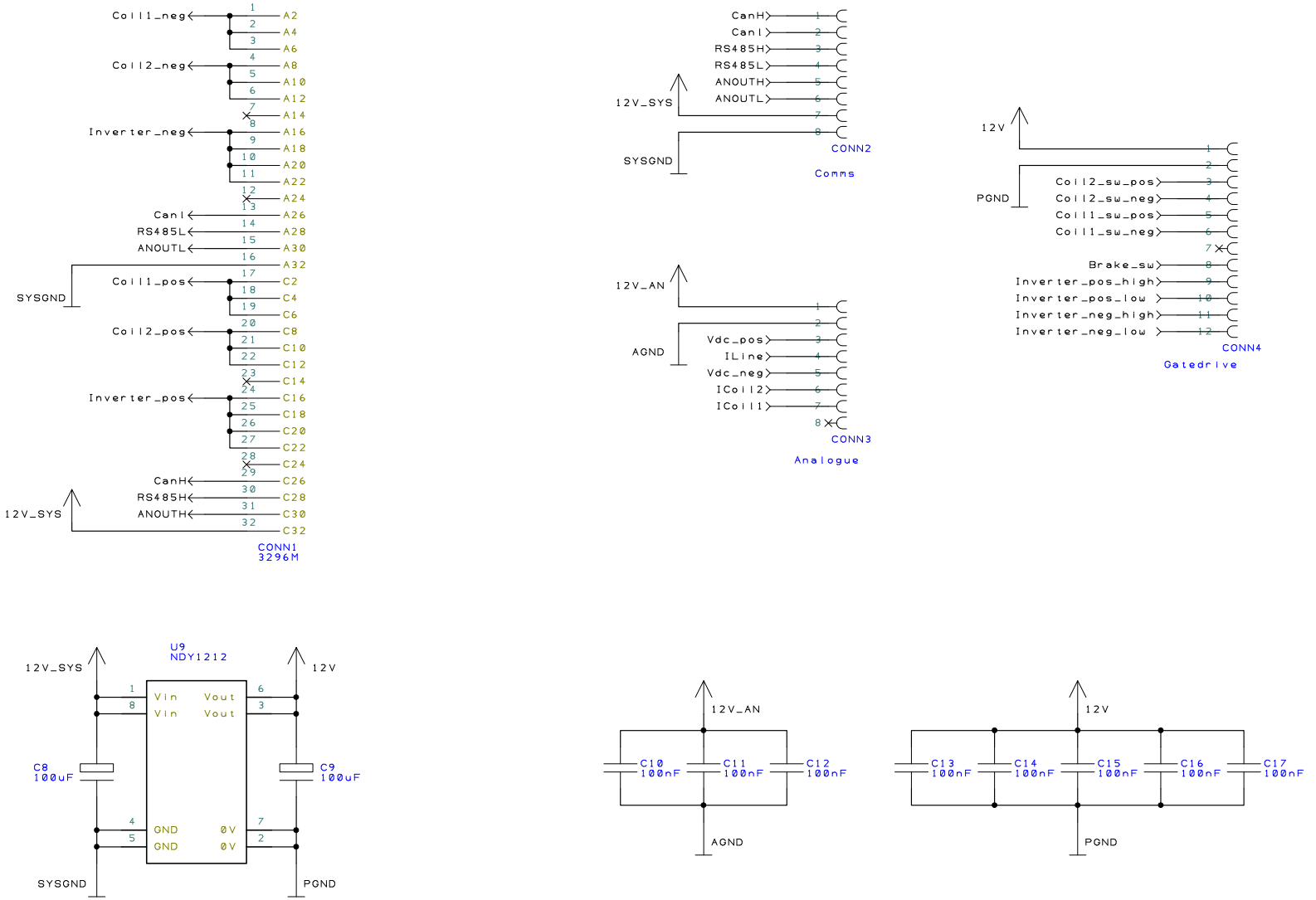


Figure B.3: Electrical board inputs and outputs

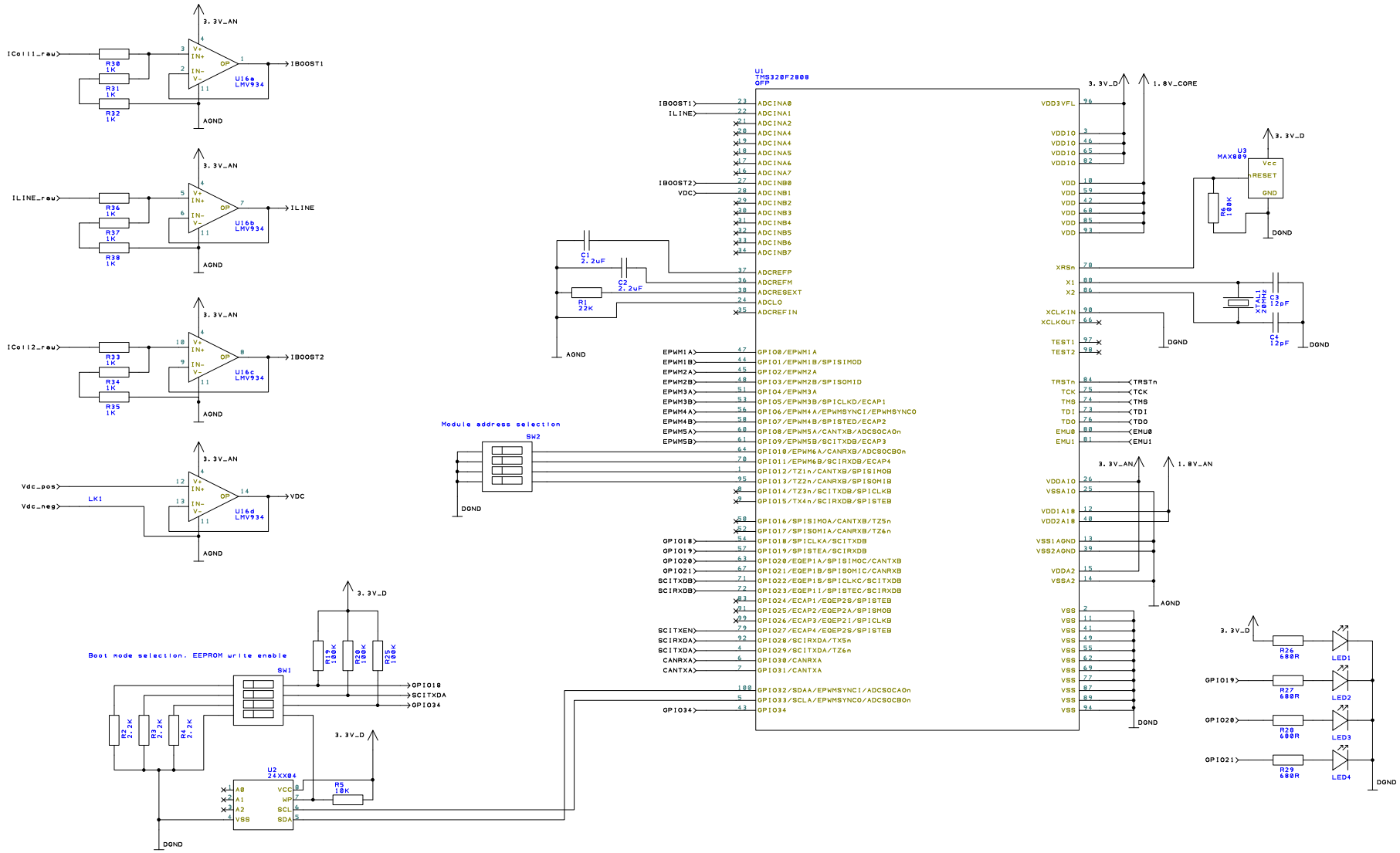


Figure B.4: Main components of the controller board

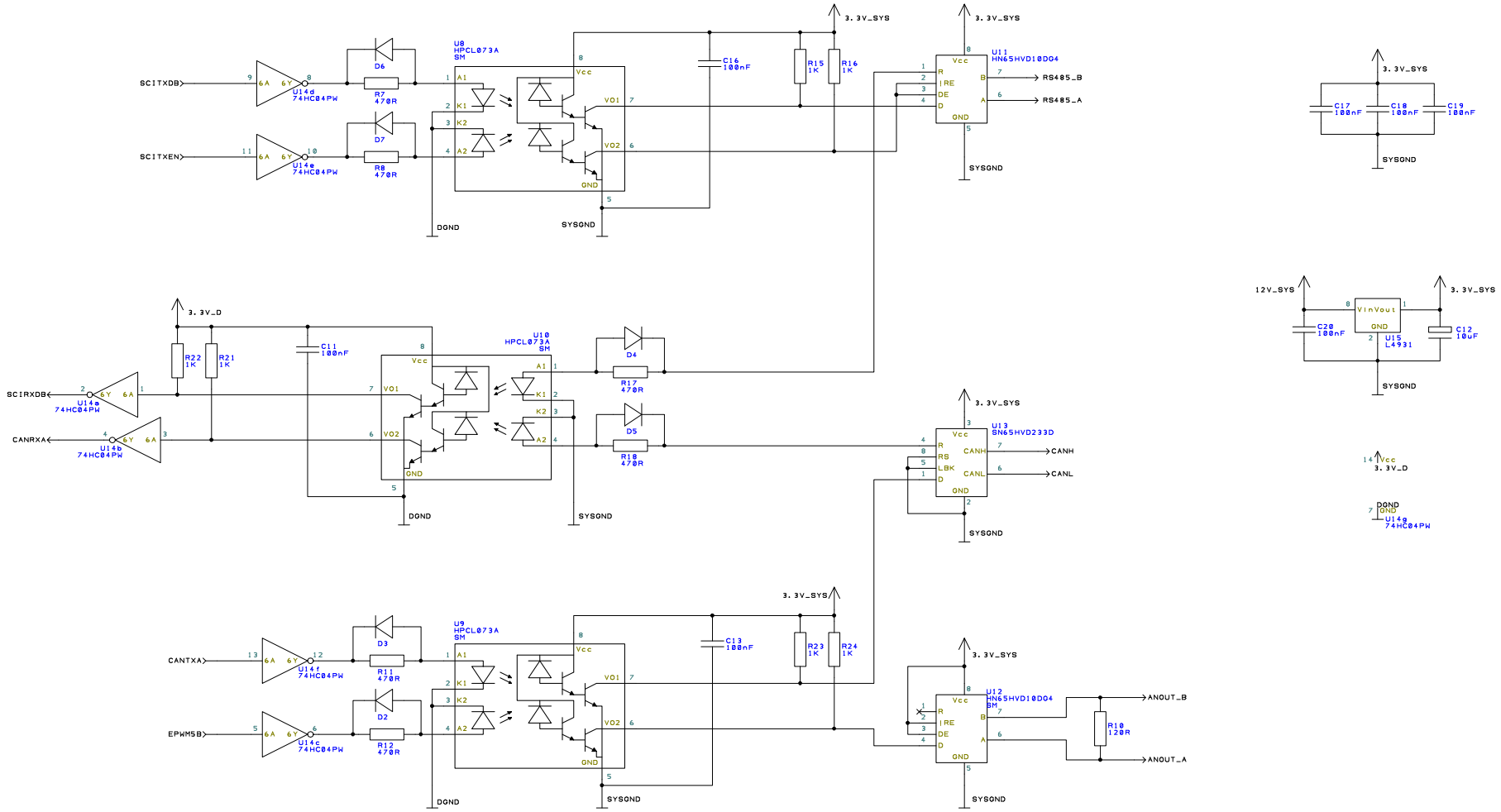


Figure B.5: Isolated communications section of the controller board

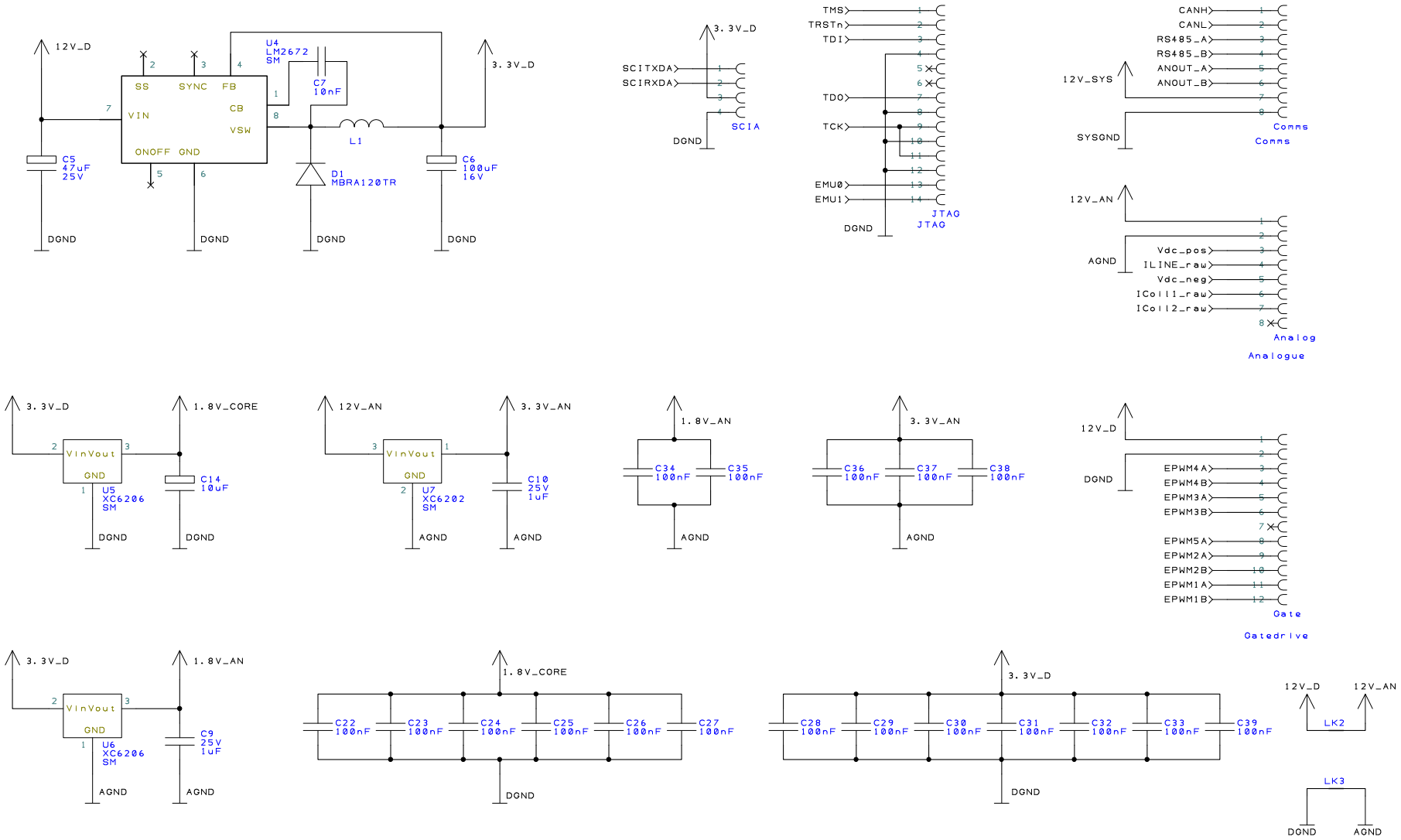


Figure B.6: Power supply and decoupling capacitros for the controller board

Appendix C

Microcontroller Code

Microcontroller code for the power modules is given here for the de-centralised control scheme described in chaper 9. Only the main functions, relating to the control of the power system, are given here – communications and peripheral functions are omitted, as is the initialisation code.

There are three main interrupt service routines (ISRs), a hardware ISR which operates at 16kHz, and has a high priority, and two software interrupts (SWIs), which operate at 8kHz and 1kHz and handle functions with less severe timing constraints. There is also a hardware ISR which controls the switching instances of the inverter when operating in the fundamental switching mode.

C.1 Rectifier Hardware Interrupt Service Routine

```
//Boost rectifier interrupt service routine. ADC sampling is triggered at 32kHz by PWM modules
     EPwm3 and EPwm4, which drive the rectifier. ADC triggers this ISR when sampling complete,
     but only every other time, i.e. at 16kHz.
#pragma CODE_SECTION(AdcIntSeq1, "RamFuncs")
void AdcIntSeq1(void)
{
    //temporary variables, last the length of the ISR
    int16 dutyhalf,pwminterval,msgtemp,igrid,addr,period;
    int32 duty1,duty2,tdiff,invduty,invduty2,timebase;

    //static variables, maintain value to next operation of ISR
    static int16 count,SyncCount,PhaseCount,SyncWait,occount,igridold,old_period,vdcold;
    static Uint32 I1zero,I2zero,Ioutzero,LastSyncIn;
    static int32 LastGridAngle;

    //initialise static variables the first time this routine is run
    if(intseq1init==1)
    {
        intseq1init=0;
        I1zero=0;
        I2zero=0;
        Ioutzero=0;
        count=0;
        SyncCount=0;
        PhaseCount=0;
        last_dir=EPwm1Regs.TBSTS.bit.CTRDIR;
        SyncWait=0;
        occount=0;
        igridold=0;
        vdcold=0;
```

```
    old_period=520;
}

//Detect rectifier operation mode
if(RectRegs.RECTSTAT.bit.Status==RECT_PREP || RectRegs.RECTSTAT.bit.Status==RECT_READY){
    if(RectRegs.RECTSTAT.bit.Active==0 || RectRegs.RECTSTAT.bit.Status==RECT_PREP){
        //Seeking or tracking
        //record coil currents from ADC
        RectRegs.IBoost1=(AdcRegs.ADCRESULT1-RectRegs.IBoost1Zero)+(AdcRegs.ADCRESULT9-
            RectRegs.IBoost1Zero);
        RectRegs.IBoost2=(AdcRegs.ADCRESULT0-RectRegs.IBoost2Zero)+(AdcRegs.ADCRESULT8-
            RectRegs.IBoost2Zero);

        //set boost rectifiers to pulses of width SEEK_PRD
        EPwm3Regs.CMPA.half.CMPA=SEEK_PRD;
        EPwm3Regs.CMPB=SEEK_PRD;
        EPwm4Regs.CMPA.half.CMPA=SEEK_PRD;
        EPwm4Regs.CMPB=SEEK_PRD;
    }else{
        //Active
        //record coil currents from ADC - average of the two readings taken
        RectRegs.IBoost1=(((long)AdcRegs.ADCRESULT1+(long)AdcRegs.ADCRESULT9)>>1)-RectRegs.
            IBoost1Zero;
        RectRegs.IBoost2=(((long)AdcRegs.ADCRESULT0+(long)AdcRegs.ADCRESULT8)>>1)-RectRegs.
            IBoost2Zero;

        //current proportional controller
        RectRegs.IError1=abs(RectRegs.IStar1)-abs(RectRegs.IBoost1);
        RectRegs.IError2=abs(RectRegs.IStar2)-abs(RectRegs.IBoost2);
        duty1=(long)RectRegs.IError1*(long)RectRegs.ICoilKp+(long)RectRegs.DutyFF1;
        duty2=(long)RectRegs.IError2*(long)RectRegs.ICoilKp+(long)RectRegs.DutyFF2;

        //duty cycle limts
        if(duty1<0) duty1=0;
        if(duty1>32767) duty1=32767;
        if(duty2<0) duty2=0;
        if(duty2>32767) duty2=32767;

        RectRegs.DutyFbk1=duty1;
        RectRegs.DutyFbk2=duty2;

        //calculate and rectifier duty cycle register values, and set
        duty1=(duty1*(long)EPwm3Regs.TBPRD)>>15;
        duty2=(duty2*(long)EPwm3Regs.TBPRD)>>15;
        EPwm3Regs.CMPA.half.CMPA=duty1;
        EPwm3Regs.CMPB=duty1;
        EPwm4Regs.CMPA.half.CMPA=duty2;
        EPwm4Regs.CMPB=duty2;
    }
}else if(RectRegs.RECTSTAT.bit.Status==RECT_CAL){
    //Calibrating, to detect zero current values of the current transducers
    //add results to accumulators, and increment counter
    //if 4096 results, reset counter and put accumulator/4096 into zero registers, signal
        end of calibration

    //switch off rectifier
    EPwm3Regs.CMPA.half.CMPA=0;
    EPwm3Regs.CMPB=0;
    EPwm4Regs.CMPA.half.CMPA=0;
    EPwm4Regs.CMPB=0;

    if(RectRegs.RECTSTAT.bit.Cal==0){    //check if calibration has finished, system will
        remain in calibration mode until set otherwise in the 1kHz ISR
        I1zero+=AdcRegs.ADCRESULT1;
        I2zero+=AdcRegs.ADCRESULT0;
        Ioutzero+=AdcRegs.ADCRESULT2;    //add ADC measurements to zero accumulators
        count++;
        if(count==4096)                  //if there are 4096 readings...
        {
            RectRegs.IBoost1Zero=I1zero>>12;
            RectRegs.IBoost2Zero=I2zero>>12;
            InvRegs.ILineZero=Ioutzero>>12;      //divide results by 4096
            I1zero=0;
            I2zero=0;
            Ioutzero=0;
            count=0;
            RectRegs.RECTSTAT.bit.Cal=1;         //reset accumulator registers to zero,
                signal end of calibration
        }
    }else{
        RectRegs.IBoost1=(AdcRegs.ADCRESULT1-RectRegs.IBoost1Zero);
        RectRegs.IBoost2=(AdcRegs.ADCRESULT0-RectRegs.IBoost2Zero);
    }
}else{
    //Idle or fault
    //record coil currents from ADC
    RectRegs.IBoost1=(AdcRegs.ADCRESULT1-RectRegs.IBoost1Zero);
    RectRegs.IBoost2=(AdcRegs.ADCRESULT0-RectRegs.IBoost2Zero);

    //switch off rectifier
    EPwm3Regs.CMPA.half.CMPA=0;
    EPwm3Regs.CMPB=0;
    EPwm4Regs.CMPA.half.CMPA=0;
    EPwm4Regs.CMPB=0;
}
```

```
//Record inverter current from ADC
igrid=InvRegs.ILineZero-AdcRegs.ADCRESULT2;

//changing of inverter modes
if(InvRegs.INVSET.bit.mode != INV_FUND){     //changing to a mode other than fundamental
     switching
     InvRegs.INVCTRL.bit.mode=InvRegs.INVSET.bit.mode;
     EPwm6Regs.ETSEL.bit.INTEN=0;          //disable EPwm6 interrupts
     EPwm1Regs.AQCSFRC.bit.CSFA=0;
     EPwm1Regs.AQCSFRC.bit.CSFB=0;
     EPwm2Regs.AQCSFRC.bit.CSFA=0;
     EPwm2Regs.AQCSFRC.bit.CSFB=0;         //disable software forcing
}else{
     //changing to fundamental switching, which occurs on the positive zero-crossing of the
          output voltage
     if(InvRegs.GridAngle>=0 && LastGridAngle<0 && InvRegs.INVCTRL.bit.mode!=INV_FUND){
          InvRegs.INVCTRL.bit.mode=INV_FUND;
          EPwm6Regs.ETCLR.bit.INT=1;       //Clear EPwm6 interrupt bit
          EPwm6Regs.ETSEL.bit.INTEN=1;     //enable EPwm6 interrupts
     }
}

//Start simulating a module fault, if asked to do so by a command from the host PC. Fault
     occurs at peak of output voltage.
if(InvRegs.INVSET.bit.fault==1 && InvRegs.INVCTRL.bit.fault!=1){
     if(InvRegs.GridAngle>=1073741824 && LastGridAngle< 1073741824){
          InvRegs.INVCTRL.bit.fault=1;
     }
}

//Stop simulating a moudle fault, happens immediately
if(InvRegs.INVSET.bit.fault==0) InvRegs.INVCTRL.bit.fault=0;

//sending of synchronisation and current limiting messages
if(InvRegs.INVCTRL.bit.fault==0){
     //receive message on mailbox 3, which receives status message frames with identifier 11
     if(ECanaRegs.CANRMP.bit.RMP3==1){
          if(ECanaMboxes.MBOX3.MSGCTRL.bit.DLC==1){        //check message length > 1 byte
               msgtemp=ECanaMboxes.MBOX3.MDL.byte.BYTE0;
               if(msgtemp==1){
                    //message=1, turn on current limiting
                    InvRegs.INVCTRL.bit.mode=INV_ILIMIT;
                    InvRegs.INVSET.bit.mode=INV_ILIMIT;
               }
          }
          ECanaRegs.CANRMP.all |= 0x0000008;               //clear message received bit
     }

     //Inverter current limit detect
     if(InvRegs.INVCTRL.bit.mode!=INV_ILIMIT){
          //activate current limiting if current is over ILimit1 on one sample, or ILimit2 on
               two consecutive samples
          if(abs(igrid)>InvRegs.ILimit1){
               occount+=2;
          }else if(abs(igrid)>InvRegs.ILimit2){
               occount+=1;
          }else{
               occount=0;
          }
          if(occount>1){
               occount=0;          //turn on current limiting and send message to other
               CANStatSend(1);     //modules to turn on current limiting
               InvRegs.INVCTRL.bit.mode=INV_ILIMIT;
               InvRegs.INVSET.bit.mode=INV_ILIMIT;
          }
     }

     //Synchronise inverter PWM with rectifier, send CAN sync message, identifier 10
     //The inverter PWM outputs, on PWM modules EPwm1 and EPwm2 run at 1/24th of the
          rectifier rate, so every 24 operations of this ISR the inverter PWM modules are
          synchronised
     PhaseCount++;
     if(PhaseCount >= 24){
          PhaseCount=0;
          EPwm1Regs.TBCTL.bit.SWFSYNC=1;  //synchronise inverter - sets timebase counter to
               zero. EPwm2 automatically synchronises from EPwm1.
          SyncCount++;
          if(SyncCount==7){    //Send sync message at 1/7 of inverter PWM frequency
               SyncCount=0;
               CANSyncSend();
               SyncWait=1;     //waiting for the next sync message from another module
          }
     }
}

//Receive CAN Grid Synchronisation message, identifier 10
if(ECanaRegs.CANRMP.bit.RMP1==1){
     //synchronisation of grid angle and voltage references
     tdiff=(((ECanaRegs.CANTSC-ECanaMOTSRegs.MOTS1+InvRegs.CanPropDly)*InvRegs.GridStep)>>16)
          *1067;  //calculate how much grid angle reference has advanced since message was
          sent
     InvRegs.PhaseError=(int)ECanaMboxes.MBOX1.MDL.word.HI_WORD-((InvRegs.GridAngle-tdiff)
          >>16);      //calculate error between this module's angle reference and that of the
          module sending the message
     InvRegs.VError=(int)ECanaMboxes.MBOX1.MDL.word.LOW_WORD-InvRegs.GridV;
                    //calculate error between this moduel's voltage reference and that of the
```

```
            module sendign the message

        //interleaving of grid PWM carriers
        //if the module has just sent it's own synchronisation message, then it waits for the
            synchronisation message of the next module
        if(SyncWait==1){
            //calculate where this module's inverter PWM timebase is relative to the modules
                before and after: should be exactly in between
            pwminterval=(ECanaMOTSRegs.MOTS1-LastSyncIn) & 0x0000FFFF;
            InvRegs.PWMError=(pwminterval>>1)-((ECanaMOTSRegs.MOTS0-LastSyncIn) & 0x0000FFFF);
            //modify PWM time period to distribute switching evenly between modules
            pwminterval=InvRegs.PWMError>>2;
            if(pwminterval>InvRegs.PWMErrorLimit) pwminterval=InvRegs.PWMErrorLimit;
            if(pwminterval<-InvRegs.PWMErrorLimit) pwminterval=-InvRegs.PWMErrorLimit;
            period=6240+pwminterval;
            EPwm1Regs.TBPRD=period;
            EPwm2Regs.TBPRD=period;
            period=((long)period*5461)>>16;       //divide by 12 to obtain rectifier PWM period
            EPwm3Regs.TBPRD=period;
            EPwm4Regs.TBPRD=period;
            EPwm4Regs.TBPHS.half.TBPHS=period;
            SyncWait=0;
        }
        LastSyncIn=ECanaMOTSRegs.MOTS1;
        ECanaRegs.CANRMP.all |= 0x0000002;
    }

    //setting inverter of duty cycle
    if(InvRegs.INVCTRL.bit.fault==0){
        //PWM-based modes
        if(InvRegs.INVCTRL.bit.mode==INV_PWM || InvRegs.INVCTRL.bit.mode==INV_ILIMIT){
            //set inverter duty
            dutyhalf=EPwm1Regs.TBPRD>>1;
            if(InvRegs.INVCTRL.bit.mode==INV_ILIMIT){
                //Current limiting mode: add output of current proportional controller to
                    feedforward duty cycle
                invduty2=(long)InvRegs.DutyFFd+((long)InvRegs.Istar-(long)igrid)*(long)InvRegs.
                    IGridKp;
            }else{
                //Normal mode: use only feedforward duty cycle
                invduty2=(long)InvRegs.DutyFFd;
            }
            invduty=(invduty2*(long)EPwm1Regs.TBPRD)>>16;
            if(invduty>dutyhalf) invduty=dutyhalf;
            if(invduty<-dutyhalf) invduty=-dutyhalf;
            EPwm1Regs.CMPA.half.CMPA=dutyhalf+invduty;
            EPwm2Regs.CMPA.half.CMPA=dutyhalf-invduty;
            if(invduty2>32767){
                InvRegs.DutyFbk=32767;
            }else if(invduty2<-32767){
                InvRegs.DutyFbk=-32767;
            }else{
                InvRegs.DutyFbk=invduty2;
            }
            PwmInvForce();  //re-calculate inverter switching state based on new duty and time
                periods
        }else{
            //Fundamental switching mode - synchronise fundamental on zero crossing
            if(InvRegs.GridAngle>=0 && LastGridAngle<0){     //if zero crossing of grid angle ref
                ...
                InvRegs.PhaseFbk=InvRegs.PhaseFFd;
                if(InvRegs.FaultMod==0){
                    //calculate switching times
                    InvRegs.TonPos=((long)STimes[InvRegs.ModAddr-1]*(long)InvRegs.TPrd)>>17;
                    InvRegs.ToffPos=((long)(0xFFFF-STimes[12-InvRegs.ModAddr])*(long)InvRegs.
                        TPrd)>>17;
                }else{
                    //if there is a faulted module somewhere, calculate new switching time based
                        on knowledge of faulted module (module needs to be told which module
                        has a fault by the host PC)
                    if(InvRegs.ModAddr>InvRegs.FaultMod){
                        addr=InvRegs.ModAddr-1;
                    }else{
                        addr=InvRegs.ModAddr;
                    }
                    InvRegs.TonPos=((long)STimesFault[addr-1]*(long)InvRegs.TPrd)>>17;
                    InvRegs.ToffPos=((long)(0xFFFF-STimesFault[11-addr])*(long)InvRegs.TPrd)
                        >>17;
                }
                InvRegs.TonNeg=InvRegs.TPrd-InvRegs.ToffPos;
                InvRegs.ToffNeg=InvRegs.TPrd-InvRegs.TonPos;

                //calculate value timebase counter for EPwm6, which controls the PWM switching
                    times
                timebase=((InvRegs.GridAngle>>16)+32768+InvRegs.PhaseFFd);
                if(timebase>=65536) timebase-=65536;
                if(timebase<0) timebase+=65536;
                timebase=(timebase*(long)InvRegs.TPrd)>>16;

                EPwm6Regs.TBCTL.bit.CTRMODE=3;  //stop EPwm6 timebase counter

                //Re-set inverter state depending on the current timebase value
                if(timebase >= InvRegs.ToffNeg){
                    //off, negative
                    EPwm1Regs.AQCSFRC.bit.CSFA=1;
                    EPwm1Regs.AQCSFRC.bit.CSFB=2;
```

```
                    EPwm2Regs.AQCSFRC.bit.CSFA=1;
                    EPwm2Regs.AQCSFRC.bit.CSFB=2;
                    EPwm6Regs.CMPA.half.CMPA=InvRegs.TonPos;
                    InvRegs.INVCTRL.bit.state=0;
                }else if(timebase >= InvRegs.TonNeg){
                    //on, negative
                    EPwm1Regs.AQCSFRC.bit.CSFA=2;
                    EPwm1Regs.AQCSFRC.bit.CSFB=1;
                    EPwm2Regs.AQCSFRC.bit.CSFA=1;
                    EPwm2Regs.AQCSFRC.bit.CSFB=2;
                    EPwm6Regs.CMPA.half.CMPA=InvRegs.ToffNeg;
                    InvRegs.INVCTRL.bit.state=3;
                }else if(timebase >= InvRegs.ToffPos){
                    //off, positive
                    EPwm1Regs.AQCSFRC.bit.CSFA=1;
                    EPwm1Regs.AQCSFRC.bit.CSFB=2;
                    EPwm2Regs.AQCSFRC.bit.CSFA=1;
                    EPwm2Regs.AQCSFRC.bit.CSFB=2;
                    EPwm6Regs.CMPA.half.CMPA=InvRegs.TonNeg;
                    InvRegs.INVCTRL.bit.state=2;
                }else if(timebase >= InvRegs.TonPos){
                    //on, positive
                    EPwm1Regs.AQCSFRC.bit.CSFA=1;
                    EPwm1Regs.AQCSFRC.bit.CSFB=2;
                    EPwm2Regs.AQCSFRC.bit.CSFA=2;
                    EPwm2Regs.AQCSFRC.bit.CSFB=1;
                    EPwm6Regs.CMPA.half.CMPA=InvRegs.ToffPos;
                    InvRegs.INVCTRL.bit.state=1;
                }else{
                    //off, negative
                    EPwm1Regs.AQCSFRC.bit.CSFA=1;
                    EPwm1Regs.AQCSFRC.bit.CSFB=2;
                    EPwm2Regs.AQCSFRC.bit.CSFA=1;
                    EPwm2Regs.AQCSFRC.bit.CSFB=2;
                    EPwm6Regs.CMPA.half.CMPA=InvRegs.TonPos;
                    InvRegs.INVCTRL.bit.state=0;
                }
                EPwm6Regs.TBCTR=timebase;        //set timebase counter value and period
                EPwm6Regs.TBPRD=InvRegs.TPrd;

                //acknowledge interrupt, if there is one
                EPwm6Regs.ETCLR.bit.INT=1;
                PieCtrlRegs.PIEACK.all=PIEACK_GROUP3;

                EPwm6Regs.TBCTL.bit.CTRMODE=0;  //restart EPwm6 timebase counter

            }
            InvRegs.DutyFbk=InvRegs.DutyFFd;
        }
    }else{
        EPwm1Regs.AQCSFRC.bit.CSFA=1;    //simulating faulted module,
        EPwm1Regs.AQCSFRC.bit.CSFB=2;    //set both inverter outputs to zero
        EPwm2Regs.AQCSFRC.bit.CSFA=1;    //to feed current through
        EPwm2Regs.AQCSFRC.bit.CSFB=2;

        InvRegs.DutyFbk=InvRegs.DutyFFd;
    }

    //Update machine and grid reference angles
    LastGridAngle=InvRegs.GridAngle;
    old_period-=520;
    RectRegs.EAngle+=RectRegs.EStep+((old_period*RectRegs.EStep)>>16)*126;
    InvRegs.GridAngle+=InvRegs.GridStep+((old_period*InvRegs.GridStep)>>16)*126;

    old_period=EPwm3Regs.TBPRD;

    //record grid current
    InvRegs.ILine=(igrid+igridold)>>1;
    igridold=igrid;

    //record dc link voltage
    LinkRegs.Vdc=AdcRegs.ADCRESULT3>>1;

    //Reinitialise for next ADC sequence
    AdcRegs.ADCTRL2.bit.RST_SEQ1 = 1;         // Reset ADC SEQ1
    AdcRegs.ADCTRL2.bit.RST_SEQ2 = 1;         // Reset ADC SEQ2
    AdcRegs.ADCST.bit.INT_SEQ1_CLR = 1;       // Clear INT SEQ1 bit
    PieCtrlRegs.PIEACK.all = PIEACK_GROUP1; // Acknowledge interrupt to PIE

    //decrement the 8kHz and 1kHz SWI triggers, so the run at the correct rate
    SWI_dec(&EREF_swi);      //SWI to compute reference waveforms
    SWI_dec(&PLL_swi);       //SWI for phase-lock loops

    return;
}
```

C.2 8kHz Software Interrupt Service Routine

```
//This software interrupt (SWI) runs at 8kHz and calculates the feedforward voltages and duty
     cycles for the rectifier and inverter, as well as the instantaneous current demands. The
     rectifier applied voltage is calculated from the duty cycle, and transformed to the rotating
      reference frame, and the rectifier current is transformed to the rotating reference frame
     as well. These rectifier values, as well as the inverter voltage and current, are passed
     through 250Hz anti-aliasing filters. The grid voltage is transformed into the rotating
     reference frame in the 1kHz interrupt as the 100Hz notch filter must be applied.
#pragma CODE_SECTION(EMachRef, "RamFuncs")
void EMachRef(void)
{
    //temporary variables
    int16 sine,cosine,vff1,vff2,vffg,GridAngle16,gsine,gcosine,vfb1,vfb2,vfbg;

    //Invert the DC-link voltage
    LinkRegs.VdcInv=qinv1(LinkRegs.Vdc);

    //calculate sine and cos of the estimated electrical angle as these will be used a lot in
         this function
    sine=qsin(RectRegs.EAngle>>16);
    cosine=qcos(RectRegs.EAngle>>16);

    //park transform and filter coil currents
    AAFilt4.input=((long)RectRegs.IBoost1*(long)cosine-(long)RectRegs.IBoost2*(long)sine)>>15;
    AAFilt4.calc(&AAFilt4);
    RectRegs.IBoostD=AAFilt4.output<<1;
    AAFilt5.input=((long)RectRegs.IBoost1*(long)sine+(long)RectRegs.IBoost2*(long)cosine)>>15;
    AAFilt5.calc(&AAFilt5);
    RectRegs.IBoostQ=AAFilt5.output<<1;

    //calculate rectifier applied voltage from the duty cycle, park transform and filter
    vfb1=((RectRegs.IBoost1>>15)*2+1)*(((long)(32767-RectRegs.DutyFbk1)*(long)LinkRegs.Vdc)>>15)
         ;
    vfb2=((RectRegs.IBoost2>>15)*2+1)*(((long)(32767-RectRegs.DutyFbk2)*(long)LinkRegs.Vdc)>>15)
         ;
    AAFilt6.input=((long)vfb1*(long)cosine-(long)vfb2*(long)sine)>>15;
    AAFilt6.calc(&AAFilt6);
    RectRegs.VFbkD=AAFilt6.output<<1;
    AAFilt7.input=((long)vfb1*(long)sine+(long)vfb2*(long)cosine)>>15;
    AAFilt7.calc(&AAFilt7);
    RectRegs.VFbkQ=AAFilt7.output<<1;

    //calculate inverter applied voltage and filter
    vfbg=((long)InvRegs.DutyFbk*(long)LinkRegs.Vdc)>>15;
    AAFilt1.input=vfbg;
    AAFilt1.calc(&AAFilt1);
    InvRegs.VoutFbk=AAFilt1.output<<1;

    //filter DC-link voltage
    AAFilt2.input=LinkRegs.Vdc;
    AAFilt2.calc(&AAFilt2);
    LinkRegs.VdcFilt=AAFilt2.output<<1;

    //filter inverter voltage
    AAFilt3.input=InvRegs.ILine;
    AAFilt3.calc(&AAFilt3);
    InvRegs.ILineFilt=AAFilt3.output<<1;

    //rectifier feedforward voltages
    if(RectRegs.RECTSTAT.bit.Active==1){
        //Inverse Park transform feedforward voltages
        vff1=((long)cosine*(long)RectRegs.VFFD+(long)sine*(long)RectRegs.VFFQ)>>15;
        vff2=(-(long)sine*(long)RectRegs.VFFD+(long)cosine*(long)RectRegs.VFFQ)>>15;

        //convert feedforward voltages to duty cycles
        if(abs(vff1)>LinkRegs.Vdc)
        {
            RectRegs.DutyFF1=0;
        }else{
            RectRegs.DutyFF1=32767-(((long)abs(vff1)*LinkRegs.VdcInv)>>16);
        }
        if(vff2>LinkRegs.Vdc)
        {
            RectRegs.DutyFF2=0;
        }else{
            RectRegs.DutyFF2=32767-(((long)abs(vff2)*LinkRegs.VdcInv)>>16);
        }

        //Calculate instantaneous current demands
        RectRegs.IStar1=((long)sine*(long)RectRegs.Idemand)>>15;
        RectRegs.IStar2=((long)cosine*(long)RectRegs.Idemand)>>15;
    }else{
        //if not active use brake resistor to control current
        EPwm5Regs.CMPA.half.CMPA=(-(long)RectRegs.Idemand*BRAKERESGAIN)>>16;
    }

    GridAngle16=InvRegs.GridAngle>>16;

    gsine=qsin(GridAngle16);
    gcosine=qcos(GridAngle16);

    //grid feedforward voltage
    vffg=((long)gsine*(long)InvRegs.VoutFFq-(long)gcosine*(long)InvRegs.VoutFFd)>>15;
```

```
    //instantaneous grid current demand
    InvRegs.Istar=((long)InvRegs.Idemand_q*(long)gsine-(long)InvRegs.Idemand_d*(long)gcosine)
        >>15;

    //convert feedforward voltages to duty cycles
    if(vffg>LinkRegs.Vdc){
        InvRegs.DutyFFd=32767;
    }else if(vffg<-LinkRegs.Vdc){
        InvRegs.DutyFFd=-32767;
    }else{
        InvRegs.DutyFFd=((long)vffg*LinkRegs.VdcInv)>>16;
    }
}
```

C.3 1kHz Software Interrupt Service Routine

```
//SWI for grid and machine PLL, 1kHz. Also contains the DC-link voltage, and handles the mode
    switching of the inverter and rectifier.
#pragma CODE_SECTION(PLLfunc, "RamFuncs")
void PLLfunc(void)
{
    //permanent variables
    static int16 count,angletemp,GSError11,GSError12,VBuffer[20],VCount;
    static int32 Mintegral,OldGridVolt,OldGridStep,Vintegral;
    //temporary variables
    int32 m_angle,GSError01,GVError01,GridStepTemp,GridVoltTemp;
    int16 vdtemp,vqtemp,idtemp,iqtemp,verror,Idem,Impedence,Vdc;

    //initialise variables the first time this function is run
    if(pllinit == 1){
        Mintegral=0;
        pllinit=0;
        count=0;
        OldGridVolt=(long)VOUTDEM<<16;
        OldGridStep=GRIDSTEP;
        GSError11=0;
        GSError12=0;
        Vintegral=0;
        VCount=0;
    }

    angletemp=(RectRegs.EAngle>>16)-FILTDELAY;  //calculate 16-bit machine angle, add delay to
        compensate for filters

    if(RectRegs.RECTSTAT.bit.Active==1){
        //Estimate machine EMF from coil currents and applied voltages
        Impedence=((long)RectRegs.Speed*(long)RectRegs.CoilL)>>15;
        RectRegs.E_d=RectRegs.VFbkD+(((long)RectRegs.IBoostD*(long)RectRegs.CoilR)>>15)+(((long)
            RectRegs.IBoostQ*(long)Impedence)>>15);
        RectRegs.E_q=RectRegs.VFbkQ+(((long)RectRegs.IBoostQ*(long)RectRegs.CoilR)>>15)-(((long)
            RectRegs.IBoostD*(long)Impedence)>>15);

        //Estimate angle and magnitude - small angle approximation
        m_angle=qdiv(RectRegs.E_d,RectRegs.E_q);
        RectRegs.EAngle_rot=(m_angle*10430)>>16;
        RectRegs.EMagnitude=RectRegs.E_q;
    }else{
        //obtain machine angle from coil currents if rectifier is in seeking mode
        RectRegs.E_d=RectRegs.IBoostD;
        RectRegs.E_q=RectRegs.IBoostQ;

        //estimate angle - full estimation
        m_angle=qdiv(RectRegs.E_d,RectRegs.E_q);
        m_angle=qatan(m_angle);
        if(RectRegs.E_q>0){
            RectRegs.EAngle_rot=m_angle;
        }else{
            if(RectRegs.E_d>0){
                RectRegs.EAngle_rot=-32768+m_angle;
            }else{
                RectRegs.EAngle_rot=32767+m_angle;
            }
        }
    }

    //detect lock status of EMF estimation PLL - detects whether estimated angle error is within
        limits
    if(RectRegs.EAngle_rot > -RectRegs.EAngleLimit && RectRegs.EAngle_rot < RectRegs.EAngleLimit
        && RectRegs.Irms1 > RectRegs.Ithresh){
        RectRegs.RECTSTAT.bit.Lock=1;
    }else{
        RectRegs.RECTSTAT.bit.Lock=0;
    }

    //Machine angle PLL loop filter (PI-controller)
    if(RectRegs.RECTSTAT.bit.Status==RECT_PREP || RectRegs.RECTSTAT.bit.Status==RECT_READY){
        Mintegral+=(long)RectRegs.EAngle_rot*(long)RectRegs.EStepKi;
        if(Mintegral>20000000) Mintegral=20000000;
        if(Mintegral<-20000000) Mintegral=-20000000;
        RectRegs.EStep=Mintegral+(long)RectRegs.EAngle_rot*(long)RectRegs.EStepKp;
    }else{
```

```
    Mintegral=RectRegs.EStep;
    RectRegs.RECTSTAT.bit.Lock=0;
}

RectRegs.Speed=abs((RectRegs.EStep*SPEEDCAL)>>16);  //Calculate speed value from EStep

//Filter measured DC-link voltage with 20-step averaging filter to eliminate 50Hz and higher
    harmonics
VBuffer[VCount]=LinkRegs.VdcFilt;
LinkRegs.VdcAv=(3277*((long)VBuffer[0]+(long)VBuffer[1]+(long)VBuffer[2]+(long)VBuffer[3]+
    (long)VBuffer[4]+(long)VBuffer[5]+(long)VBuffer[6]+(long)VBuffer[7]+
    (long)VBuffer[8]+(long)VBuffer[9]+(long)VBuffer[10]+(long)VBuffer[11]+
    (long)VBuffer[12]+(long)VBuffer[13]+(long)VBuffer[14]+(long)VBuffer[15]+
    (long)VBuffer[16]+(long)VBuffer[17]+(long)VBuffer[18]+(long)VBuffer[19]))>>16;
VCount++;
if(VCount>19) VCount=0;


angletemp=(InvRegs.GridAngle>>16)-FILTDELAY;     //calculate 16-bit grid angle, add delay to
    compensate for filters

//park transform grid feedback voltage, and filter 100Hz with notch filter
vdtemp=-((long)qcos(angletemp)*(long)InvRegs.VoutFbk)>>15;
vqtemp=((long)qsin(angletemp)*(long)InvRegs.VoutFbk)>>15;
NotchFilt1.input=vdtemp;
NotchFilt2.input=vqtemp;
NotchFilt1.calc(&NotchFilt1);
NotchFilt2.calc(&NotchFilt2);
vdtemp=NotchFilt1.output<<2;
vqtemp=NotchFilt2.output<<2;

//park transform grid current, and filter with 100Hz notch filter
idtemp=-((long)qcos(angletemp)*(long)InvRegs.ILineFilt)>>15;
iqtemp=((long)qsin(angletemp)*(long)InvRegs.ILineFilt)>>15;
NotchFilt4.input=idtemp;
NotchFilt5.input=iqtemp;
NotchFilt4.calc(&NotchFilt4);
NotchFilt5.calc(&NotchFilt5);
InvRegs.I_d=NotchFilt4.output<<2;
InvRegs.I_q=NotchFilt5.output<<2;

//estimate grid voltage
if(InvRegs.INVCTRL.bit.mode==INV_ILIMIT){
    //current limiting mode, use grid current and feedback voltage
    InvRegs.V_d=vdtemp+(((long)InvRegs.I_q*(long)InvRegs.Xl)>>15)-(((long)InvRegs.I_d*(long)
        InvRegs.Xr)>>15);
    InvRegs.V_q=vqtemp-(((long)InvRegs.I_d*(long)InvRegs.Xl)>>15)-(((long)InvRegs.I_q*(long)
        InvRegs.Xr)>>15);
}else if(InvRegs.INVCTRL.bit.mode==INV_FUND){
    //fundamental switching mode, use grid current, DC-link voltage and previously applied
        phase feedforward
    InvRegs.V_d=(((long)LinkRegs.VdcFilt*(long)qsin(InvRegs.PhaseFFd))>>15)+(((long)InvRegs.
        I_q*(long)InvRegs.Xl)>>15)-(((long)InvRegs.I_d*(long)InvRegs.Xr)>>15);
    InvRegs.V_q=(((long)LinkRegs.VdcFilt*(long)qcos(InvRegs.PhaseFFd))>>15)-(((long)InvRegs.
        I_d*(long)InvRegs.Xl)>>15)-(((long)InvRegs.I_q*(long)InvRegs.Xr)>>15);
}else{
    //Normal PWM switching mode, use grid current and previously applied feedforward voltage
    InvRegs.V_d=InvRegs.VoutFFd+(((long)InvRegs.I_q*(long)InvRegs.Xl)>>15)-(((long)InvRegs.
        I_d*(long)InvRegs.Xr)>>15);
    InvRegs.V_q=InvRegs.VoutFFq-(((long)InvRegs.I_d*(long)InvRegs.Xl)>>15)-(((long)InvRegs.
        I_q*(long)InvRegs.Xr)>>15);
}

//calculate grid voltage angle and magnitude
InvRegs.GridVoltageEst=qsqrt((long)InvRegs.V_d*(long)InvRegs.V_d+(long)InvRegs.V_q*(long)
    InvRegs.V_q);
angletemp=qatan(qdiv(InvRegs.V_d,InvRegs.V_q));
if(InvRegs.V_q>0){
    InvRegs.GridAngleEst=-angletemp;
}else{
    if(InvRegs.V_d>0){
        InvRegs.GridAngleEst=-32768-angletemp;
    }else{
        InvRegs.GridAngleEst=32767-angletemp;
    }
}

//Grid angle PLL loop filter
GSError01=GRIDSTEP-InvRegs.GridStep;                                    //bias grid
    frequency towards 50Hz so it doesn't wander off if there is no data
if(GSError01>InvRegs.AngleBiasLimit) GSError01=InvRegs.AngleBiasLimit;
if(GSError01<-InvRegs.AngleBiasLimit) GSError01=-InvRegs.AngleBiasLimit;        //limit
    magnitude of bias signal
GSError01+=InvRegs.PhaseError;                                          //error
    relative to other modules
GridStepTemp=OldGridStep+InvRegs.StepB01*(long)GSError01-InvRegs.StepB11*(long)GSError11;
if(InvRegs.INVCTRL.bit.track==1 && InvRegs.INVCTRL.bit.fault==0){       //error from
     grid voltage estimator
    GridStepTemp+=InvRegs.StepB02*(long)InvRegs.GridAngleEst-InvRegs.StepB12*(long)GSError12
        ;
}
if(GridStepTemp>GRIDSTEPMAX) GridStepTemp=GRIDSTEPMAX;
if(GridStepTemp<GRIDSTEPMIN) GridStepTemp=GRIDSTEPMIN;
OldGridStep=GridStepTemp;
InvRegs.GridStep=GridStepTemp;
GSError11=GSError01;
```

```
GSError12=InvRegs.GridAngleEst;
InvRegs.PhaseError=0;

//grid voltage filter
GVError01=InvRegs.GridVBias-InvRegs.GridV;                                    //bias grid
    voltage to 230V
if(GVError01>InvRegs.VoltBiasLimit) GVError01=InvRegs.VoltBiasLimit;
if(GVError01<-InvRegs.VoltBiasLimit) GVError01=-InvRegs.VoltBiasLimit;        //limit bias
    value
GVError01+=InvRegs.VError;                                                    //error relative
     to other modules
GridVoltTemp=OldGridVolt+InvRegs.VoltB01*(long)GVError01;
if(InvRegs.INVCTRL.bit.track==1 && InvRegs.INVCTRL.bit.fault==0){             //error from
    grid voltage estimator
    GridVoltTemp+=InvRegs.VoltB02*(long)(InvRegs.GridVoltageEst-InvRegs.GridV);
}
if(GridVoltTemp>((long)GRIDVMAX<<16)) GridVoltTemp=((long)GRIDVMAX<<16);
InvRegs.GridV=GridVoltTemp>>16;
OldGridVolt=GridVoltTemp;
InvRegs.VError=0;

//calculate inverter feedforward voltage, in rotating reference frame
InvRegs.VoutFFq=InvRegs.GridV+(((long)InvRegs.Idemand_q*(long)InvRegs.Xr+(long)InvRegs.
    Idemand_d*(long)InvRegs.Xl)>>15);
InvRegs.VoutFFd=-(((long)InvRegs.Idemand_q*(long)InvRegs.Xl+(long)InvRegs.Idemand_d*(long)
    InvRegs.Xr)>>15);

//set DC-link voltage demand - if in fundamental switching mode this is equal to the
    estimated grid voltage magnitude
if(InvRegs.INVCTRL.bit.mode==INV_FUND){
    LinkRegs.VdcDem=InvRegs.VoutFFq;
}else{
    LinkRegs.VdcDem=LinkRegs.VdcDemDem;
}

//calculate the inverter voltage phase angle, from the feedforward voltage - used to set the
     angle in fundamental switching
InvRegs.PhaseFFd=qatan(qdiv(InvRegs.VoutFFd,InvRegs.VoutFFq));

//Vdc Controller
if(RectRegs.RECTSTAT.bit.Charge==1){
    verror=LinkRegs.VdcDem-LinkRegs.VdcAv;
    Vintegral+=(long)verror*(long)LinkRegs.VcontKi;
    if(RectRegs.RECTSTAT.bit.Status!=RECT_READY && Vintegral>0) Vintegral=0;
    if(Vintegral>((long)RectRegs.Idem_max<<16)) Vintegral=((long)RectRegs.Idem_max<<16);
    if(Vintegral<((long)RectRegs.Idem_min<<16)) Vintegral=((long)RectRegs.Idem_min<<16);
    Idem=(Vintegral>>16)+verror*LinkRegs.VContKp;
    if(Idem>RectRegs.Idem_max) Idem=RectRegs.Idem_max;
    if(Idem<RectRegs.Idem_min) Idem=RectRegs.Idem_min;
    RectSetI(Idem);
    if(LinkRegs.VdcAv<LinkRegs.VdcDem-VDCUCHARGE) RectRegs.RECTSTAT.bit.Charge=0;
}else{
    RectSetI(0);
    if(LinkRegs.VdcAv>LinkRegs.VdcDem-VDCCHARGE) RectRegs.RECTSTAT.bit.Charge=1;
}

//detect if there is an overvoltage condition in the DC-link voltage
if(LinkRegs.Vdc>LinkRegs.VdcMax){
    RectRegs.RECTSTAT.bit.OverV=1;
    RectRegs.RECTSTAT.bit.OverVClear=0;
}else if(LinkRegs.Vdc<LinkRegs.VdcDem){
    RectRegs.RECTSTAT.bit.OverV=0;
    RectRegs.RECTSTAT.bit.OverVClear=1;
}else{
    RectRegs.RECTSTAT.bit.OverV=0;
    RectRegs.RECTSTAT.bit.OverVClear=0;
}

InvRegs.GridFreq=(InvRegs.GridStep*SPEEDCAL)>>16;

//calculate the time period for EPwm6, for fundamental switching
InvRegs.TPrd=(qinv1(InvRegs.GridFreq)*11328)>>16;
InvRegs.INVCTRL.bit.newprd=1;

//calculate rectifier feedforward voltage, rotating reference frame
Impedence=((long)RectRegs.Speed*(long)RectRegs.CoilL)>>15;
RectRegs.VFFD=-((long)RectRegs.Idemand*(long)Impedence)>>15;
RectRegs.VFFQ=RectRegs.Speed-(((long)RectRegs.Idemand*(long)RectRegs.CoilR)>>15);

//Change of rectifier mode
switch(RectRegs.RECTSTAT.bit.Status){
    case RECT_START:
        //at start, set counter to zero then go to waiting stage
        count=0;
        RectRegs.RECTSTAT.bit.Status=RECT_WAIT;
        break;
    case RECT_WAIT:
        //incremente counter until waiting period is over. Need time for everything to
            settle before calibration is initiated
        count++;
        if(count==STARTWAIT) RectRegs.RECTSTAT.bit.Status=RECT_CAL;
        break;
    case RECT_CAL:
        //run calibration routine, move to preparation stage when complete
        if(RectRegs.RECTSTAT.bit.Cal==1){
            RectRegs.RECTSTAT.bit.Status=RECT_PREP;
```

```
                count=0;
                RectRegs.RECTSTAT.bit.Cal=0;
            }
            break;
        case RECT_PREP:
            //preparation stage, waits until rectifier PLL has locked on to the machine EMF and
                the DC-link has charged, then moves on to ready stage
            if(RectRegs.RECTSTAT.bit.Charge==1 && RectRegs.RECTSTAT.bit.Lock==1){
                count++;
                if(count>LOCKTOTAL){
                    RectRegs.RECTSTAT.bit.Status=RECT_READY;
                    count=0;
                }
            }else{
                count--;
                if(count<0) count=0;
            }
            break;
        case RECT_READY:
            //ready stage, remains unless rectifier PLL falls out of lock
            if(RectRegs.RECTSTAT.bit.Charge==1 && RectRegs.RECTSTAT.bit.Lock==1){
                count++;
                if(count>LOCKMAX) count=LOCKMAX;
            }else{
                count--;
                if(count<=0){
                    RectRegs.RECTSTAT.bit.Status=RECT_PREP;
                }
            }
            break;
        case RECT_FAULT:
            if(RectRegs.RECTSTAT.bit.OverVClear==1) RectRegs.RECTSTAT.bit.Status=RECT_PREP;
            break;
    }

    //change of rectifier mode from modbus register (from host PC)
    switch(RectRegs.RECTSET.bit.Status){
        case RECT_CAL:
            RectRegs.RECTSTAT.bit.Status=RECT_CAL;
            RectRegs.RECTSET.bit.Status=RECT_START;
            break;
        case RECT_PREP:
            RectRegs.RECTSTAT.bit.Status=RECT_PREP;
            RectRegs.RECTSET.bit.Status=RECT_START;
            break;
        case RECT_IDLE:
            RectRegs.RECTSTAT.bit.Status=RECT_IDLE;
            RectRegs.RECTSET.bit.Status=RECT_START;
            break;
    }

    //detect rectifier fault condition
    if(RectRegs.RECTSTAT.bit.OverC==1 || RectRegs.RECTSTAT.bit.OverV==1){
        RectRegs.RECTSTAT.bit.Status=RECT_FAULT;
    }
}
```

C.4 Inverter Fundamental Switching Hardware Interrupt Service Routine

```
//inverter fundamental interrupt sequence
#pragma CODE_SECTION(InvInt2, "RamFuncs")
void InvInt2(void)
{
/*
Inverter fundamental switching is handled by this interrupt. The PWM module EPwm6 is set to have
     the same time period as the fundamental, and the value of the compare register set so that
    this interrupt routine is run at the switching transitions.

ISR only changes the inverter state if the pwm6 interrupt flag is set. This allows the main ADC
    ISR to cancel a pending interrupt by resetting the pwm6 interrupt flag, which is necessary
    when the fundamental mode is enabled, and a spurious interrupt is generated, or possibly
    when re-synchronising. It is really troublesome to properly cancel a pending interrupt, as
    you have to divert it to a blank ISR, let it run, then divert it back, so this is the
    easiest way of doing things.
*/
    if(EPwm6Regs.ETFLG.bit.INT==1){
        //set new inverter state based on previous state, force the inverter outputs to new
            value, set the new state, and the set the compare value for the next switching event
             on EPwm6
        switch(InvRegs.INVCTRL.bit.state){
            case 0:
                //off-on, positive
                EPwm6Regs.CMPA.half.CMPA=InvRegs.ToffPos;
                InvRegs.INVCTRL.bit.state=1;
                EPwm1Regs.AQCSFRC.bit.CSFA=1;
                EPwm1Regs.AQCSFRC.bit.CSFB=2;
                EPwm2Regs.AQCSFRC.bit.CSFA=2;
                EPwm2Regs.AQCSFRC.bit.CSFB=1;
                break;
```

```
            case 1:
                //on-off, positive
                EPwm6Regs.CMPA.half.CMPA=InvRegs.TonNeg;
                InvRegs.INVCTRL.bit.state=2;
                EPwm1Regs.AQCSFRC.bit.CSFA=1;
                EPwm1Regs.AQCSFRC.bit.CSFB=2;
                EPwm2Regs.AQCSFRC.bit.CSFA=1;
                EPwm2Regs.AQCSFRC.bit.CSFB=2;
                break;
            case 2:
                //off-on, negative
                EPwm6Regs.CMPA.half.CMPA=InvRegs.ToffNeg;
                InvRegs.INVCTRL.bit.state=3;
                EPwm1Regs.AQCSFRC.bit.CSFA=2;
                EPwm1Regs.AQCSFRC.bit.CSFB=1;
                EPwm2Regs.AQCSFRC.bit.CSFA=1;
                EPwm2Regs.AQCSFRC.bit.CSFB=2;
                break;
            case 3:
                //on-off, negative
                EPwm6Regs.CMPA.half.CMPA=InvRegs.TonPos;
                InvRegs.INVCTRL.bit.state=0;
                EPwm1Regs.AQCSFRC.bit.CSFA=1;
                EPwm1Regs.AQCSFRC.bit.CSFB=2;
                EPwm2Regs.AQCSFRC.bit.CSFA=1;
                EPwm2Regs.AQCSFRC.bit.CSFB=2;
                break;
        }
    }

    //acknowledge interrupt
    EPwm6Regs.ETCLR.bit.INT=1;
    PieCtrlRegs.PIEACK.all=PIEACK_GROUP3;
}
```